PRELIMINARY

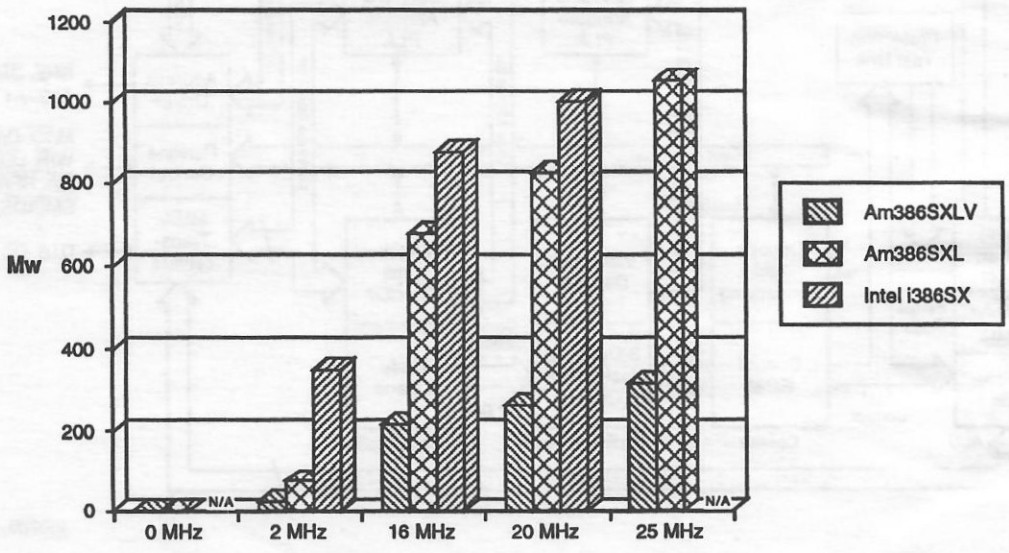
Am386™SXLV

High-Performance, Low-Voltage, 32-Bit Microprocessor with 16-Bit Data Bus

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Operating range 3.0 V to 5.5 V—Ideal for notebook PC designs**
  - —2X improvement in battery life over existing 5 V designs
  - —Wide range of chipsets and other logic available for 3 V systems with support for Standby Mode operation
  - —True static design for long battery life
  - —Power consumption 75% lower than Intel i386SX, 65% lower than Am386SXL microprocessor
  - —Performance on demand (0 to 25 MHz)
- **System Management Mode (SMM) for system and power management**
  - —System Management Interrupt (SMI) for power management independent of processor operating mode and operating system
  - —SMI coupled with I/O instruction break feature provides transparent power off and auto resume of peripherals which may not be "power aware"
  - —SMI is non-maskable and has higher priority than NMI
  - —Automatic save and restore of the microprocessor state
  - —Wide range of chipsets supporting SMM available to allow product differentiation
- **Lower heat dissipation facilitates elimination of the cooling fan in desktop PCs**
- **"Float" input to facilitate system debug and test**
- **Compatible with 386SX systems and software**
- **Supports 387SX-compatible math coprocessors**
- **100-pin PQFP package with optional protective ring for better lead coplanarity**
- **AMD® advanced 0.8 micron CMOS technology**



Typical Power Consumption

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GENERAL DESCRIPTION

The Am386SXLV microprocessor is a low-voltage, true static implementation of the Intel i386SX microprocessor. With the operating range of 3.0 V to 5.5 V, it is ideal for both desktop and battery-powered notebook personal computers. For desktop PCs, this device offers lower heat dissipation, allowing system designers to remove or reduce the size and cost of the cooling fan.

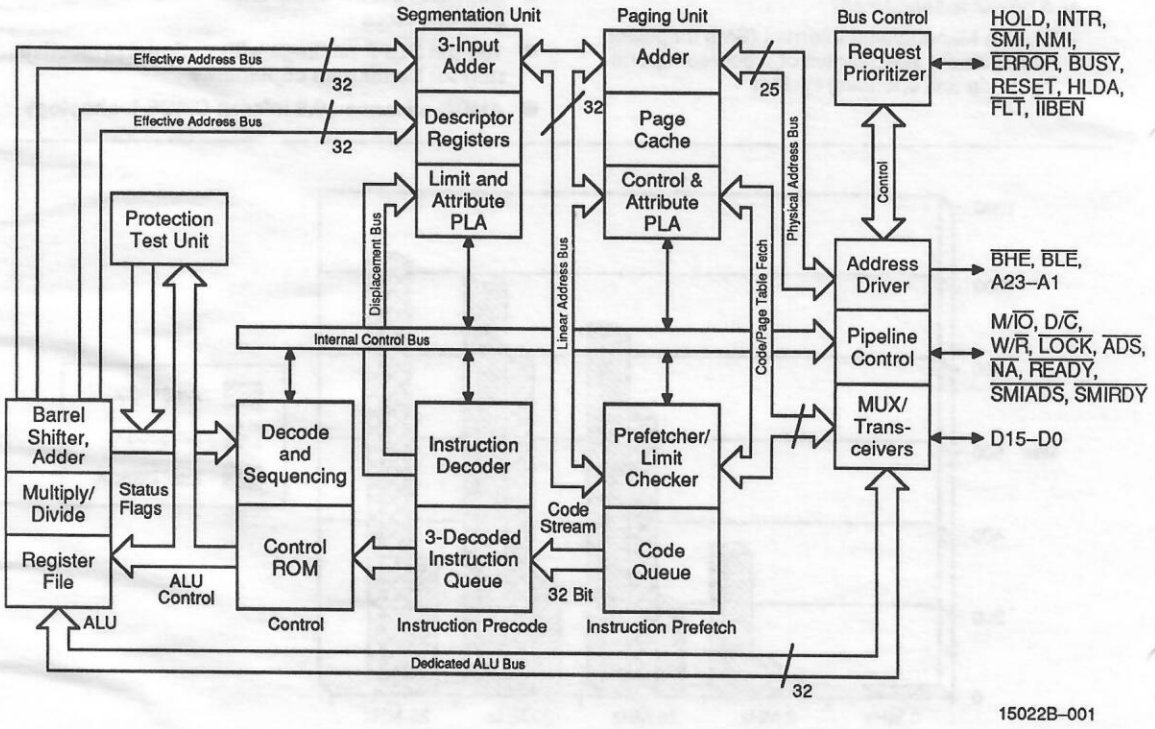
The Am386SXLV microprocessor's lower operating voltage and true static design enables longer battery life and/or lower weight for notebook applications. At 20 MHz, this device has 60% lower operating Icc than the Intel i386SX. Lowering typical operating voltage from 5.0 V to 3.3 V enables battery life to increase by a factor of two. Standby Mode allows the Am386SXLV microprocessor to be clocked down to 0 MHz (DC) and retain full register contents. In Standby Mode, typical current draw is less than 0.01 mA, a greater than 1000X reduction in power consumption versus the Intel i386SX.

The Am386SXLV microprocessor is available in a small footprint 100-pin Plastic Quad Flat Pack (PQFP) package. This package may be shipped in an optional protective ring for better lead protection during shipping.

Additionally, the Am386SXLV microprocessor comes with System Management Mode (SMM) for system and power management. SMI (System Management Interrupt) is a non-maskable, higher priority interrupt than NMI and has its own code space (1 Mb). SMI can be coupled with the I/O instruction break feature to implement transparent power managment of peripherals. SMM can be used by system designers to implement system and power management code independent of the operating system or the Processor Mode.

The Am386SXLV microprocessor incorporates a float pin that places all outputs in a three-state mode to facilitate board test and debug.

BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

Benefits of Lower Operating Voltage

The Am386SXLV microprocessor has an operating voltage range of 3.0 V to 5.5 V. Low voltage allows for lower operating power consumption, longer battery life, and/or smaller batteries for notebook applications.

Because power is proportional to the square of voltage, reduction of the supply voltage from 5.0 V to 3.3 V reduces power consumption by 56%. This directly translates to a doubling of battery life for portable applications. Lower power consumption can also be used to reduce the size and weight of the battery. Thus, 3.3 V designs facilitate a reduction in the form factor. For desktop PCs, low power consumption means elimination of the cooling fan, thus reducing the size and noise of the PC.

A lower operating voltage results in a reduction of I/O voltage swings. This reduces noise generation providing a less hostile environment for board design. It also reduces electromagnetic radiation noise making it easier to obtain FCC approval.

SMM—System Management Mode

The Am386SXLV microprocessor has a new System Management Mode (SMM) for system and power management. This mode consists of two features: System Management Interrupt (SMI) and I/O instruction break.

SMI—System Management Interrupt

SMI is implemented through the use of special bus interface pins. This interrupt method can be used to perform system management functions such as power management independent of Processor Operating Mode (Real, Protected, or Virtual 86 modes).

SMI can also be invoked in software. This allows system software to communicate with SMI power management code. In addition, an instruction called UMOV allows data transfers between SMI and normal system memory spaces.

Activating the $\overline{SMI}$ pin invokes a sequence that saves the operating state of the processor into a separate SMM memory space, independent of the main system memory. After the state is saved, the processor is forced into Real Mode and begins execution at address FFFFF0h in the SMM memory space where a far jump to the SMM code is executed. This Real Mode code can perform its system management function and then resume execution of the normal system software by executing a special opcode sequence which will reload the saved processor state and continue execution in the main system memory space. See Figure 1 for a general flowchart of an SMM operation.

CPU Interface—Pin Functions

The CPU interface for SMM consists of three pins dedicated to the SMI function. One pin, $\overline{SMI}$, is the new interrupt input. The other two pins, $\overline{SMIADS}$ and $\overline{SMIRDY}$, provide the control signals necessary for the separate SMM mode memory space.

Description of SMM Operation

The execution of a System Management Interrupt has four distinct phases: the initiation of the interrupt via $\overline{SMI}$, a processor state save, execution of the SMM interrupt code, and a processor state restore (to resume normal operation).

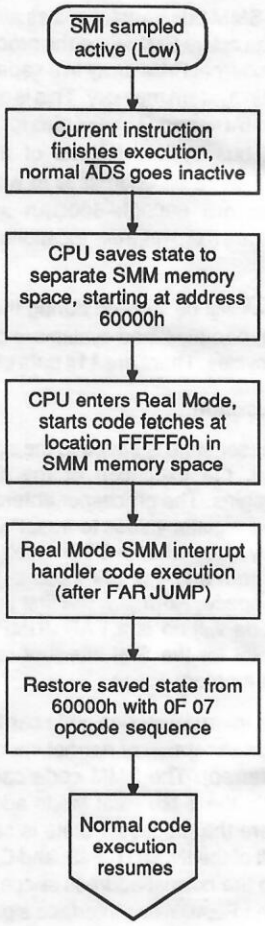


Figure 1. SMM Flow

Interrupt Initiation

A System Management Interrupt is initiated by the driving of an active Low pulse on the $\overline{SMI}$ pin of at least four CLK2 periods. This pulse period will ensure recognition of the interrupt. The CPU will drive the $\overline{SMI}$ pin active after the completion of the current operation (active bus cycle, instruction execution, or both). The active drive of

the pin by the CPU will be released at the end of the interrupt routine following the last register read of the saved state.

While the CPU is in SMM, a bus hold request via the HOLD pin **will be granted.** The HLDA pin will go active after bus release and the $\overline{\text{SMIADS}}$ pin will float along with the other pins that normally float during a bus hold cycle.

Processor State Save

The first set of SMM bus transfer cycles after the CPU's recognition of an active SMI will be the processor saving its state to an external RAM array in a separate address space from main system memory. This is accomplished by using the $\overline{\text{SMIADS}}$ and $\overline{\text{SMIRDY}}$ pins for initiation and termination of bus cycles, instead of the $\overline{\text{ADS}}$ and $\overline{\text{READY}}$ pins. The 32-bit addresses to which the CPU saves its state are 60000h–600CAh and 60100h–60126h. These are fixed address locations for each register saved.

The value of $\overline{\text{NA}}$ will be ignored during the state save. Only full 16-bit, non-pipelined cycles are generated for the state save cycles. There are 114 data transfer cycles

SMI Code Execution

After the processor state is saved to the separate SMM memory space, the execution of the SMI interrupt routine code begins. The processor enters Real Mode, sets most of the register values to "reset" values (those values normally seen after a CPU reset), and begins fetching code from address FFFFF0h in the separate SMM memory space. Normally, the first thing the interrupt routine code will do is a FAR JUMP to the Real Mode entry point for the SMI interrupt routine, which is also in SMM memory space.

Any Real Mode interrupt routine code can be executed, with the obvious exception of normal interrupt routines (which are deferred). The SMM code can be located anywhere within the 1-Mb Real Mode address space, except for where the processor state is saved. I/O cycles, as a result of the IN, OUT, INS, and OUTS instructions, will go to the normal address space, utilizing the normal $\overline{\text{ADS}}$ and $\overline{\text{READY}}$ bus interface signals. This facilitates power management code manipulating system hardware registers as needed through the standard I/O subsystem; a separate I/O space does not need to be implemented.

Processor State Restore (Resuming Normal Execution)

Returning to normal code execution in the main system memory, including restoring the Processor Operating Mode, is accomplished by executing a special code sequence. This code invokes a restore CPU state operation which reloads the CPU registers from the saved data in the RAM controlled by $\overline{\text{SMIADS}}$ and $\overline{\text{SMIRDY}}$.

The ES:EDI register pair must point to physical address 60000h. Then the special opcode sequence 0Fh 07h should be executed to start the restore state operation. After completion of the restore state operation, the $\overline{\text{SMI}}$ pin will be deactivated by the CPU and normal code execution will continue at the point it left off before the SMI occurred. There are 114 data transfer cycles in the restore operation.

Software Features

There are several features of the SMI function that provide support for special operations during the execution of the system's software. These features involve the execution of reserved opcodes to induce specific SMI related operations.

Software SMI Generation

Besides hardware initiation of the System Management Interrupt via the $\overline{\text{SMI}}$ pin, there is also a software induced SMI mechanism. Generating a soft SMI involves setting a control bit in Debug Register 7 (DR7) and executing a reserved opcode (0F1H).

The functional sequence of the software based SMI is identical to the hardware based SMI with the exception that the $\overline{\text{SMI}}$ pin is not initially driven active by an external source. Upon execution of a soft SMI opcode, the $\overline{\text{SMI}}$ pin is driven active (Low) by the processor before the save state operation begins.

Memory Transfers to Main System Memory

While executing an SMI routine, the interrupt code can initiate memory data reads and writes to the main system memory using the normal $\overline{\text{ADS}}$ and $\overline{\text{READY}}$ pins. This is accomplished by using reserved opcodes that are special forms of the MOV instruction (called UMOV). The UMOV opcodes can move byte, word, or double word register operands to or from main system memory. Multiple data transfers using the normal $\overline{\text{ADS}}$ and $\overline{\text{READY}}$ pins will occur if the operands are misaligned relative to the effective address used. The UMOV opcodes are 0F10h, 0F11h, 0F12h, and 0F13h.

I/O Instruction Break

The Am386SXLV microprocessor has an I/O instruction break feature that allows the system logic to implement I/O trapping for peripheral devices. To enable the I/O Instruction break feature, $\overline{\text{IIBEN}}$ must first be asserted active Low. On detecting an I/O instruction, the processor will prevent the execution unit from executing further instructions until $\overline{\text{READY}}$ is driven active Low by the system. Once $\overline{\text{READY}}$ is driven active, the execution unit

will either immediately respond to any active interrupt request or continue executing instructions following the I/O instruction that caused the break.

The I/O instruction break feature can be used to allow system logic to implement I/O trapping for peripheral devices. On sensing an I/O instruction, the system can drive the $\overline{SMI}$ pin active before driving $\overline{READY}$ active. This ensures that the SMI service routine is executed immediately following the I/O instruction that caused the break. (If the I/O instruction break feature is not enabled via $\overline{IIBEN}$, several instructions could execute before the SMI service routine is executed.)

The SMI service routine can access the peripheral for which $\overline{SMI}$ was asserted and modify its state.The SMI service routine will normally return to the instruction following the I/O instruction that caused the break. By modifying the saved state instruction pointer, the routine can choose to return to the I/O instruction that caused the break and re-execute that instruction. The default is to return to the following instruction (except for REP I/O string instruction). To re-execute the I/O instruction that caused the break, the SMI service routine must copy the I/O instruction pointer over the default pointer. This feature is particularly useful when an application program requests an access to a peripheral that has been powered down. The SMI service routine can restore power to the peripheral and initiate a re-execution sequence transparent to the application program. This re-execution feature should only be used if the SMI is in response to an I/O trap with $\overline{IIBEN}$ active. Note that the I/O instruction break feature is not enabled for memory mapped I/O devices or for coprocessor bus cycles even if $\overline{IIBEN}$ is active.

I/O Instruction Break Timing

The I/O Instruction Break feature requires that $\overline{SMI}$ be sampled active (Low) by the processor at least three CLK2 edges before the CLK2 edge that ends the I/O cycle with an active $\overline{READY}$ signal. This timing applies for both pipelined and non-pipelined cycles. If this timing constraint is not met, the next instruction may be executed by the internal execution unit prior to entering SMI Mode, but the $\overline{SMI}$ will be recognized eventually.

True Static Operation

The Am386SXLV microprocessor incorporates a true static design. Unlike dynamic circuit design, the Am386SXLV device eliminates the minimum operating frequency restriction. It may be clocked from its maximum speed of 25 MHz all the way down to 0 MHz (DC). System designers can use this feature to design battery-powered notebook PCs with long battery life.

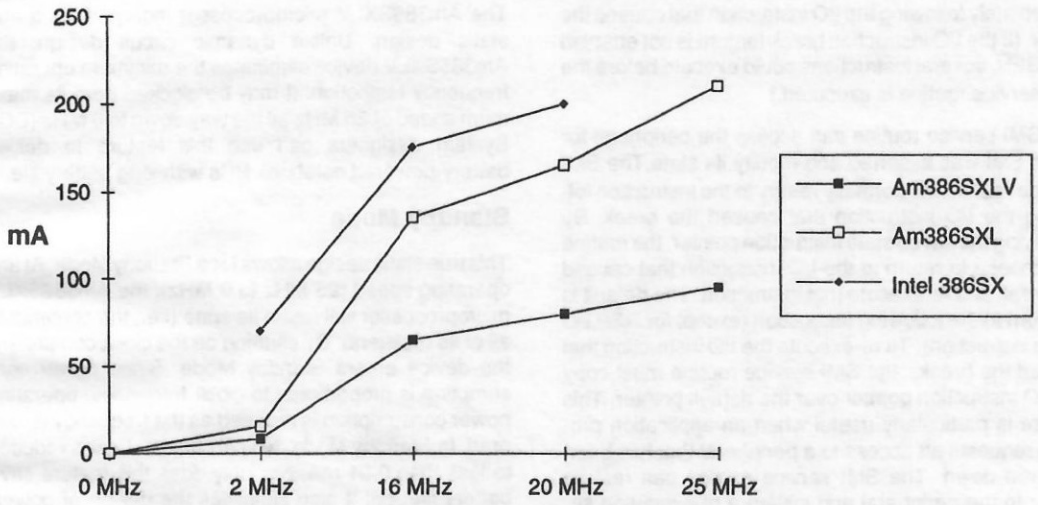
Standby Mode

This true static design allows for a Standby Mode. At any operating speed (25 MHz to 0 MHz), the Am386SXLV microprocessor will retain its state (i.e., the contents of all of its registers). By shutting off the clock completely, the device enters Standby Mode. Since power consumption is proportional to clock frequency, operating power consumption is reduced as the frequency is lowered. In Standby Mode, typical current draw is reduced to less than 0.01 mA. Not only does this feature save battery life, but it also simplifies the design of power-conscious notebook computers in the following ways.

1. Eliminates the need for software in BIOS to save and restore the contents of registers
2. Allows simpler circuitry to control stopping of the clock (since) the system does not need to know what state the processor is in

Lower Operating Icc

True static design also allows lower operating Icc when operating at any speed. See the following graph for typical current at operating speeds.



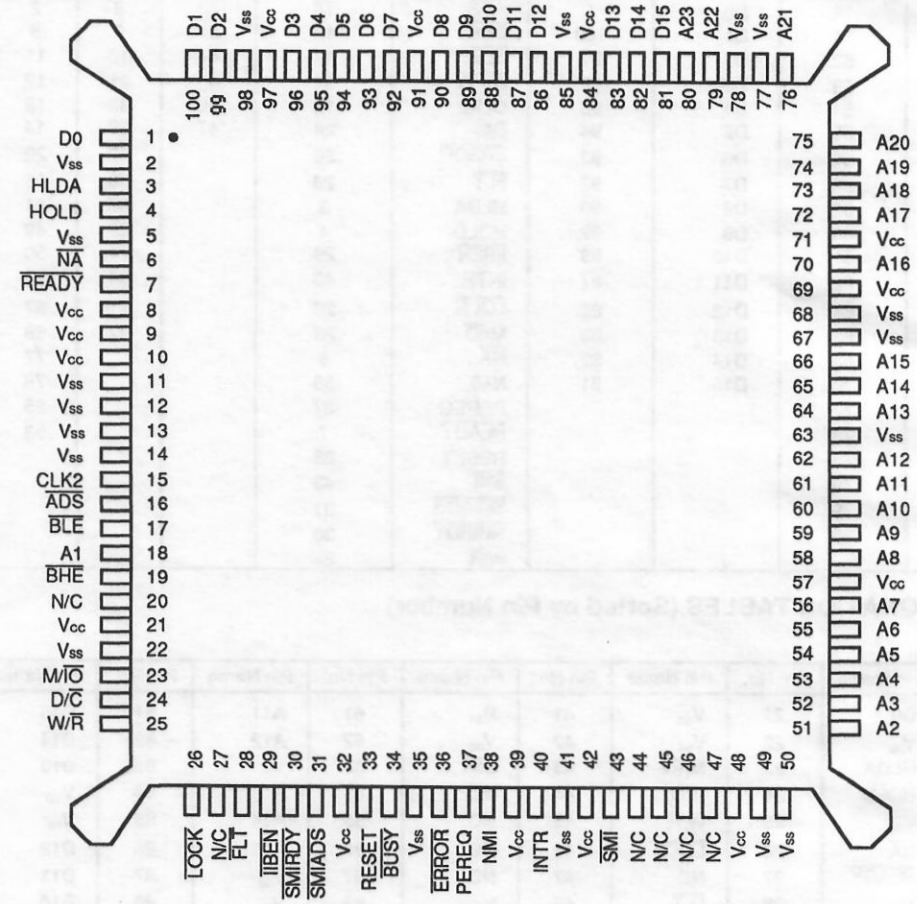
Performance on Demand

The Am386SXLV microprocessor retains its state at any speed from 0 MHz (DC) to its maximum operating speed. With this feature, system designers may vary the operating speed of the system to extend the battery life in notebook systems.

For example, the system could operate at low speeds during inactivity or polling operations. However, upon interrupt, the system clock can be increased up to its maximum speed. After a user-defined time-out period, the system can be returned to a low (or a 0 MHz) operating speed without losing its state. This design maximizes battery life while achieving optimal performance.

CONNECTION DIAGRAM
Top View

100-Pin PQFP



Notes: Pin 1 is marked for orientation.
N/C = Not connected.

PIN DESIGNATION TABLES (Sorted by Pin Name)

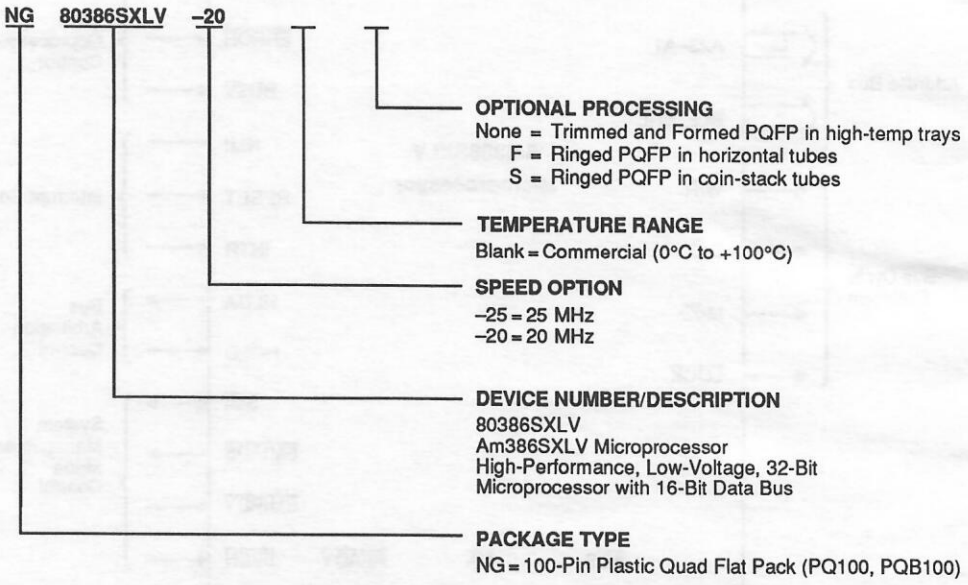
Address		Data		Control		NC	V_{CC}	V_{SS}
Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin No.	Pin No.	Pin No.
A1	18	D0	1	$\overline{ADS}$	16	20	8	2
A2	51	D1	100	$\overline{BHE}$	19	27	9	5
A3	52	D2	99	$\overline{BLE}$	17	44	10	11
A4	53	D3	96	$\overline{BUSY}$	34	45	21	12
A5	54	D4	95	CLK2	15	46	32	13
A6	55	D5	94	D/$\overline{C}$	24	47	39	14
A7	56	D6	93	$\overline{ERROR}$	36		42	22
A8	58	D7	92	$\overline{FLT}$	28		48	35
A9	59	D8	90	HLDA	3		57	41
A10	60	D9	89	HOLD	4		69	49
A11	61	D10	88	$\overline{IIBEN}$	29		71	50
A12	62	D11	87	INTR	40		84	63
A13	64	D12	86	$\overline{LOCK}$	26		91	67
A14	65	D13	83	M/$\overline{IO}$	23		97	68
A15	66	D14	82	$\overline{NA}$	6			77
A16	70	D15	81	NMI	38			78
A17	72			PEREQ	37			85
A18	73			$\overline{READY}$	7			98
A20	75			RESET	33			
A21	76			$\overline{SMI}$	43			
A22	79			$\overline{SMIADS}$	31			
A23	80			$\overline{SMIRDY}$	30			
				W/$\overline{R}$	25			

PIN DESIGNATION TABLES (Sorted by Pin Number)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	D0	21	V_{CC}	41	V_{SS}	61	A11	81	D15
2	V_{SS}	22	V_{SS}	42	V_{CC}	62	A12	82	D14
3	HLDA	23	M/$\overline{IO}$	43	$\overline{SMI}$	63	V_{SS}	83	D13
4	HOLD	24	D/$\overline{C}$	44	NC	64	A13	84	V_{CC}
5	V_{SS}	25	W/$\overline{R}$	45	NC	65	A14	85	V_{SS}
6	$\overline{NA}$	26	$\overline{LOCK}$	46	NC	66	A15	86	D12
7	$\overline{READY}$	27	NC	47	NC	67	V_{SS}	87	D11
8	V_{CC}	28	$\overline{FLT}$	48	V_{CC}	68	V_{SS}	88	D10
9	V_{CC}	29	$\overline{IIBEN}$	49	V_{SS}	69	V_{CC}	89	D9
10	V_{CC}	30	$\overline{SMIRDY}$	50	V_{SS}	70	A16	90	D8
11	V_{SS}	31	$\overline{SMIADS}$	51	A2	71	V_{CC}	91	V_{CC}
12	V_{SS}	32	V_{CC}	52	A3	72	A17	92	D7
13	V_{SS}	33	RESET	53	A4	73	A18	93	D6
14	V_{SS}	34	$\overline{BUSY}$	54	A5	74	A19	94	D5
15	CLK2	35	V_{SS}	55	A6	75	A20	95	D4
16	$\overline{ADS}$	36	$\overline{ERROR}$	56	A7	76	A21	96	D3
17	$\overline{BLE}$	37	PEREQ	57	V_{CC}	77	V_{SS}	97	V_{CC}
18	A1	38	NMI	58	A8	78	V_{SS}	98	V_{SS}
19	$\overline{BHE}$	39	V_{CC}	59	A9	79	A22	99	D2
20	NC	40	INTR	60	A10	80	A23	100	D1

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

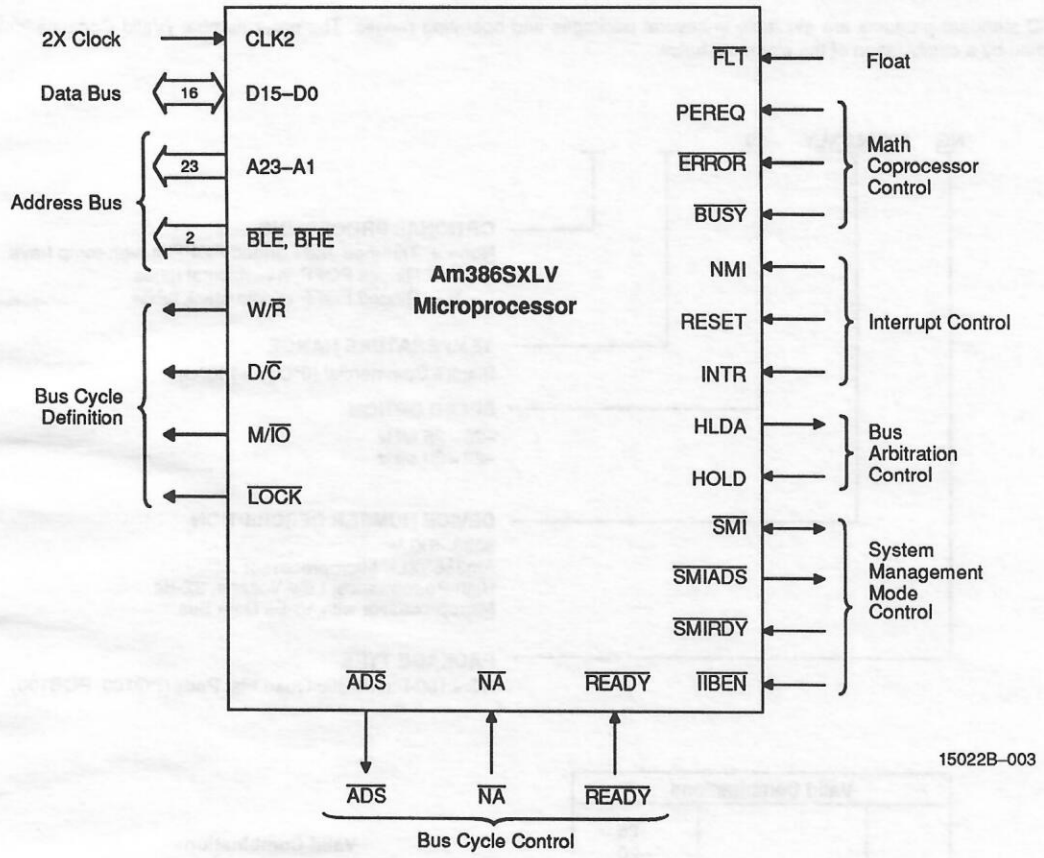


Valid Combinations		
NG	80386SXLV	–25 –20
		–25F –20F
		–25S –20S

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

LOGIC SYMBOL



PIN DESCRIPTIONS

A23–A1
Address Bus (Outputs)

Outputs physical memory or port I/O addresses.

$\overline{ADS}$
Address Status (Active Low; Output)

Indicates that a valid bus cycle definition and address (W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{BHE}$, $\overline{BLE}$, and A23–A1) are being driven at the Am386SXLV microprocessor pins.

$\overline{BHE}$, $\overline{BLE}$
Byte Enables (Active Low; Outputs)

Indicate which data bytes of the data bus take part in a bus cycle.

$\overline{BUSY}$
Busy (Active Low; Input)

Signals a busy condition from a processor extension. $\overline{BUSY}$ has an internal pullup resistor.

CLK2
CLK2 (Input)

Provides the fundamental timing for the Am386SXLV microprocessor.

D15–D0
Data Bus (Inputs/Outputs)

Inputs data during memory, I/O, and interrupt acknowledge read cycles; outputs data during memory and I/O write cycles.

D/$\overline{C}$
Data/Control (Output)

A bus cycle definition pin that distinguishes data cycles, either memory or I/O, from control cycles which are: interrupt acknowledge, halt, and code fetch.

$\overline{ERROR}$
Error (Active Low; Input)

Signals an error condition from a processor extension. $\overline{ERROR}$ has an internal pullup resistor.

$\overline{FLT}$
Float (Active Low; Input)

An input which forces all bi-directional and output signals, including HLDA, to the three-state condition. $\overline{FLT}$ has an internal pullup resistor. The pin, if not used, should be disconnected.

HLDA
Bus Hold Acknowledge (Active High; Output)

Output indicates that the Am386SXLV microprocessor has surrendered control of its logical bus to another bus master.

HOLD
Bus Hold Request (Active High; Input)

Input allows another bus master to request control of the local bus.

$\overline{IIBEN}$
I/O Instruction Break Enable (Active Low; Input)

Enables the I/O instruction break feature. $\overline{IIBEN}$ has an internal pullup resistor.

INTR
Interrupt Request (Active High; Input)

A maskable input that signals the Am386SXLV microprocessor to suspend execution of the current program and execute an interrupt acknowledge function.

$\overline{LOCK}$
Bus Lock (Active Low; Output)

A bus cycle definition pin that indicates that other system bus masters are not to gain control of the system bus while it is active.

M/$\overline{IO}$
Memory/IO (Output)

A bus cycle definition pin that distinguishes memory cycles from input/output cycles.

$\overline{NA}$
Next Address (Active Low; Input)

Used to request address pipelining.

NC
No Connect

Should always be left unconnected. Connection of a NC pin may cause the processor to malfunction or be incompatible with future steppings of the Am386SXLV microprocessor.

NMI
Non-Maskable Interrupt Request (Active High; Input)

A non-maskable input that signals the Am386SXLV microprocessor to suspend execution of the current program and execute an interrupt acknowledge function.

PEREQ
Processor Extension Request (Active High; Input)

Indicates that the processor has data to be transferred by the Am386SXLV microprocessor. PEREQ has an internal pulldown resistor.

$\overline{\text{READY}}$
Bus Ready (Active Low; Input)

Terminates the bus cycle.

RESET
Reset (Active High; Input)

Suspends any operation in progress and places the Am386SXLV microprocessor in a known reset state.

$\overline{\text{SMI}}$
System Management Interrupt (Active Low; I/O)

A non-maskable interrupt pin which signals the Am386SXLV microprocessor to suspend execution and enter System Management Mode. $\overline{\text{SMI}}$ has an internal pullup resistor.

$\overline{\text{SMIADS}}$
SMI Address Status (Active Low Three-State; Output)

When active, this pin indicates that a valid bus cycle definition and address (W/$\overline{\text{R}}$ D/$\overline{\text{C}}$, M/$\overline{\text{IO}}$, $\overline{\text{BHE}}$, $\overline{\text{BLE}}$, and A23–A1) are being driven at the Am386SXLV microprocessor pins while in the System Management Mode.

$\overline{\text{SMIRDY}}$
SMI Ready (Active Low; Input)

This input terminates the current bus cycle to the SMM Mode address space in the same manner as the $\overline{\text{READY}}$ pin does for the normal mode address space. $\overline{\text{SMIRDY}}$ has an internal pullup resistor.

V_{cc}
System Power (Active High; Input)

Provides the DC supply input.

V_{ss}
System Ground (Input)

Provides the 0-V connection from which all inputs and outputs are measured.

W/$\overline{\text{R}}$
Write/Read (Output)

A bus cycle definition pin that distinguishes write cycles from read cycles.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C
Ambient Temperature Under Bias . –65°C to +125°C

Stresses above those listed may cause permanent damage to the device. Functionality at or above these limits is not implied. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods of time may affect device reliability.

OPERATING RANGES

Supply Voltage with respect to V_{SS} . . –0.5 V to +7.0 V
Voltage on Other Pins . . . . . –0.5 V to V_{CC} +0.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges

V_{CC} = 3.0 V to 3.6 V; T_{CASE} = 0°C to +100°C

			Preliminary		
Symbol	Parameter Description	Notes	Min	Max	Unit
V_{IL}	Input Low Voltage	(Note 1)	–0.3	+0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+0.3	V
V_{ILC}	CLK2 Input Low Voltage	(Note 1)	–0.3	+0.8	V
V_{IHC}	CLK2 Input High Voltage 16, 20 MHz		V_{CC}–0.6	V_{CC}+0.3	V
V_{OL}	Output Low Voltage I_{OL} = 0.5 mA: A23–A1, D15–D0 I_{OL} = 0.5 mA: $\overline{BHE}$, $\overline{BLE}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, $\overline{SMIADS}$, HLDA I_{OL} = 2 mA: A23–A1, D15–D0 I_{OL} = 2.5 mA: $\overline{BHE}$, $\overline{BLE}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, $\overline{SMIADS}$, HLDA	(Note 5)		 0.2 0.2 0.45 0.45	 V V V V
V_{OH}	Output High Voltage I_{OH} = 0.1 mA: A23–A1, D15–D0 I_{OH} = 0.1 mA: $\overline{BHE}$, $\overline{BLE}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, $\overline{SMIADS}$, HLDA I_{OH} = 0.5 mA: A23–A1, D15–D0 I_{OH} = 0.5 mA: $\overline{BHE}$, $\overline{BLE}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, $\overline{SMIADS}$, HLDA	(Note 5)	 V_{CC}– 0.2 V_{CC}– 0.2 V_{CC}– 0.45 V_{CC}– 0.45		 V V V V
I_{LI}	Input Leakage Current (All pins except PEREQ, $\overline{BUSY}$, $\overline{ERROR}$, $\overline{SMI}$, $\overline{SMIRDY}$, $\overline{FLT}$, $\overline{IIBEN}$)	0 V ≤ V_{IN} ≤ V_{CC}		±15	µA
I_{IH}	Input Leakage Current (PEREQ pin)	V_{IH} = V_{CC}–0.1 V V_{IH} = 2.4 V (Note 2)		300 200	µA µA
I_{IL}	Input Leakage Current ($\overline{BUSY}$, $\overline{ERROR}$, $\overline{SMI}$, $\overline{SMIRDY}$, $\overline{FLT}$, $\overline{IIBEN}$)	V_{IL} = 0.1 V V_{IL} = 0.45 V (Note 3)		–300 –200	µA µA
I_{LO}	Output Leakage Current	0.1 V ≤ V_{OUT} ≤ V_{CC}		±15	µA
I_{CC}	Supply Current CLK2 = 32 MHz: Oper. Freq. 16 MHz CLK2 = 40 MHz: Oper. Freq. 20 MHz CLK2 = 50 MHz: Oper. Freq. 25 MHz	 I_{CC} Typ = 65 I_{CC} Typ = 80 I_{CC} Typ = 95		 95 110 125	 mA mA mA
I_{CCSB}	Standby Current	I_{CCSB} Typ=10		150	µA
C_{IN}	Input or I/O Capacitance	F_c = 1 MHz (Note 4)		10	pF
C_{OUT}	Output Capacitance	F_c = 1 MHz (Note 4)		12	pF
C_{CLK}	CLK2 Capacitance	F_c = 1 MHz (Note 4)		20	pF

Notes: 1. The min value, –0.3, is not 100% tested.
2. $\overline{PEREQ}$ input has an internal pulldown resistor.
3. $\overline{BUSY}$, $\overline{ERROR}$, $\overline{FLT}$, $\overline{SMI}$, $\overline{IIBEN}$, and $\overline{SMIRDY}$ inputs each have an internal pullup resistor.
4. Not 100% tested.
5. Outputs are CMOS and will pull rail to rail if the load is not resistive.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C
Ambient Temperature under Bias . –65°C to +125°C

Stresses above those listed may cause permanent damage to the device. Functionality at or above these limits is not implied. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods of time may affect device reliability.

OPERATING RANGES

Supply Voltage with respect to V_{SS} . . . –0.5 V to +7 V
Voltage on Other Pins . . . . . –0.5 V to V_{CC} +0.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges

V_{CC} = 3.6 V to 5.5 V; T_{CASE} = 0°C to +100°C

			Preliminary		
Symbol	**Parameter Description**	**Notes**	**Min**	**Max**	**Unit**
V_{IL}	Input Low Voltage	(Note 1)	–0.3	+0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+0.3	V
V_{ILC}	CLK2 Input Low Voltage	(Note 1)	–0.3	+0.8	V
V_{IHC}	CLK2 Input High Voltage		V_{CC}–0.8	V_{CC}+0.3	V
V_{OL}	Output Low Voltage I_{OL} = 4 mA: A23–A1, D15–D0 I_{OL} = 5 mA: $\overline{BHE}$, $\overline{BLE}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, $\overline{SMIADS}$, HLDA	(Note 5)		0.45 0.45	V V
V_{OH}	Output High Voltage I_{OH} = 1.0 mA: A23–A1, D15–D0 I_{OH} = 0.2 mA: A23–A1, D15–D0 I_{OH} = 0.9 mA: $\overline{BHE}$, $\overline{BLE}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, $\overline{SMIADS}$, HLDA I_{OH} = 0.18 mA: $\overline{BHE}$, $\overline{BLE}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, $\overline{SMIADS}$, HLDA	(Note 5)	2.4 V_{CC}–0.5 2.4 V_{CC}–0.5		V V V V
I_{LI}	Input Leakage Current (All pins except PEREQ, $\overline{BUSY}$, $\overline{ERROR}$, $\overline{SMI}$, $\overline{SMIRDY}$, $\overline{FLT}$, and $\overline{IIBEN}$)	0 V ≤ V_{IN} ≤ V_{CC}		±15	µA
I_{IH}	Input Leakage Current (PEREQ pin)	V_{IH} = 2.4 V (Note 2)		200	µA
I_{IL}	Input Leakage Current ($\overline{BUSY}$, $\overline{ERROR}$, $\overline{SMI}$, $\overline{SMIRDY}$, $\overline{FLT}$, $\overline{IIBEN}$)	V_{IL} = 0.45 V (Note 3)		–400	µA
I_{LO}	Output Leakage Current	0.45 V ≤ V_{OUT} ≤ V_{CC}		±15	µA
I_{CC}	Supply Current CLK2 = 32 MHz: Oper. Freq. 16 MHz CLK2 = 40 MHz: Oper. Freq. 20 MHz CLK2 = 50 MHz: Oper. Freq. 25 MHz	V_{CC} = 5.5 V I_{CC} Typ = 135 I_{CC} Typ = 165 I_{CC} Typ = 210		 160 200 250	 mA mA mA
I_{CCSB}	Standby Current	I_{CCSB} Typ = 0.02 mA		0.15	mA
C_{IN}	Input or I/O Capacitance	F_C = 1 MHz (Note 4)		10	pF
C_{OUT}	Output Capacitance	F_C = 1 MHz (Note 4)		12	pF
C_{CLK}	CLK2 Capacitance	F_C = 1 MHz (Note 4)		20	pF

Notes: 1. The min value, –0.3, is not 100% tested.
2. $\overline{PEREQ}$ input has an internal pulldown resistor.
3. $\overline{BUSY}$, $\overline{ERROR}$, $\overline{FLT}$, $\overline{SMI}$, $\overline{IIBEN}$, and $\overline{SMIRDY}$ inputs each have an internal pullup resistor.
4. Not 100% tested.
5. Outputs are CMOS and will pull rail to rail if the load is not resistive.

SWITCHING CHARACTERISTICS

The switching characteristics given consist of output delays, input setup requirements, and input hold requirements. All switching characteristics are relative to the CLK2 rising edge crossing the 2.0 V level.

Switching characteristic measurement is defined by Figure 2. Inputs must be driven to the voltage levels indicated by Figure 2 when switching characteristics are measured. Output delays are specified with minimum and maximum limits measured, as shown. The minimum delay times are hold times provided to external circuitry. Input setup and hold times are specified as minimums, defining the smallest acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct operation.

Outputs $\overline{ADS}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{BHE}$, $\overline{BLE}$, $\overline{SMIADS}$, A23–A1, and HLDA only change at the beginning of phase one. D15–D0 (write cycles) only change at the beginning of phase two. The $\overline{READY}$, HOLD, $\overline{BUSY}$, $\overline{SMIRDY}$, $\overline{ERROR}$, PEREQ, $\overline{FLT}$, and D15–D0 (read cycles) inputs are sampled at the beginning of phase one. The $\overline{NA}$, INTR, NMI, and $\overline{SMI}$ inputs are sampled at the beginning of phase two.

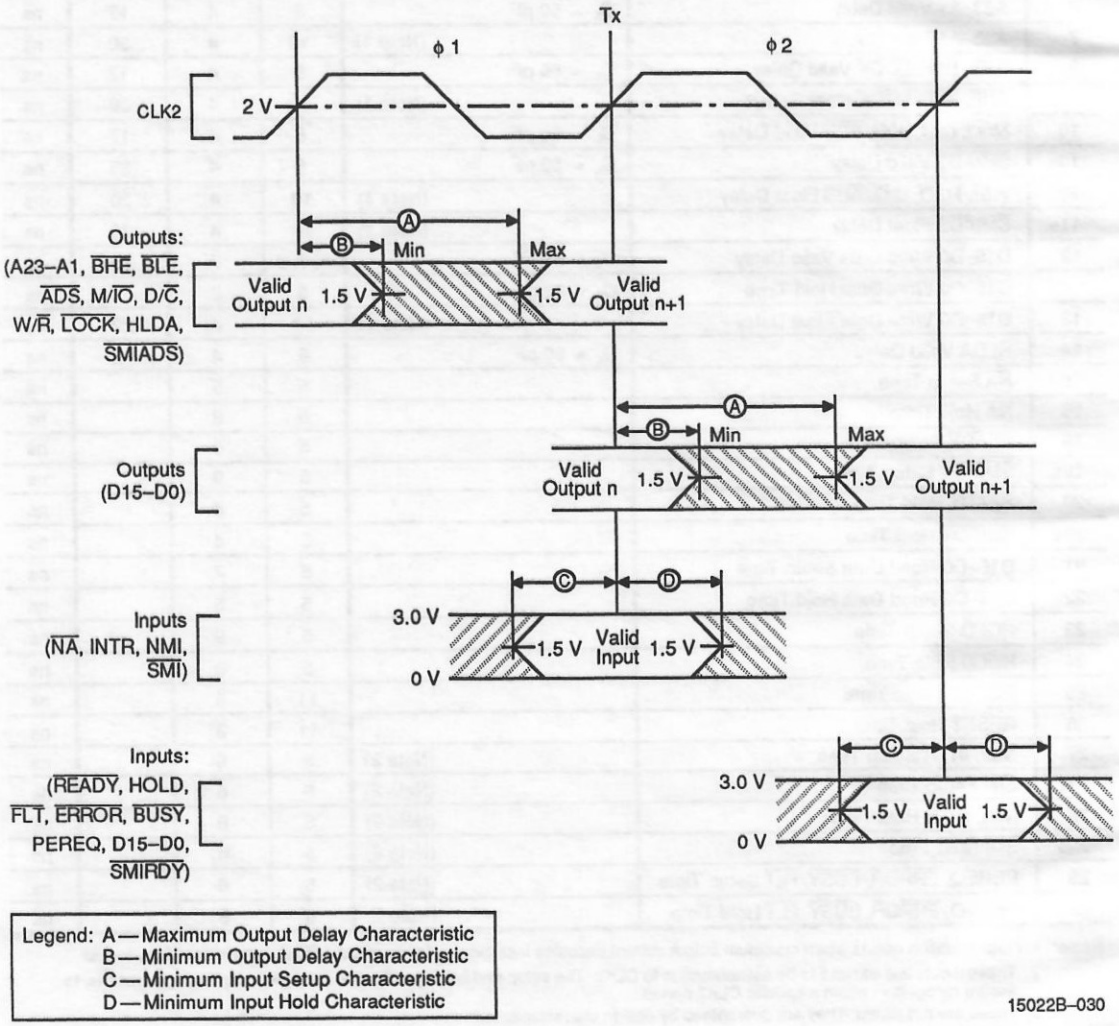


Figure 2. Drive Levels and Measurement Points for Switching Characteristics

SWITCHING CHARACTERISTICS over operating ranges at 25 MHz

V_{CC} = 3.0 V –5.5 V; T_{CASE} = 0°C to 100°C

			Preliminary			
Symbol	Parameter Description	Notes	Ref. Figures	Min	Max	Unit
	Operating Frequency	Half CLK2 freq.		0	25	MHz
1	CLK2 Period		3	20		ns
2a	CLK2 High Time	at 2 V	3	7		ns
2b	CLK2 High Time	at (V_{CC}–0.8 V)	3	4		ns
3a	CLK2 Low Time	at 2 V	3	7		ns
3b	CLK2 Low Time	at 0.8 V	3	5		ns
4	CLK2 Fall Time	(V_{CC}–0.8 V) to 0.8 V (Note 3)	3		7	ns
5	CLK2 Rise Time	0.8 V to (V_{CC}–0.8 V) (Note 3)	3		7	ns
6	A23–A1 Valid Delay	C_L = 50 pF	6	4	17	ns
7	A23–A1 Float Delay	(Note 1)	10	4	30	ns
8	$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ Valid Delay	C_L = 50 pF	6	4	17	ns
9	$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ Float Delay	(Note 1)	10	4	30	ns
10	M/$\overline{IO}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{ADS}$ Valid Delay	C_L = 50 pF	6	4	17	ns
10s	$\overline{SMIADS}$ Valid Delay	C_L = 50 pF	6	4	25	ns
11	W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$, $\overline{ADS}$ Float Delay	(Note 1)	10	4	30	ns
11s	$\overline{SMIADS}$ Float Delay	(Note 1)	10	4	30	ns
12	D15–D0 Write Data Valid Delay	C_L = 50 pF	6, 7, 9	7	23	ns
12a	D15–D0 Write Data Hold Time	C_L = 50 pF	8	2		ns
13	D15–D0 Write Data Float Delay	(Note 1)	10	4	22	ns
14	HLDA Valid Delay	C_L = 50 pF	6	4	22	ns
15	$\overline{NA}$ Setup Time		5	5		ns
16	$\overline{NA}$ Hold Time		5	3		ns
19	$\overline{READY}$ Setup Time		5	9		ns
19s	$\overline{SMIRDY}$ Setup Time		5	9		ns
20	$\overline{READY}$ Hold Time		5	4		ns
20s	$\overline{SMIRDY}$ Hold Time		5	4		ns
21	D15–D0 Read Data Setup Time		5	7		ns
22	D15–D0 Read Data Hold Time		5	5		ns
23	HOLD Setup Time		5	9		ns
24	HOLD Hold Time		5	3		ns
25	RESET Setup Time		11	8		ns
26	RESET Hold Time		11	3		ns
27	NMI, INTR Setup Time	(Note 2)	5	6		ns
27s	$\overline{SMI}$ Setup Time	(Note 2)	5	6		ns
28	NMI, INTR Hold Time	(Note 2)	5	6		ns
28s	$\overline{SMI}$ Hold Time	(Note 2)	5	6		ns
29	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$ Setup Time	(Note 2)	5	6		ns
30	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$ Hold Time	(Note 2)	5	5		ns

Notes: 1. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not 100% tested.
2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
3. These are not tested. They are guaranteed by design characterization.

SWITCHING CHARACTERISTICS over operating ranges at 20 MHz

V_{CC} = 3.0 V to 5.5 V; T_{CASE} = 0°C to 100°C

			Preliminary			
Symbol	Parameter Description	Notes	Ref. Figures	Min	Max	Unit
	Operating Frequency	Half CLK2 freq.		0	20	MHz
1	CLK2 Period		3	25		ns
2a	CLK2 High Time	at 2 V	3	8		ns
2b	CLK2 High Time	at (V_{CC}–0.8 V)	3	5		ns
3a	CLK2 Low Time	at 2 V	3	8		ns
3b	CLK2 Low Time	at 0.8 V	3	6		ns
4	CLK2 Fall Time	(V_{CC}–0.8 V) to 0.8 V (Note 3)	3		8	ns
5	CLK2 Rise Time	0.8 V to (V_{CC}–0.8 V) (Note 3)	3		8	ns
6	A23–A1 Valid Delay	C_L = 120 pF (Note 4)	6	4	30	ns
7	A23–A1 Float Delay	(Note 1)	10	4	32	ns
8	$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ Valid Delay	C_L = 75 pF (Note 4)	6	4	30	ns
9	$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ Float Delay	(Note 1)	10	4	32	ns
10a	M/$\overline{IO}$, D/$\overline{C}$ Valid Delay	C_L = 75 pF (Note 4)	6	4	28	ns
10b	W/$\overline{R}$, $\overline{ADS}$ Valid Delay	C_L = 75 pF (Note 4)	6	4	26	ns
10s	$\overline{SMIADS}$ Valid Delay	C_L = 75 pF (Note 4)	6	4	26	ns
11	W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$, $\overline{ADS}$ Float Delay	(Note 1)	10	6	30	ns
11s	$\overline{SMIADS}$ Float Delay	(Note 1)	10	4	30	ns
12	D15–D0 Write Data Valid Delay	C_L = 120 pF (Note 4)	6, 7, 9	4	38	ns
13	D15–D0 Write Data Float Delay	(Note 1)	10	4	27	ns
14	HLDA Valid Delay	C_L = 75 pF (Note 4)	6	4	28	ns
15	$\overline{NA}$ Setup Time		5	5		ns
16	$\overline{NA}$ Hold Time		5	12		ns
19	$\overline{READY}$ Setup Time		5	12		ns
19s	$\overline{SMIRDY}$ Setup Time		5	12		ns
20	$\overline{READY}$ Hold Time		5	4		ns
20s	$\overline{SMIRDY}$ Hold Tme		5	4		ns
21	D15–D0 Read Data Setup Time		5	9		ns
22	D15–D0 Read Data Hold Time		5	6		ns
23	HOLD Setup Time		5	17		ns
24	HOLD Hold Time		5	5		ns
25	RESET Setup Time		11	12		ns
26	RESET Hold Time		11	4		ns
27	NMI, INTR Setup Time	(Note 2)	5	16		ns
27s	$\overline{SMI}$ Setup Time	(Note 2)	5	16		ns
28	NMI, INTR Hold Time	(Note 2)	5	16		ns
28s	$\overline{SMI}$ Hold Time	(Note 2)	5	16		ns
29	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$ Setup Time	(Note 2)	5	14		ns
30	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$ Hold Time	(Note 2)	5	5		ns

Notes:
1. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not 100% tested.
2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
3. These are not tested. They are guaranteed by design characterization.
4. Tested with C_L set at 50 pF and derated to support the indicated distributed capacitive load. See Figures 12–14 for the capacitive derating curve.

SWITCHING CHARACTERISTICS (continued)

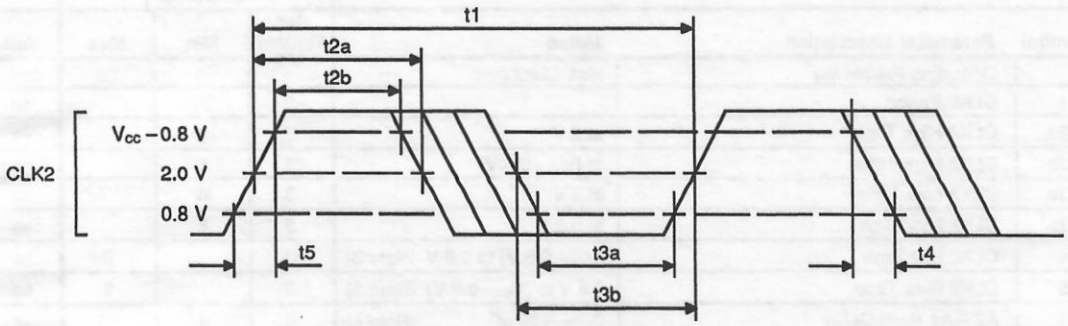


Figure 3. CLK2 Timing

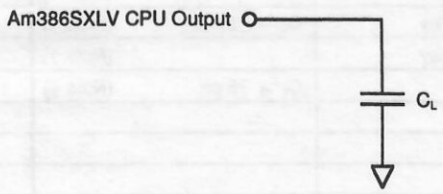
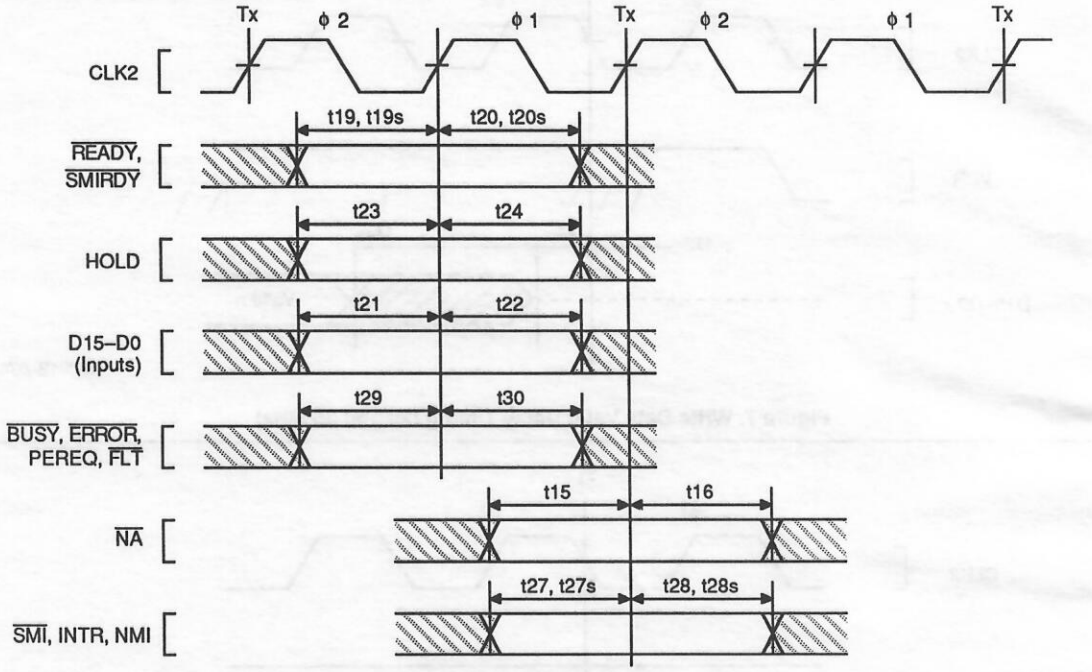


Figure 4. AC Test Circuit

SWITCHING WAVEFORMS



15022B–033

Figure 5. Input Setup and Hold Timing

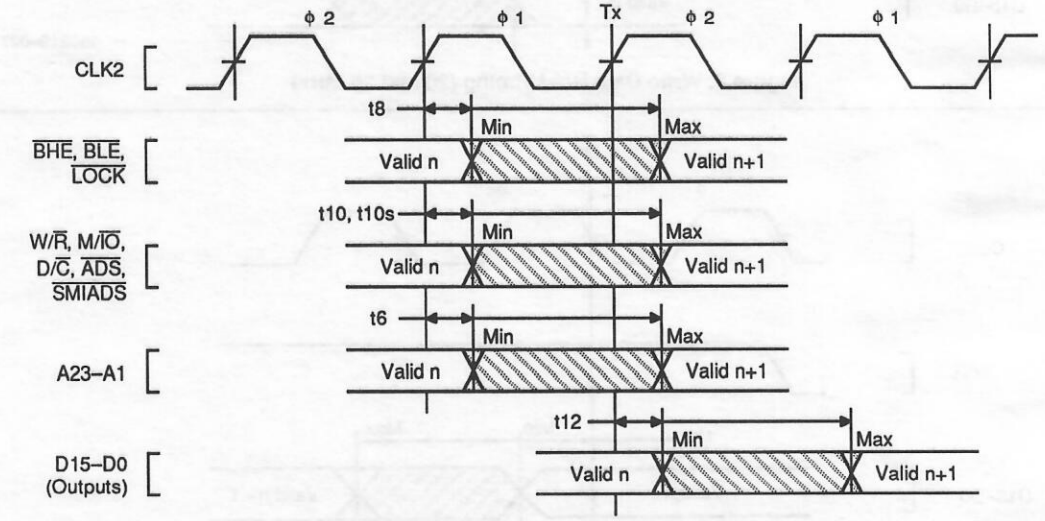


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Figure 6. Output Valid Delay Timing

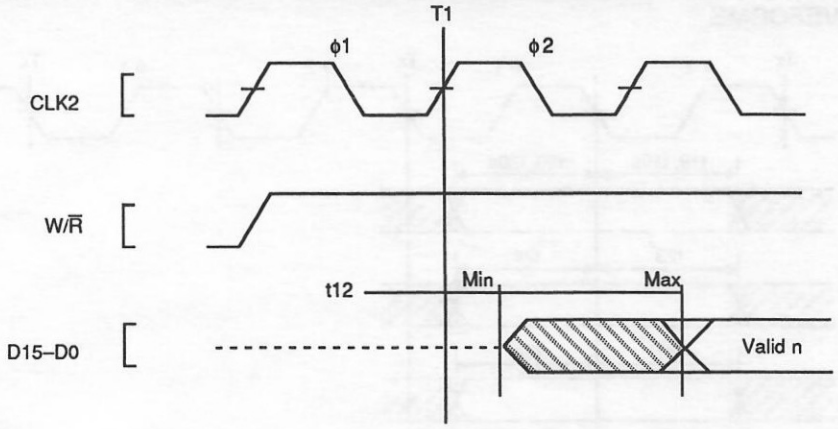

Figure 7. Write Data Valid Delay Timing (20 and 25 MHz)

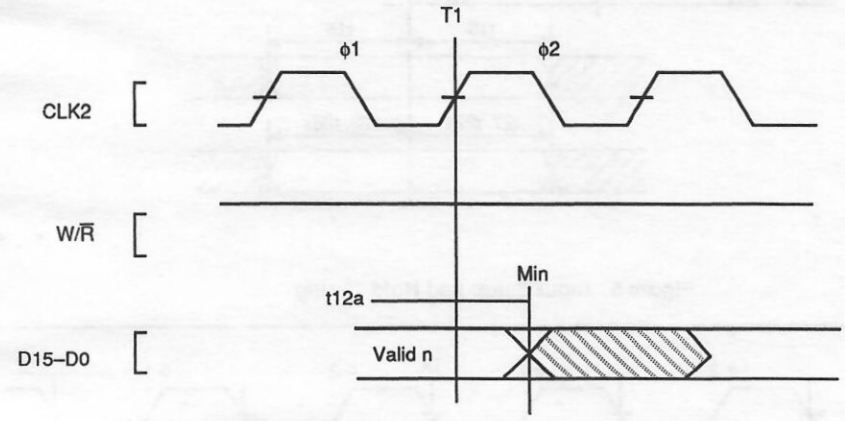

Figure 8. Write Data Hold Timing (20 and 25 MHz)

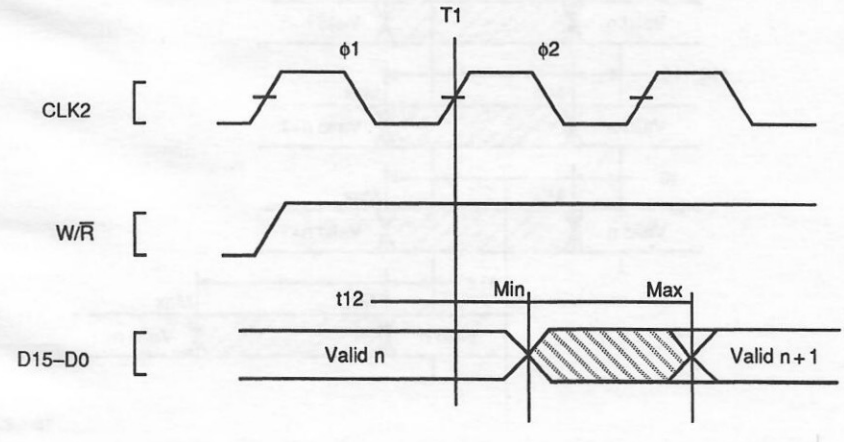

Figure 9. Write Data Valid Delay Timing (20 MHz)

SWITCHING WAVEFORMS (continued)

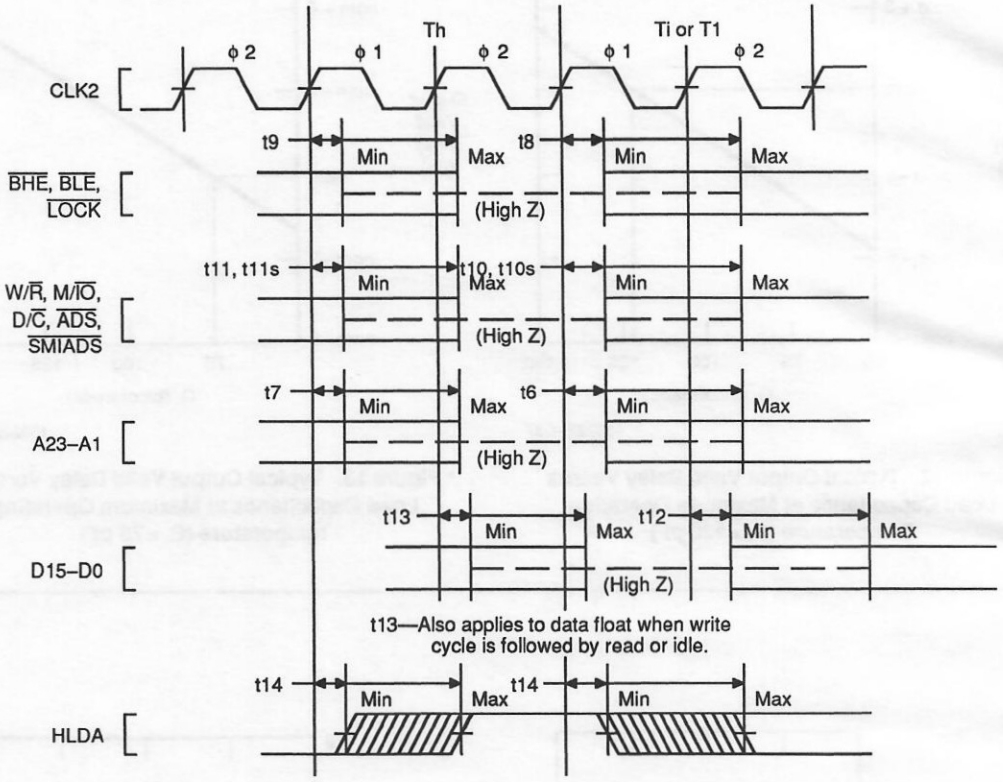

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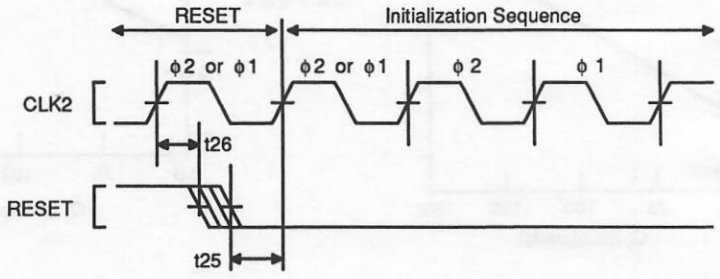
Figure 10. Output Float Delay and HLDA Valid Delay Timing



15022B–036

Figure 11. RESET Setup and Hold Timing and Internal Phase

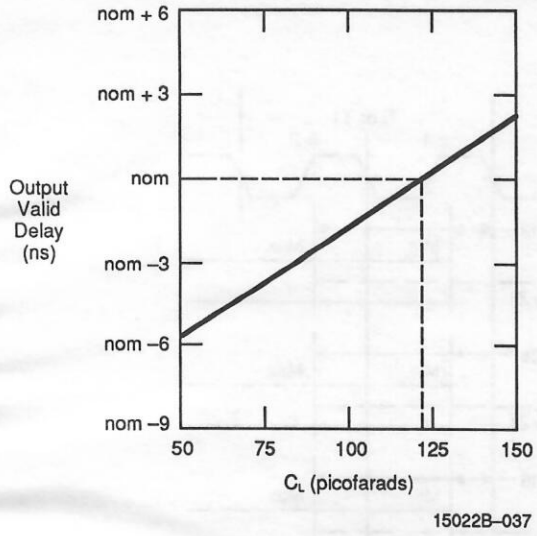


Figure 12. Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature (C_L = 120 pF)

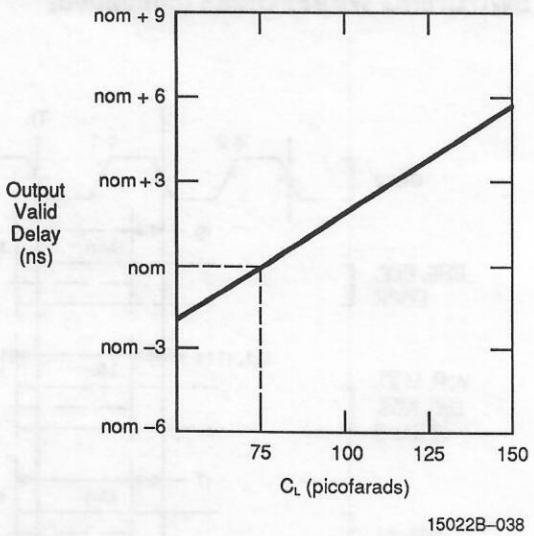


Figure 13. Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature (C_L = 75 pF)

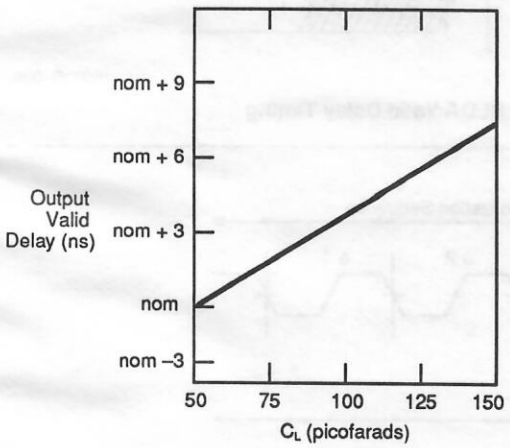


Figure 14. Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature (C_L = 50 pF)

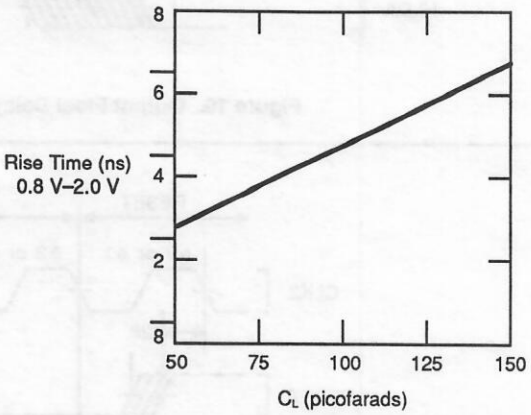
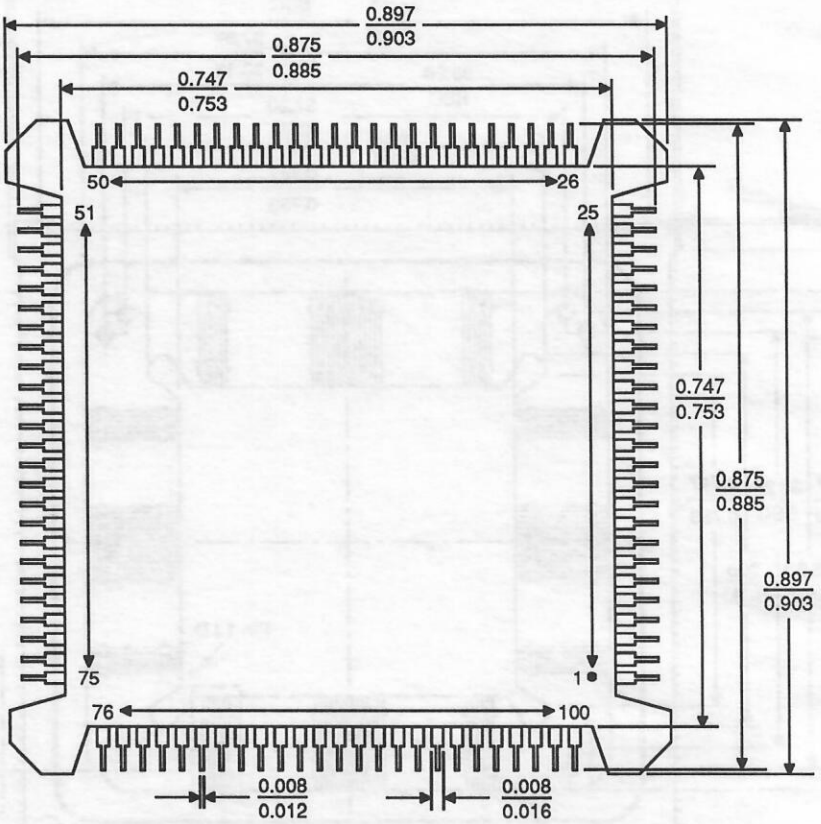


Figure 15. Typical Output Rise Time Versus Load Capacitance at Maximum Operating Temperature

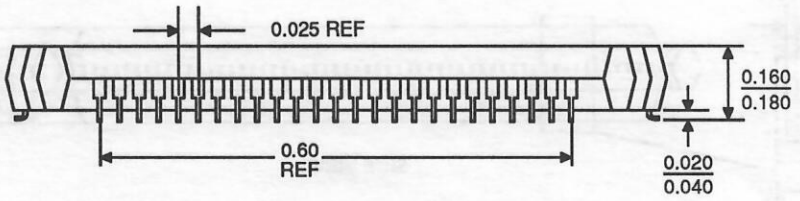
PHYSICAL DEMENSIONS

For reference only. Dimensions are measured in millimeters unless otherwise noted. BSC is an ANSI standard for Basic Space Centering. Preliminary; package in development.

PQ 100



Top View

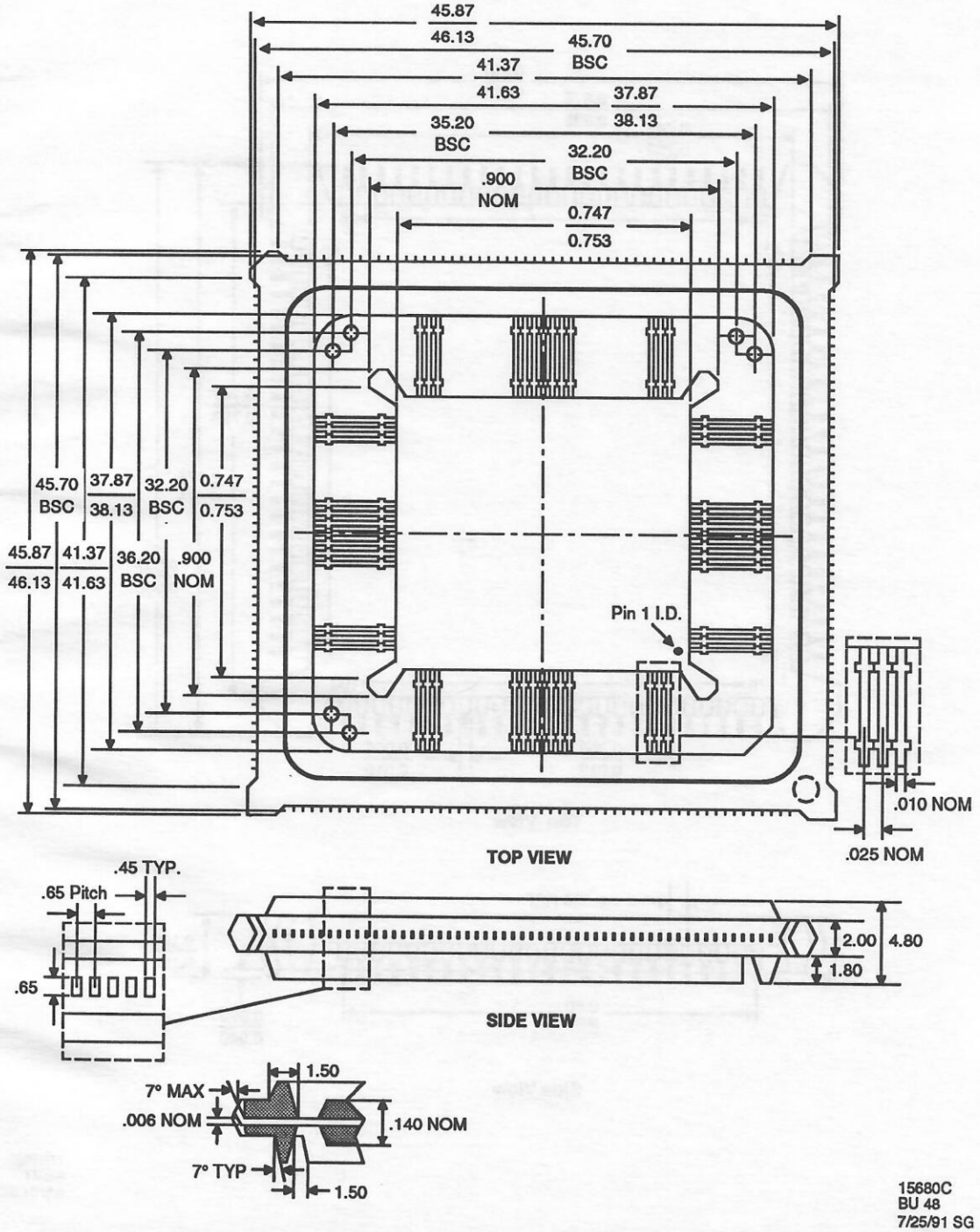


Side View

15679E
BS 41
8/5/91 SG

PHYSICAL DEMINSIONS (continued)

PQB-100
(Outer Ring measured in millimeters)



15680C
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