AMD

AMD-K6® Processor

100-MHz Bus Specification

Application Note

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Revision History

Date	Rev	Description
May 1998	E	Initial published release.
May 1999	F	Changed title and added first sentence on page 1 to reflect that the information in this document applies to both the AMD-K6®-2 and AMD-K6®-III processors.
May 1999	F	Added Figure 29, "ATX Motherboard (Partial View)," on page 46 and Figure 30, "Baby AT Motherboard (Partial View)," on page 47.
June 1999	G	Deleted "Processor Recommendations" on page 4.
June 1999	G	Added note 5 to Table 4, "Processor RESET and Configuration Signals," on page 10.

Application Note

AMD-K6® Processor 100-MHz Bus Specification

Unless otherwise noted, the information in this application note pertains only to the AMD-K6®-2 processor Model 8 and AMD-K6-III processor Model 9.

1 Super7™ Platform Initiative

AMD and its industry partners are investing in the future of Socket 7 with the new Super7™ platform initiative. The goal of the initiative is to maintain competitive vitality of the Socket 7 infrastructure through a series of planned enhancements, including the development of an industry-standard 100-MHz processor bus protocol. This document provides the AC specifications, requirements, and recommendations for a system built around the AMD-K6 processors that support a 100-MHz frontside processor bus.

In addition to the 100-MHz local bus protocol, the Super7 initiative includes the introduction of chipsets that support the accelerated graphics port (AGP) specification and includes support for a backside L2 cache and frontside L3 cache.

1.1 Super7™ Enhancements

- *100-MHz local bus*—The AMD-K6 processor Model 8 and AMD-K6-III processor Model 9 support a 100-MHz, 800-Mbyte/second frontside bus to provide a high-speed interface to Super7 platform-based chipsets. The 100-MHz

interface to the frontside level 2 (L2) cache and to the main system memory speeds up access to the frontside cache and main memory by 50-percent over the 66-MHz Socket 7 interface—a significant increase in system performance that is potentially equivalent to a jump of up to two processor speed grades.

- *Accelerated graphics port (AGP) support*—AGP improves the performance of mid-range PCs that have small amounts of video memory on the graphics card. The industry-standard AGP specification enables a 133-MHz graphics interface and can scale to even higher levels of performance.
- *Support for backside L2 and frontside L3 cache*—The Super7 platform has the potential to support higher-performance AMD-K6 processors, with clock speeds scaling to 475 MHz and beyond. The AMD-K6-III processor features a full-speed, on-chip backside 256-Kbyte L2 cache designed to deliver new levels of system performance to mainstream desktop systems. The AMD-K6-III processor also supports an optional 100-MHz frontside L3 cache for even higher performance system configurations.

1.2 Super7™ Advantages

- Delivers performance and features competitive with alternate platforms at the same clock speed and at significantly lower cost.
- Leverages existing system designs for superior value and faster time to market.
- Enables OEMs and resellers to take advantage of mature, high-volume infrastructure supported by multiple BIOS, chipset, graphics, and motherboard suppliers.
- Reduces inventory and design costs by using one motherboard for a wide range of products.
- Builds on a huge installed base of more than 100-million motherboards.
- Provides an easy upgrade path for future PC users and a bridge to legacy users.

By taking advantage of the low-cost, mature Socket 7 infrastructure, the Super7 platform continues to provide superior value and leading-edge performance for mainstream desktop systems.

2 100-MHz Bus Signal-Switching Analysis

Figure 1 illustrates the interconnection of the major components of a typical Super7 platform-based system. This document addresses those components and interfaces that run at 100 MHz, including the AMD-K6 processor, the L2 cache, the Northbridge, and the synchronous DRAM (SDRAM).

The use of an external L2 cache tag is optional and is dependent on the chipset used in the system.

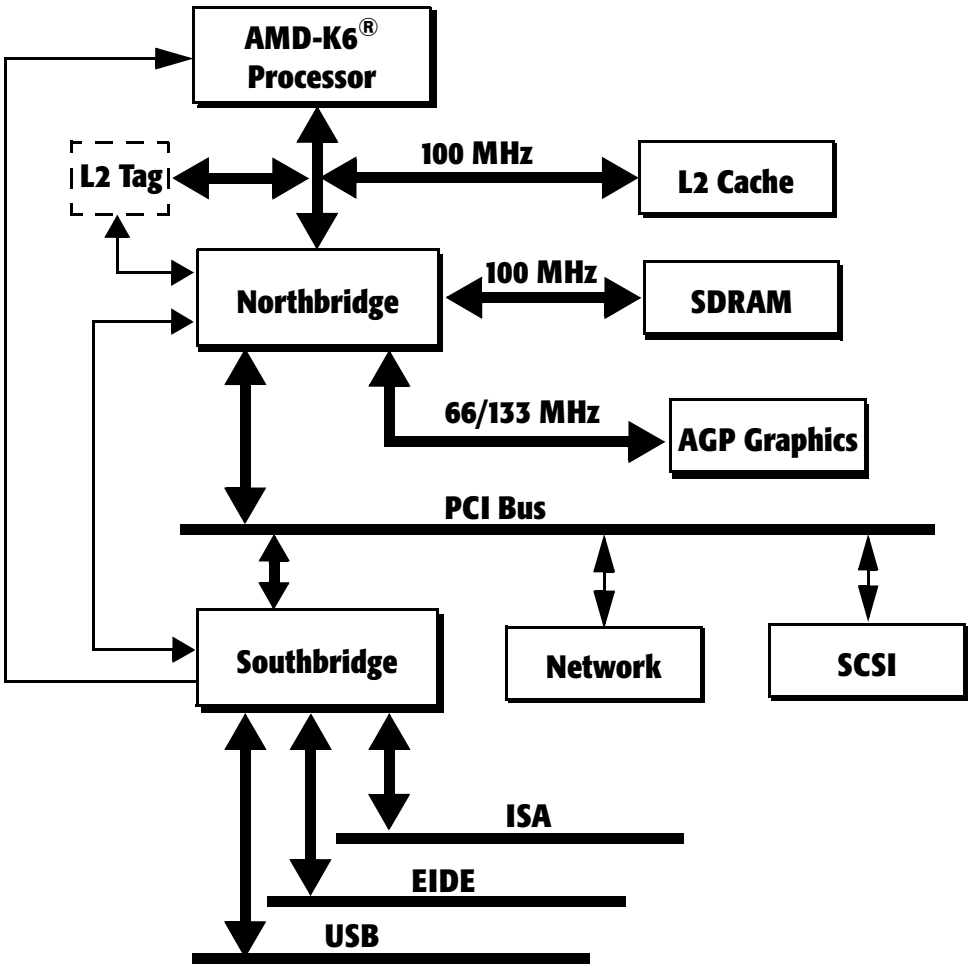


Figure 1. System Block Diagram

3 Processor Specifications

3.1 Processor AC Specifications

The 100-MHz AC specifications for the AMD-K6 processors are presented in Table 1 through Table 6 (consult the *AMD-K6®-2 Processor Data Sheet*, order# 21850, or the *AMD-K6®-III Processor Data Sheet*, order# 21918 for the latest specifications). Valid delay, float, setup, and hold timing specifications are listed. These specifications are provided for the system designer to determine if the timings necessary for the processor to interface with the system logic are met. Table 1 contains the AC specifications of the CLK input. Table 2 and Table 3 contain the timings for the normal operation signals. Table 4 contains the timings for RESET and the configuration signals. Table 5 and Table 6 contain the timings for the test operation signals.

All processor signal timings are provided as follows:

- Measured between CLK, TCK, or RESET at 1.5 V and the corresponding signal at 1.5 V—this applies to input and output signals that are switching from low to high, or from high to low.
- Based on input signals applied at a slew rate of 1 V/ns between 0 V and 3 V (rising) and 3 V to 0 V (falling).
- Valid within the normal processor operating ranges.
- Based on a load capacitance (C_L) of 0 pF.

CLK AC Specifications

Table 1 contains the AC specifications of the CLK input to the processor for 100-MHz bus operation as measured at the voltage levels indicated by Figure 2 on page 5.

The CLK period stability specifies the variance (jitter) allowed between successive periods of the CLK input measured at 1.5 V. This parameter must be considered as one of the elements of clock skew between the processor and the system logic.

Table 1. Processor CLK AC Specifications

Symbol	Parameter Description	Preliminary Data		Figure	Comments
		Min	Max		
	Frequency		100 MHz		In normal mode
t_1	CLK Period	10.0 ns		2	In normal mode
t_2	CLK High Time	3.0 ns		2	
t_3	CLK Low Time	3.0 ns		2	
t_4	CLK Fall Time	0.15 ns	1.5 ns	2	
t_5	CLK Rise Time	0.15 ns	1.5 ns	2	
	CLK Period Stability		± 250 ps		Note

Note:
Jitter frequency power spectrum peaking must occur at frequencies greater than (Frequency of CLK)/3 or less than 500 kHz.

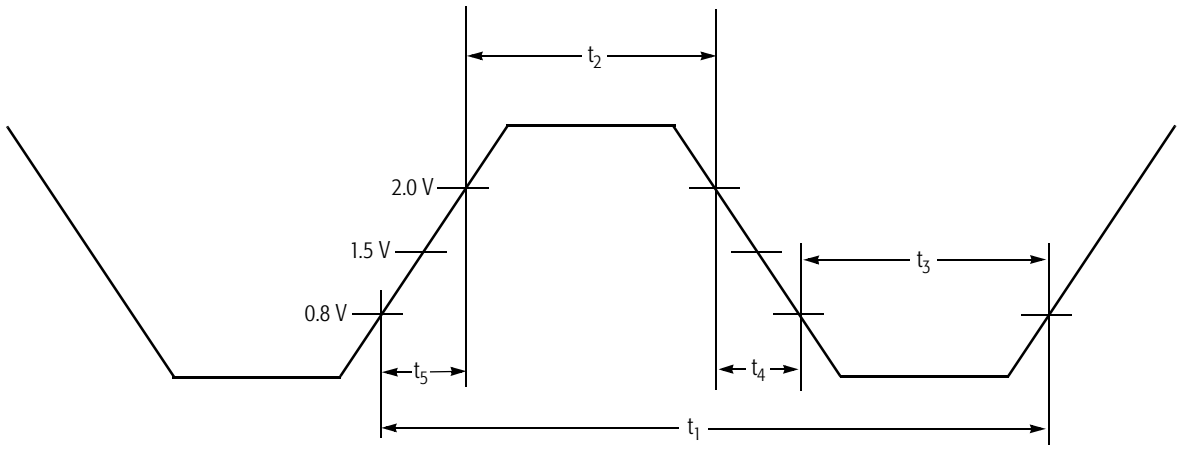


Figure 2. Processor CLK Waveform

Processor Valid Delay, Float, Setup, and Hold Timings

Valid delay and float timings are given for output signals during functional operation and are given relative to the rising edge of CLK. During boundary-scan testing, valid delay and float timings for output signals are with respect to the falling edge of TCK. The maximum valid delay timings are provided to allow a system designer to determine if setup times to the system logic can be met. Likewise, the minimum valid delay timings are used to analyze hold times to the system logic.

The setup and hold time requirements for the processor input signals must be met by the system logic to assure the proper operation. The setup and hold timings during functional and boundary-scan test mode are given relative to the rising edge of CLK and TCK, respectively.

Processor Output Delay Timings

Table 2 shows processor output delay timings.

Table 2. Processor Output Delay Timings

Symbol	Parameter Description	Preliminary Data		Figure	Comments
		Min	Max		
t_6	A[31:3] Valid Delay	1.1 ns	4.0 ns	4	
t_7	A[31:3] Float Delay		7.0 ns	5	
t_8	ADS# Valid Delay	1.0 ns	4.0 ns	4	
t_9	ADS# Float Delay		7.0 ns	5	
t_{10}	ADSC# Valid Delay	1.0 ns	4.0 ns	4	
t_{11}	ADSC# Float Delay		7.0 ns	5	
t_{12}	AP Valid Delay	1.0 ns	5.5 ns	4	
t_{13}	AP Float Delay		7.0 ns	5	
t_{14}	APCHK# Valid Delay	1.0 ns	4.5 ns	4	
t_{15}	BE[7:0]# Valid Delay	1.0 ns	4.0 ns	4	
t_{16}	BE[7:0]# Float Delay		7.0 ns	5	
t_{17}	BREQ Valid Delay	1.0 ns	4.0 ns	4	
t_{18}	CACHE# Valid Delay	1.0 ns	4.0 ns	4	
t_{19}	CACHE# Float Delay		7.0 ns	5	
t_{20}	D/C# Valid Delay	1.0 ns	4.0 ns	4	
t_{21}	D/C# Float Delay		7.0 ns	5	

Table 2. Processor Output Delay Timings (continued)

Symbol	Parameter Description	Preliminary Data		Figure	Comments
		Min	Max		
t_{22}	D[63:0] Write Data Valid Delay	1.3 ns	4.5 ns	4	
t_{23}	D[63:0] Write Data Float Delay		7.0 ns	5	
t_{24}	DP[7:0] Write Data Valid Delay	1.3 ns	4.5 ns	4	
t_{25}	DP[7:0] Write Data Float Delay		7.0 ns	5	
t_{26}	FERR# Valid Delay	1.0 ns	4.5 ns	4	
t_{27}	HIT# Valid Delay	1.0 ns	4.0 ns	4	
t_{28}	HITM# Valid Delay	1.1 ns	4.0 ns	4	
t_{29}	HLDA Valid Delay	1.0 ns	4.0 ns	4	
t_{30}	LOCK# Valid Delay	1.1 ns	4.0 ns	4	
t_{31}	LOCK# Float Delay		7.0 ns	5	
t_{32}	M/IO# Valid Delay	1.0 ns	4.0 ns	4	
t_{33}	M/IO# Float Delay		7.0 ns	5	
t_{34}	PCD Valid Delay	1.0 ns	4.0 ns	4	
t_{35}	PCD Float Delay		7.0 ns	5	
t_{36}	PCHK# Valid Delay	1.0 ns	4.5 ns	4	
t_{37}	PWT Valid Delay	1.0 ns	4.0 ns	4	
t_{38}	PWT Float Delay		7.0 ns	5	
t_{39}	SCYC Valid Delay	1.0 ns	4.0 ns	4	
t_{40}	SCYC Float Delay		7.0 ns	5	
t_{41}	SMIACT# Valid Delay	1.0 ns	4.0 ns	4	
t_{42}	W/R# Valid Delay	1.0 ns	4.0 ns	4	
t_{43}	W/R# Float Delay		7.0 ns	5	

Processor Input Setup and Hold Timings

Table 3 shows processor input setup and hold timings.

Table 3. Processor Input Setup and Hold Timings

Symbol	Parameter Description	Preliminary Data		Figure	Comments
		Min	Max		
t_{44}	A[31:5] Setup Time	3.0 ns		6	
t_{45}	A[31:5] Hold Time	1.0 ns		6	
t_{46}	A20M# Setup Time	3.0 ns		6	Note 1
t_{47}	A20M# Hold Time	1.0 ns		6	Note 1
t_{48}	AHOLD Setup Time	3.5 ns		6	
t_{49}	AHOLD Hold Time	1.0 ns		6	
t_{50}	AP Setup Time	1.7 ns		6	
t_{51}	AP Hold Time	1.0 ns		6	
t_{52}	BOFF# Setup Time	3.5 ns		6	
t_{53}	BOFF# Hold Time	1.0 ns		6	
t_{54}	BRDY# Setup Time	3.0 ns		6	
t_{55}	BRDY# Hold Time	1.0 ns		6	
t_{56}	BRDYC# Setup Time	3.0 ns		6	
t_{57}	BRDYC# Hold Time	1.0 ns		6	
t_{58}	D[63:0] Read Data Setup Time	1.7 ns		6	
t_{59}	D[63:0] Read Data Hold Time	1.5 ns		6	
t_{60}	DP[7:0] Read Data Setup Time	1.7 ns		6	
t_{61}	DP[7:0] Read Data Hold Time	1.5 ns		6	
t_{62}	EADS# Setup Time	3.0 ns		6	
t_{63}	EADS# Hold Time	1.0 ns		6	
t_{64}	EWBE# Setup Time	1.7 ns		6	
t_{65}	EWBE# Hold Time	1.0 ns		6	
t_{66}	FLUSH# Setup Time	1.7 ns		6	Note 2
t_{67}	FLUSH# Hold Time	1.0 ns		6	Note 2

Notes:

1. *These level-sensitive signals can be asserted synchronously or asynchronously. To be sampled on a specific clock edge, setup and hold times must be met. If asserted asynchronously, they must be asserted for a minimum pulse width of two clocks.*
2. *These edge-sensitive signals can be asserted synchronously or asynchronously. To be sampled on a specific clock edge, setup and hold times must be met. If asserted asynchronously, they must have been negated at least two clocks prior to assertion and must remain asserted at least two clocks.*

Table 3. Processor Input Setup and Hold Timings (continued)

Symbol	Parameter Description	Preliminary Data		Figure	Comments
		Min	Max		
t_{68}	HOLD Setup Time	1.7 ns		6	
t_{69}	HOLD Hold Time	1.5 ns		6	
t_{70}	IGNNE# Setup Time	1.7 ns		6	Note 1
t_{71}	IGNNE# Hold Time	1.0 ns		6	Note 1
t_{72}	INIT Setup Time	1.7 ns		6	Note 2
t_{73}	INIT Hold Time	1.0 ns		6	Note 2
t_{74}	INTR Setup Time	1.7 ns		6	Note 1
t_{75}	INTR Hold Time	1.0 ns		6	Note 1
t_{76}	INV Setup Time	1.7 ns		6	
t_{77}	INV Hold Time	1.0 ns		6	
t_{78}	KEN# Setup Time	3.0 ns		6	
t_{79}	KEN# Hold Time	1.0 ns		6	
t_{80}	NA# Setup Time	1.7 ns		6	
t_{81}	NA# Hold Time	1.0 ns		6	
t_{82}	NMI Setup Time	1.7 ns		6	Note 2
t_{83}	NMI Hold Time	1.0 ns		6	Note 2
t_{84}	SMI# Setup Time	1.7 ns		6	Note 2
t_{85}	SMI# Hold Time	1.0 ns		6	Note 2
t_{86}	STPCLK# Setup Time	1.7 ns		6	Note 1
t_{87}	STPCLK# Hold Time	1.0 ns		6	Note 1
t_{88}	WB/WT# Setup Time	1.7 ns		6	
t_{89}	WB/WT# Hold Time	1.0 ns		6	

Notes:

1. *These level-sensitive signals can be asserted synchronously or asynchronously. To be sampled on a specific clock edge, setup and hold times must be met. If asserted asynchronously, they must be asserted for a minimum pulse width of two clocks.*
2. *These edge-sensitive signals can be asserted synchronously or asynchronously. To be sampled on a specific clock edge, setup and hold times must be met. If asserted asynchronously, they must have been negated at least two clocks prior to assertion and must remain asserted at least two clocks.*

Processor RESET and Test Signal Timing

Table 4 shows processor RESET and configuration signals. Table 5 shows processor TCK waveform and TRST# timing at 25 MHz. Table 6 shows processor test signal timing at 25 MHz.

Table 4. Processor RESET and Configuration Signals

Symbol	Parameter Description	Preliminary Data		Figure	Comments
		Min	Max		
t_{90}	RESET Setup Time	1.7 ns		7	
t_{91}	RESET Hold Time	1.0 ns		7	
t_{92}	RESET Pulse Width, V_{CC} and CLK Stable	15 clocks		7	
t_{93}	RESET Active After V_{CC} and CLK Stable	1.0 ms		7	
t_{94}	BF[2:0] Setup Time	1.0 ms		7	Note 3
t_{95}	BF[2:0] Hold Time	2 clocks		7	Note 3
t_{96}	BRDYC# Hold Time	1.0 ns		7	Note 4, 5
t_{97}	BRDYC# Setup Time	2 clocks		7	Note 2, 5
t_{98}	BRDYC# Hold Time	2 clocks		7	Note 2, 5
t_{99}	FLUSH# Setup Time	1.7 ns		7	Note 1
t_{100}	FLUSH# Hold Time	1.0 ns		7	Note 1
t_{101}	FLUSH# Setup Time	2 clocks		7	Note 2
t_{102}	FLUSH# Hold Time	2 clocks		7	Note 2

Notes:

1. *To be sampled on a specific clock edge, setup and hold times must be met the clock edge before the clock edge on which RESET is sampled negated.*
2. *If asserted asynchronously, these signals must meet a minimum setup and hold time of two clocks relative to the negation of RESET.*
3. *BF[2:0] must meet a minimum setup time of 1.0 ms and a minimum hold time of two clocks relative to the negation of RESET.*
4. *If RESET is driven synchronously, BRDYC# must meet the specified hold time relative to the negation of RESET.*
5. *This specification applies only to the AMD-K6-2 processor Model 8, and not to the AMD-K6-III processor Model 9.*

Table 5. Processor TCK Waveform and TRST# Timing at 25 MHz

Symbol	Parameter Description	Preliminary Data		Figure	Comments
		Min	Max		
	TCK Frequency		25 MHz	8	
t_{103}	TCK Period	40.0 ns		8	
t_{104}	TCK High Time	14.0 ns		8	
t_{105}	TCK Low Time	14.0 ns		8	
t_{106}	TCK Fall Time		5.0 ns	8	Note 1, 2
t_{107}	TCK Rise Time		5.0 ns	8	Note 1, 2
t_{108}	TRST# Pulse Width	30.0 ns		9	Asynchronous

Notes:

1. *Rise/fall times can be increased by 1.0 ns for each 10 MHz that TCK is run below its maximum frequency of 25 MHz.*
2. *Rise/fall times are measured between 0.8 V and 2.0 V.*

Table 6. Processor Test Signal Timing at 25 MHz

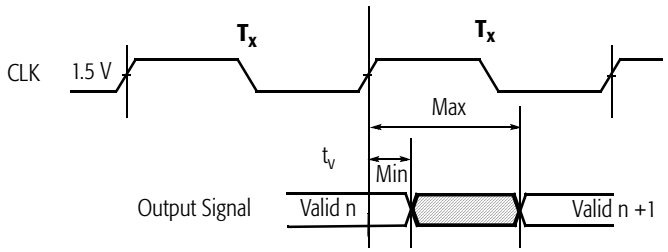
Symbol	Parameter Description	Preliminary Data		Figure	Notes
		Min	Max		
t_{109}	TDI Setup Time	5.0 ns		10	Note 2
t_{110}	TDI Hold Time	9.0 ns		10	Note 2
t_{111}	TMS Setup Time	5.0 ns		10	Note 2
t_{112}	TMS Hold Time	9.0 ns		10	Note 2
t_{113}	TDO Valid Delay	3.0 ns	13.0 ns	10	Note 1
t_{114}	TDO Float Delay		16.0 ns	10	Note 1
t_{115}	All Outputs (Non-Test) Valid Delay	3.0 ns	13.0 ns	10	Note 1
t_{116}	All Outputs (Non-Test) Float Delay		16.0 ns	10	Note 1
t_{117}	All Inputs (Non-Test) Setup Time	5.0 ns		10	Note 2
t_{118}	All Inputs (Non-Test) Hold Time	9.0 ns		10	Note 2

Notes:

1. *Parameter is measured from the TCK falling edge.*
2. *Parameter is measured from the TCK rising edge.*

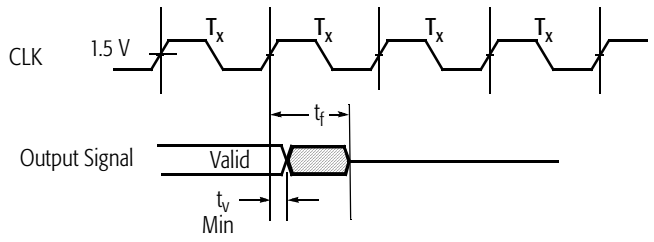
WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Steady
	Can change from high to low	Changing from high to low
	Can change from low to high	Changing from low to high
	Don't care, any change permitted	Changing, state unknown
	(Does not apply)	Center line is high-impedance state

Figure 3. Diagrams Key



v = 6, 8, 10, 12, 14, 15, 17, 18, 20, 22, 24, 26, 27, 28, 29, 30, 32, 34, 36, 37, 39, 41, 42

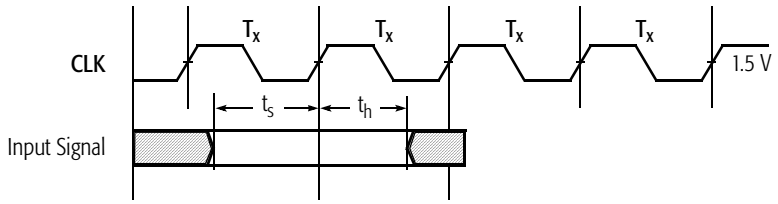
Figure 4. Processor Output Valid Delay Timing



v = 6, 8, 10, 12, 15, 18, 20, 22, 24, 30, 32, 34, 37, 39, 42

f = 7, 9, 11, 13, 16, 19, 21, 23, 25, 31, 33, 35, 38, 40, 43

Figure 5. Maximum Processor Float Delay Timing



s = 44, 46, 48, 50, 52, 54, 56, 58, 60, 62, 64, 66, 68, 70, 72, 74, 76, 78, 80, 82, 84, 86, 88

h = 45, 47, 49, 51, 53, 55, 57, 59, 61, 63, 65, 67, 69, 71, 73, 75, 77, 79, 81, 83, 85, 87, 89

Figure 6. Processor Input Setup and Hold Timing

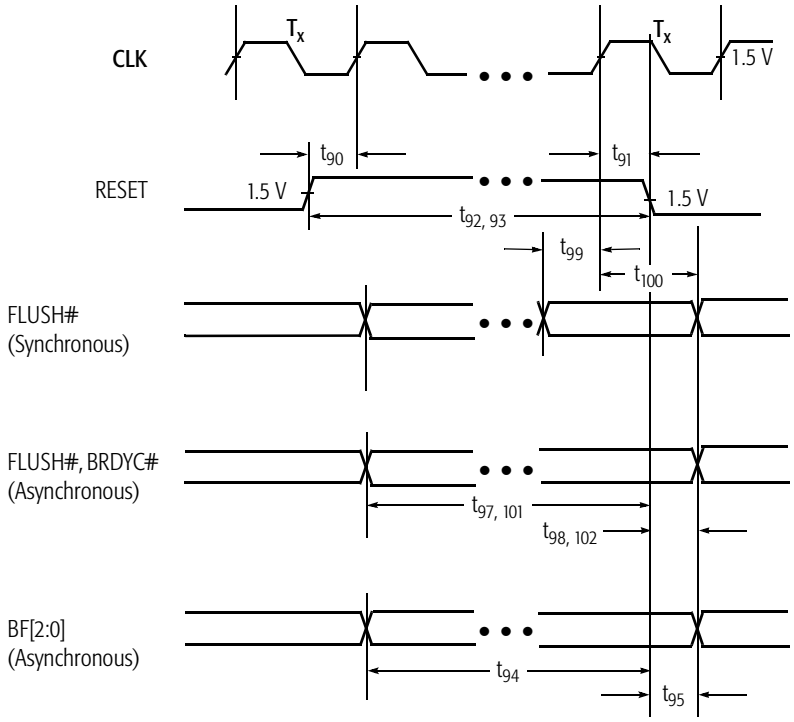


Figure 7. Processor Reset and Configuration Timing

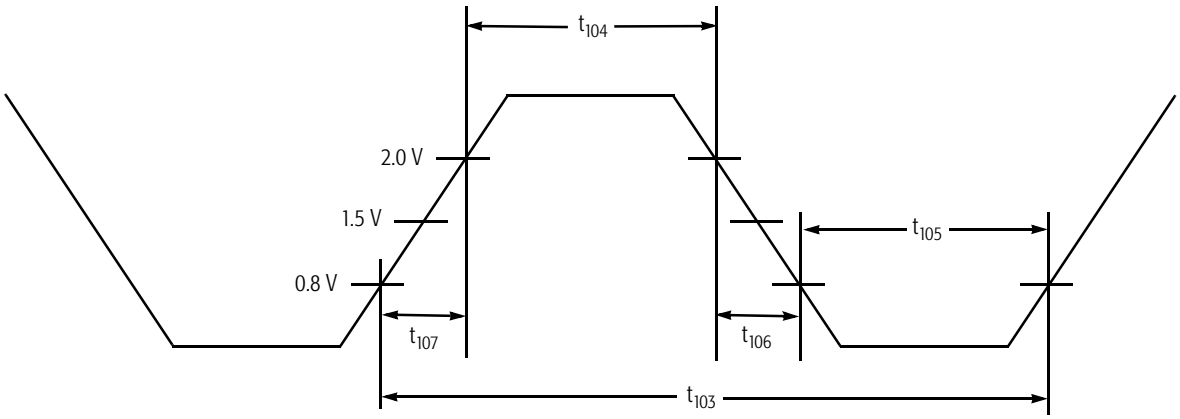


Figure 8. Processor TCK Waveform

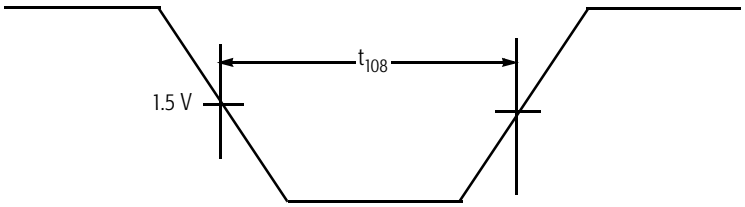


Figure 9. Processor TRST# Timing

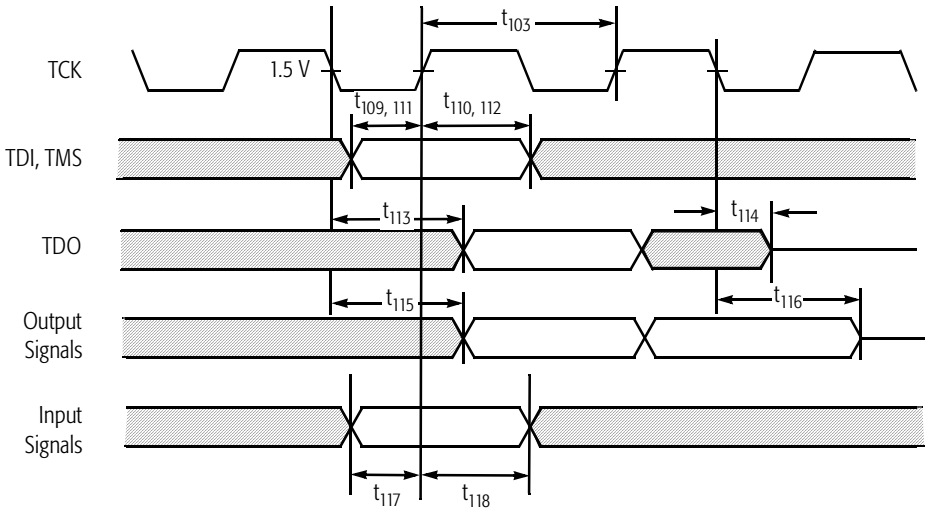


Figure 10. Processor Test Signal Timing Diagram

3.2 Processor DC Specifications

The DC characteristics of the AMD-K6 processor I/O buffers are shown in Table 7.

Table 7. DC Specifications

Symbol	Parameter Description	Preliminary Data		Comments
		Min	Max	
V_{IL}	Input Low Voltage	–0.3 V	+0.8 V	
V_{IH}	Input High Voltage	2.0 V	V_{CC3}+0.3 V	Note 1
V_{OL}	Output Low Voltage		0.4 V	I_{OL} = 4.0-mA load
V_{OH}	Output High Voltage	2.4 V		I_{OH} = 3.0-mA load
I_{LI}	Input Leakage Current		±15 µA	Note 2
I_{LO}	Output Leakage Current		±15 µA	Note 2
I_{IL}	Input Leakage Current Bias with Pullup		–400 µA	Note 3
I_{IH}	Input Leakage Current Bias with Pulldown		200 µA	Note 4
C_{IN}	Input Capacitance		15 pF	
C_{OUT}	Output Capacitance		20 pF	
C_{OUT}	I/O Capacitance		25 pF	
C_{CLK}	CLK Capacitance		15 pF	
C_{TIN}	Test Input Capacitance (TDI, TMS, TRST#)		15 pF	
C_{TOUT}	Test Output Capacitance (TDO)		20 pF	
C_{TCK}	TCK Capacitance		15 pF	

Notes:

1. *V_{CC3} refers to the voltage being applied to V_{CC3} during functional operation.*
2. *Refers to inputs and I/O without an internal pullup resistor and $0 \leq V_{IN} \leq V_{CC3}$.*
3. *Refers to inputs with an internal pullup and V_{IL} = 0.4 V.*
4. *Refers to inputs with an internal pulldown and V_{IH} = 2.4 V.*

4 Clock Chip Specifications

4.1 Clock Chip Requirements

In order to meet the timings of a 100-MHz system, the following requirements must be met by the clock chip:

- The clock chip meets the AC specifications as defined in "CLK AC Specifications" on page 4.
- The skew between the 100-MHz clock output pins of the clock chip must not exceed 250 ps.
- The edge-to-edge jitter of each 100-MHz clock output pin must not exceed 250 ps.

5 Chipset Specifications

5.1 Chipset Requirements

Timing

In this document, if a signal is launched off a clock edge and must be sampled at its destination on the next clock edge, then the cycle time or path length for this signal is defined as one clock. Likewise, if a signal is launched off a clock edge and must be sampled at its destination two clock edges later, then the path length for this signal is defined as two clocks.

In order to meet the timings of a 100-MHz system, the following requirements must be met by the chipset:

- The chipset meets the AC specifications as defined in "Chipset AC Specifications" on page 19.
- The Northbridge meets the DC specifications as defined in "Northbridge I/O Buffer Specifications" on page 29.
- The cycle time for the following paths is two clocks (20.0 ns):
  - Processor address bus (A[31:3]) to the Northbridge for processor bus cycles (for chipsets with an integrated L2 cache tag)
  - Processor address bus (A[31:3]) to the L2 cache tag, and then L2 cache tag address (TA) to the Northbridge for processor bus cycles (for chipsets with an external L2 cache tag)
  - Northbridge memory address (MA) to SDRAM for memory accesses
- The cycle time for the following paths is two clocks (20.0 ns) or greater:
  - Northbridge address bus (A[31:3]) to processor for inquire cycles
  - Northbridge address bus (A[31:3]) to the pipelined burst SRAM (PBSRAM) chips (L2 cache) for inquire cycles

Performance

The chipset must implement the following L2 cache and memory cycle lengths in order to achieve optimal performance at 100 MHz:

- L2 burst read cycle of 3-1-1-1
- Minimum memory burst read cycle of 8-1-1-1

5.2 Chipset Recommendations

In order to meet the timings of a 100-MHz system, the following recommendations should be considered with respect to the chipset:

- In order to optimize performance, the L2 cache tag and the Northbridge should be designed to support a front-side L2 cache size of at least 512 Kbytes.
- For those chipsets that require an external L2 cache tag, the L2 cache should be implemented using a single PBSRAM chip in order to minimize the loading on the host address bus.
- Minimize the number of one-clock paths in order to increase the timing margin of the system. If possible, the following processor-to-Northbridge paths should be investigated to determine if their path lengths can be two clocks (20.0 ns) or greater:

  - BE[7:0]#
  - CACHE#
  - LOCK#
  - M/IO#
  - HITM#
  - SMIACT#
  - D/C#
  - W/R#

- In order to minimize the number of one-clock paths between the Southbridge and the processor, the signals that are listed in Table 12, "Southbridge Processor Interface Signals," on page 28, can be asserted asynchronously.

5.3 Chipset AC Specifications

The 100-MHz target AC specifications for the chipset are presented in Table 8 through Table 10. These timings are derived based on the following:

- The specifications defined in "Processor AC Specifications" on page 4.
- The requirements described in "Clock Chip Requirements" on page 17.
- The requirements described in "Chipset Requirements" on page 18.

- A maximum skew of 500 ps between the 100-MHz clocks that source the processor, the chipset, and the PBSRAM chip(s), due to the following:
  - Maximum clock skew of 250 ps at the output pins of the clock chip
  - Maximum clock skew of 250 ps due to the differences associated with the clock trace lengths

Note: *The skew requirement for the SDRAM 100-MHz clocks is dependent on the clocking scheme implemented for the SDRAM interface.*

- A maximum edge-to-edge jitter of 250 ps for each 100-MHz clock
- A clock period of 10.0 ns (unless noted otherwise)
- A worst-case propagation delay of 1.75 ns for point-to-point traces (sometimes referred to as 2-load or 2-drop traces)
- A best-case propagation delay of 1.25 ns for point-to-point and multidrop traces
- A worst-case propagation delay of 2.5 ns for all multidrop traces
- A target of achieving a timing margin of at least 0 ns using a worst-case analysis for setup times and a best-case analysis for hold times
- ADSC# routed point-to-point to the Northbridge and ADS# routed to the PBSRAM chip(s)
- An L2 cache comprised of one (if the L2 tag is external to the chipset) or two (if the L2 tag is integrated in the chipset) PBSRAM chips with the following AC timings:
  - Maximum data valid delay of 5.0 ns
  - Minimum data valid delay of 1.50 ns
  - Minimum setup time of 2.2 ns for data and control signals
  - Minimum hold time of 1.0 ns for data and control signals

Note: *The access time of the L2 cache tag static RAM (SRAM) is dependent on several factors. Refer to Table 11 on page 26 for a list of tag access requirements relative to propagation delays and Northbridge setup times.*

- Main memory comprised of synchronous DRAM (SDRAM) DIMMs with the following AC timings:
  - Maximum data valid delay of 7.0 ns
  - Minimum data valid delay of 3.0 ns
  - Minimum setup time of 3.0 ns for data and control signals
  - Minimum hold time of 1.0 ns for data and control signals

Note: *The number of SDRAM DIMMs is variable and must be considered when analyzing the Northbridge SDRAM interface.*

All chipset signal timings are provided as follows:

- Measured between CLK at 1.5 V and the corresponding signal at 1.5 V—this applies to input and output signals that are switching from low to high, or from high to low
- Valid within the normal chipset operating ranges
- Based on a load capacitance (C_L) of 0 pF

The Northbridge and Southbridge AC specifications provided are for those signals that are typically supported by chipsets that support a single processor. The available timing budget that is available for a signal that is omitted from Table 8 through Table 10 can easily be derived by using the processor specifications along with the assumptions given in this document for propagation delays, clock skew, and clock jitter. For example, the following analysis can be used to determine the maximum allowable valid delay for a signal sourced by the Northbridge and sampled by the processor:

$$T_{nb\_max\_valid} = (T_{cycle} - T_{cpu\_min\_setup} - T_{propmax} - T_{skew} - T_{jitter})$$

Therefore, if:

T_{cycle} = 10.0 ns,

$T_{cpu\_min\_setup}$ = 3.5 ns,

$T_{propmax}$ = 1.75 ns,

T_{skew} = 0.5 ns,

T_{jitter} = 0.25 ns

then, $T_{nb\_max\_valid}$ = (10.0 – 3.5 – 1.75 – 0.5 – 0.25) = 4.0 ns

Similarly, the following analysis can be used to determine the minimum valid delay for a signal sourced by the Northbridge and sampled by the processor:

$T_{nb\_min\_valid} = T_{cpu\_min\_hold} - T_{propmin} + T_{skew} + T_{jitter}$

Therefore, if:

$T_{cpu\_min\_hold} = 1.0$ ns,

$T_{propmin} = 1.25$ ns,

$T_{skew} = 0.5$ ns,

$T_{jitter} = 0.25$ ns,

then, $T_{nb\_min\_valid} = (1.0 - 1.25 + 0.5 + 0.25) = 0.5$ ns

Note: *The minimum output delay timings provided in Table 8 on page 23 and Table 10 on page 25 have been rounded up to 1.0 ns to increase the timing margin.*

5.4 Northbridge Processor Interface Target AC Specifications

Table 8 and Table 9 contain AC specifications for the Northbridge signals that interface to the processor.

Table 8. Northbridge Processor Interface Output Delay Timings

Parameter Description	Preliminary Data		Comments
	Min	Max	
A[31:3] Valid Delay	1.0 ns	13.7 ns	Note 1
A[31:3] Float Delay		7.0 ns	
AHOLD Valid Delay	1.0 ns	4.0 ns	
BOFF# Valid Delay	1.0 ns	4.0 ns	
BRDY# Valid Delay	1.0 ns	4.5 ns	
D[63:0] Valid Delay	1.2 ns	4.5 ns	Note 2
D[63:0] Float Delay		7.0 ns	
EADS# Valid Delay	1.0 ns	4.5 ns	
INV Valid Delay	1.0 ns	3.7 ns	
KEN# Valid Delay	1.0 ns	3.7 ns	
NA# Valid Delay	1.0 ns	5.8 ns	

Notes:

1. *The maximum valid delay assumes that A[31:3] is sampled by the processor two clock edges after the clock edge that drives A[31:3]. That is, EADS# is asserted by the Northbridge one clock edge after the clock edge that drives A[31:3] during an inquire cycle. If A[31:3] is driven off the same clock that asserts EADS#, then subtract 10.0 ns from this specification. The maximum valid delay assumes that the Northbridge address bus-to-processor path is more critical than the Northbridge address bus-to-PBSRAM path.*
2. *The maximum valid delay is based on the Northbridge data bus-to-PBSRAM path (during processor read cycles) being more critical than the Northbridge data bus-to-processor path.*

Table 9. Northbridge Processor Interface Input Setup/Hold Timings

Parameter Description	Preliminary Data		Comments
	Min	Max	
A[31:3] Setup Time	12.7 ns		Note 1
A[31:3] Hold Time	1.0 ns		
ADS# Setup Time	3.5 ns		Note 2
ADS# Hold Time	1.0 ns		
BE[7:0]# Setup Time	12.7 ns		Note 1
BE[7:0]# Hold Time	1.0 ns		
CACHE# Setup Time	13.5 ns		Note 1
CACHE# Hold Time	1.0 ns		
D/C# Setup Time	3.5 ns		
D/C# Hold Time	1.0 ns		
D[63:0] Setup Time	1.7 ns		Note 3
D[63:0] Hold Time	1.0 ns		
HITM# Setup Time	13.5 ns		Note 4
HITM# Hold Time	1.0 ns		
LOCK# Setup Time	3.5 ns		
LOCK# Hold Time	1.0 ns		
M/IO# Setup Time	3.5 ns		
M/IO# Hold Time	1.0 ns		
SMIACT# Setup Time	13.5 ns		Note 4
SMIACT# Hold Time	1.0 ns		
W/R# Setup Time	3.5 ns		
W/R# Hold Time	1.0 ns		

Notes:

1. *The setup time is relative to the clock edge after the clock edge that negates ADS#. If this signal is sampled on the clock that negates ADS#, then subtract 10.0 ns from this specification.*
2. *This specification assumes that ADSC# is routed point-to-point to the Northbridge and ADS# is routed to each of the two PBSRAM chips.*
3. *This specification is based on the PBSRAM data bus-to-Northbridge path (during writeback cycles) being more critical than the processor data bus-to-Northbridge path.*
4. *This specification assumes a cycle time of two clocks.*

5.5 Northbridge PBSRAM and L2 Tag SRAM Target AC Specifications

Table 10 contains the AC specifications for the Northbridge output control signals that interface to the PBSRAM chip(s) (L2 cache).

Table 10. Northbridge PBSRAM Output Delay Timings

Parameter Description	Preliminary Data		Comments
	Min	Max	
BWE# Valid Delay	1.0 ns	4.5 ns	
CADS# Valid Delay	1.0 ns	4.5 ns	
CADV Valid Delay	1.0 ns	4.5 ns	
CE1# Valid Delay	1.0 ns	4.5 ns	
COE# Valid Delay	1.0 ns	4.5 ns	
GWE# Valid Delay	1.0 ns	4.5 ns	

Table 11 contains a list of Northbridge tag address setup time requirements relative to various tag access times and propagation delays for those chipsets that require an external L2 tag SRAM.

The headings in Table 11 are defined as follows:

- *A[31:3] Valid Delay*—The maximum output valid delay of the processor address bus
- *A[31:3] to Tag Delay*—The maximum propagation delay of the processor address bus to the input of the L2 tag SRAM
- *Tag Access*—The maximum access time of the L2 tag SRAM
- *TA to Northbridge Delay*—The maximum propagation delay of the tag address output of the L2 tag SRAM to the input of the Northbridge
- *CLK Skew/Jitter*—The sum of the maximum clock skew at the output pins of the clock generator (250 ps), the maximum clock skew due to clock trace length differences (250 ps), and the maximum clock edge-to-edge jitter (250 ps)
- *Northbridge TA Setup Time*—The minimum setup time required for the tag address into the Northbridge

Minimum Setup Time

The minimum setup time required for the tag address into the Northbridge is calculated by subtracting the sum of all of the timing elements in the first five columns in Table 11 from the cycle time of this particular path (20.0 ns). For example, the minimum Northbridge TA setup time of 6.0 ns in the first row of Table 11 is calculated by subtracting 14.0 ns (4.0 + 2.5 + 5.0 + 1.75 + 0.75) from 20.0 ns.

The propagation delays for the processor address to the L2 tag SRAM, and for TA to the Northbridge, are dependent on the location of the tag and the corresponding trace lengths.

Table 11. Northbridge Tag Address (TA) Setup Times

A[31:3] Valid Delay	A[31:3] to Tag Delay	Tag Access	TA to Northbridge Delay	CLK Skew/Jitter	Northbridge TA Setup Time	Comment
4.0 ns	2.5 ns	5.0 ns	1.75 ns	0.75 ns	6.0 ns	
4.0 ns	2.5 ns	6.0 ns	1.75 ns	0.75 ns	5.0 ns	
4.0 ns	2.5 ns	7.0 ns	1.75 ns	0.75 ns	4.0 ns	
4.0 ns	2.5 ns	8.0 ns	1.75 ns	0.75 ns	3.0 ns	

5.6 Northbridge SDRAM Interface Target AC Specifications

The interface between the Northbridge and the SDRAM DIMM modules requires special consideration due to several reasons:

1. The trace loading is relatively heavy because control signals and data are routed to multiple DIMM sockets, and in some cases, these traces are routed to multiple SDRAM components on a DIMM.
2. The trace loading is variable because the number of DIMM sockets supported on the motherboard varies from board to board. In addition, the number of SDRAM components on a DIMM module varies among DIMM vendors.
3. With the exception of the memory address (MA) path from the Northbridge to the DIMM modules, all path lengths are one clock. Meeting the setup time required by the Northbridge within a single clock is particularly difficult when considering the data access time of state-of-the-art SDRAM technology is approximately 6.0 to 7.0 ns.
4. The DIMM sockets represent an impedance discontinuity in the trace, which can adversely affect signal quality and, therefore, timing integrity.

Because of the challenges associated with meeting the timings on the Northbridge to DIMM socket interface, a different approach to the traditional clocking scheme must be considered. For example, if the analysis that has been used throughout this specification is applied to the DIMM data-to-Northbridge path for memory read cycles from a 7.0 ns DIMM module, then the sum of the SDRAM access time and the maximum system delay is greater than the 10.0 ns period of the 100-MHz clock (7.0 ns plus 3.25 ns equals 10.25 ns). Furthermore, when considering the setup time of the Northbridge, the path would yield a negative timing margin of approximately 2.0 ns.

The specific implementation of the SDRAM clocking scheme is dependent upon the specific Northbridge being used in the application. Refer to the design application notes provided by the Northbridge vendor for specific details on their particular clocking scheme implementation and corresponding timing analysis.

5.7 Southbridge Processor Interface Target AC Specifications

The signals in Table 12 are inputs to the processor. If they are asserted synchronously, they must meet the setup and hold time requirements as specified in Table 3, "Processor Input Setup and Hold Timings," on page 8. If they are asserted asynchronously, then their assertion requirements depend on whether the signal is sampled as a level-sensitive signal or an edge-sensitive signal. Level-sensitive signals must be asserted for a minimum pulse width of two clocks. Edge-sensitive signals must have been negated at least two clocks prior to assertion and must remain asserted at least two clocks.

Table 12 defines the signal type for each Southbridge processor interface signal.

Table 12. Southbridge Processor Interface Signals

Name	Type	Note
A20M#	Level-sensitive	
FLUSH#	Edge-sensitive	
IGNNE#	Level-sensitive	
INIT	Edge-sensitive	
INTR	Level-sensitive	
NMI	Edge-sensitive	
RESET	Asynchronous	Note
SMI#	Edge-sensitive	
STPCLK#	Level-sensitive	

Note:
During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification before it is negated. During a warm reset, while CLK and V_{CC} are within their specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

5.8 Northbridge I/O Buffer Specifications

All of the signal integrity simulations and subsequent timing analysis performed to generate the recommended topologies and routing guidelines provided in "Geometrical Routing Rules" on page 33 were based on host bus Northbridge I/O buffers that adhere to the specifications provided in this section.

A chipset vendor designing a Northbridge to interface to the processor at 100 MHz is encouraged to use host bus I/O buffers that meet the characteristics described in this section as closely as possible.

5.9 Voltage Versus Current (V/I) Curves

Pulldown V/I Curves

Figure 11 illustrates the minimum, typical, and maximum V/I characteristics of the pulldown structure of the Northbridge I/O buffer.

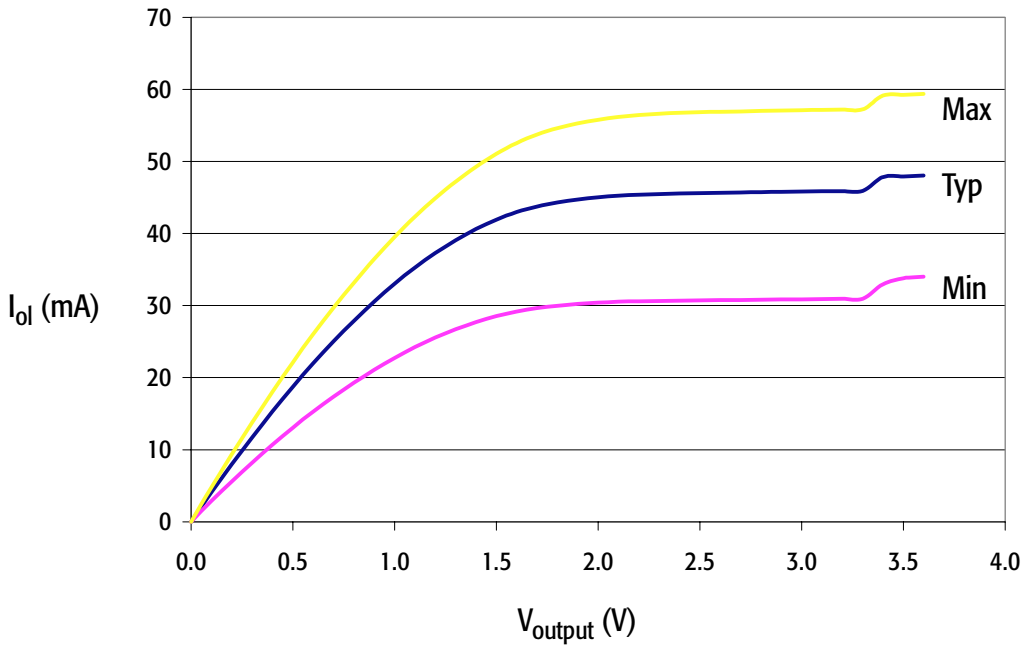


Figure 11. Northbridge Pulldown V/I Curves

Pullup V/I Curves

Figure 12 illustrates the minimum, typical, and maximum V/I characteristics of the pullup structure of the Northbridge I/O buffer.

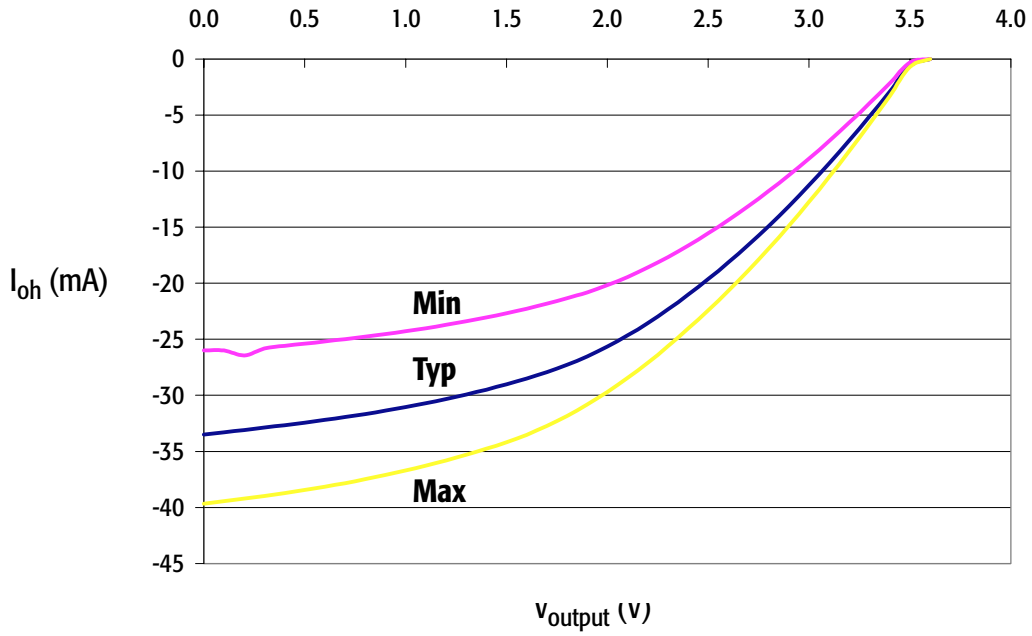


Figure 12. Northbridge Pullup V/I Curves

Rise and Fall Times

The minimum, typical, and maximum rise and fall times of the Northbridge I/O buffer are provided in Table 13. These times are specified in the manner defined by the *I/O Buffer Information Specification (IBIS)*, Version 2.1, which requires that they be expressed as the voltage swing from 20% to 80% of the final value, divided by the time it takes for the signal to transition through this voltage swing. The rise time ratios are not reduced, but are expressed as a ratio in order to remain consistent with the IBIS specification.

Table 13. Northbridge I/O Buffer Rise and Fall Times

Parameter	Minimum	Typical	Maximum	Comment
Rise Time	0.66 V / 0.37 ns	0.85 V / 0.31 ns	1.00 V / 0.28 ns	Note
Fall Time	0.60 V / 0.36 ns	0.91 V / 0.34 ns	1.13 V / 0.31 ns	Note

Note:
These specifications assume that the I/O buffer is driving a 50 ohm load.

6 Motherboard Specifications

The following sections list the motherboard requirements.

6.1 Geometrical Printed Circuit Board Fabrication Rules

Assumptions

- 4-layer board with microstrip traces (refer to Figure 13)
- FR4 core and PREPREG with a dielectric constant of 4.5

Trace and Space

- The trace width (**w**) must be greater than or equal to 0.006 inches
- The space (**s**) between traces must be greater than or equal to 0.009 inches

Stackup

- Distance (**h**) between layer 1 and layer 2 must be less than or equal to 0.008 inches
- Distance (**h**) between layer 3 and layer 4 must be less than or equal to 0.008 inches

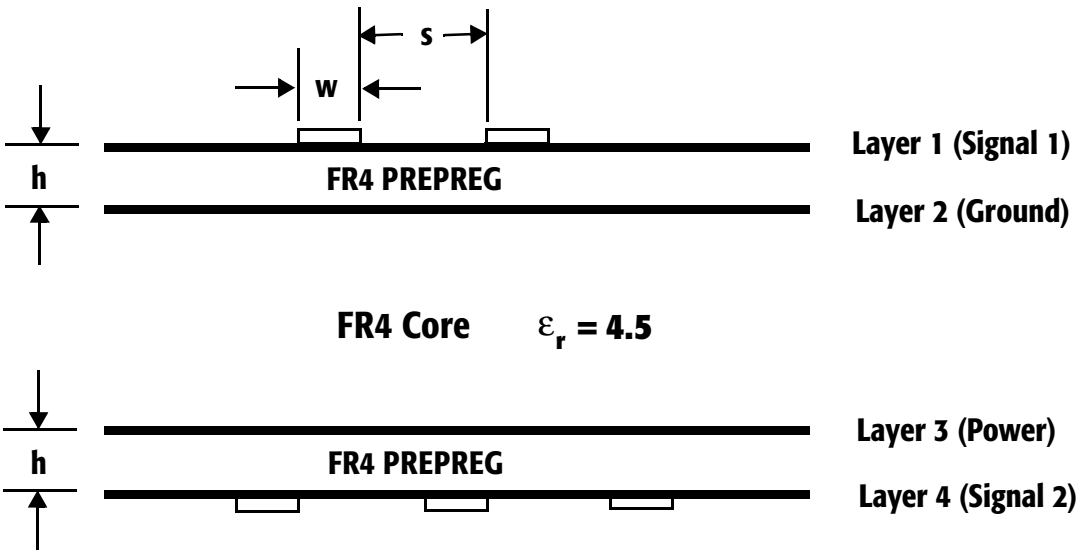


Figure 13. 4-Layer Board Stackup

6.2 Geometrical Routing Rules

Topology

- The recommended topology for systems that use a chipset with an integrated L2 cache tag is illustrated in Figure 14, where the processor and the Northbridge are placed at the ends of a daisy chain connection, and each 32-bit PBSRAM chip (L2 cache) is in the middle of the daisy chain.
- The recommended topology for systems that use a chipset that requires an external L2 cache tag is illustrated in Figure 15, where the processor and the Northbridge are placed at the ends of a daisy chain connection, and a single 64-bit PBSRAM chip (L2 cache) along with the tag SRAM is in the middle of the daisy chain.

Note: *The L2 cache is implemented using a single PBSRAM chip in order to limit the total number of loads on the host address bus to four.*

- In some cases, to allow for routing flexibility, alternate topologies for specific host bus signals are provided.
- All of the topology and routing guidelines provided hereafter assume the Northbridge I/O buffers are designed in accordance with the specifications provided in "Northbridge I/O Buffer Specifications" on page 29.

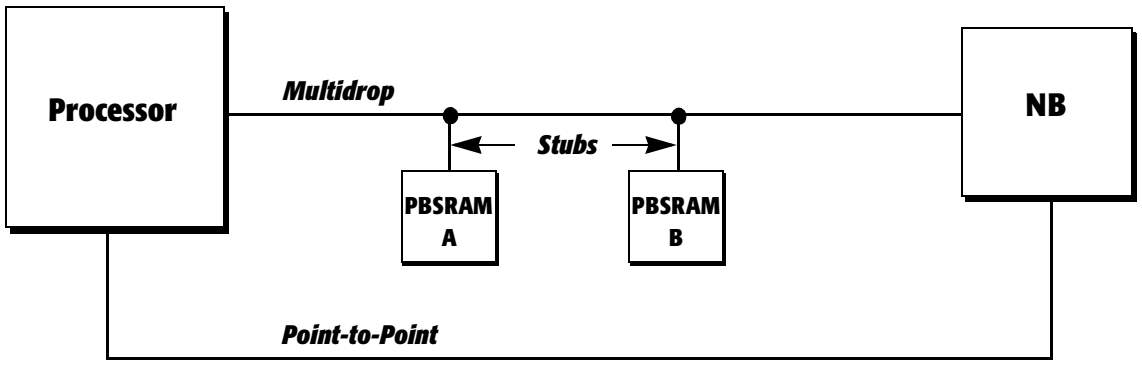


Figure 14. Recommended Host Bus Topology, Integrated L2 Cache Tag

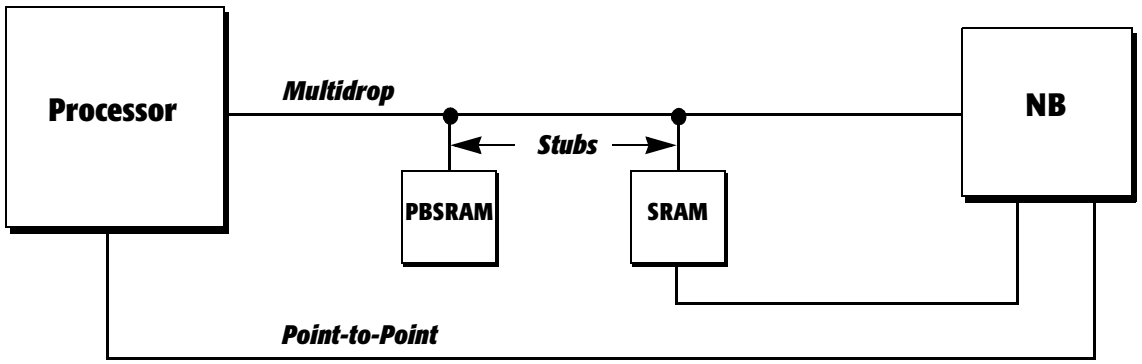


Figure 15. Recommended Host Bus Topology, External L2 Cache Tag

Trace Length

The trace length requirements defined in this section are chosen based on a compromise between signal integrity, positive timing margin, and routing feasibility. In some particular cases, routing trade-offs are provided in the event the recommended trace length requirements cannot be met due to routing limitations associated with a particular design—such as the board form factor or the pinout of the chipset. The trade-offs have been chosen to allow routing flexibility while ensuring that positive timing margin is maintained.

Note: *The following guidelines are based on extensive signal integrity and timing analysis simulations and are based on the stated assumptions provided in this document. Alternate topologies and/or trace length guidelines not specifically provided by AMD can be acceptable for 100-MHz operation. AMD recommends that any such alternate guidelines adopted by a motherboard designer be thoroughly analyzed by running the appropriate signal integrity simulations to ensure proper operation at 100 MHz.*

6.3 Host Data Bus

The topology recommendations for the host data bus are more flexible than the general topology recommendation provided in "Topology" on page 33. There are three different topologies offered in this section.

Option 1—The preferred topology recommended for the host data bus is a daisy chain topology with the processor and the Northbridge at each end of the daisy chain, and each PBSRAM chip located in the middle of the daisy chain, as illustrated in Figure 16.

- The trace length between the processor and each PBSRAM chip must be 1.5 inches or less.
- The trace length between each PBSRAM chip and the Northbridge must be 4.5 inches or less.
- The total trace length between the processor and the Northbridge must be 6.0 inches or less.
- The stub to each PBSRAM chip must be 0.5 inch or less.

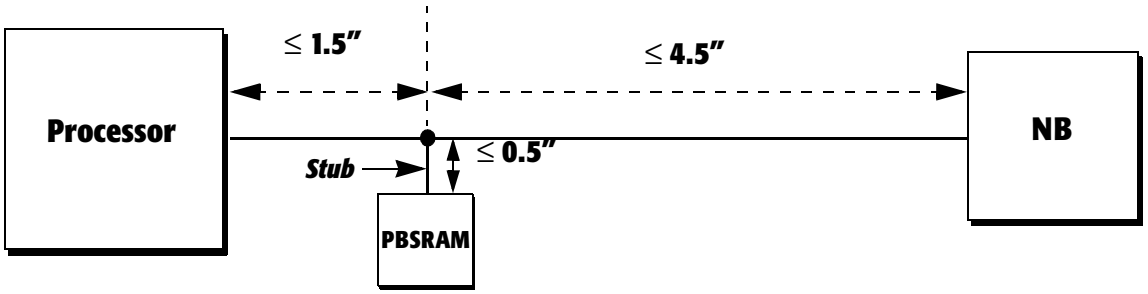


Figure 16. Host Data Bus Routing, Daisy Chain Option 1

Option 2—Another acceptable topology for the host data bus is a daisy chain topology with each PBSRAM chip and the Northbridge at each end of the daisy chain, and the processor in the middle of the daisy chain, as illustrated in Figure 17.

- The trace length between each PBSRAM chip and the processor must be 1.5 inches or less.
- The trace length between the processor and the Northbridge must be 4.5 inches or less.

- The total trace length between each PBSRAM chip and the Northbridge must be 6.0 inches or less.
- The stub to the processor must be 0.5 inch or less.

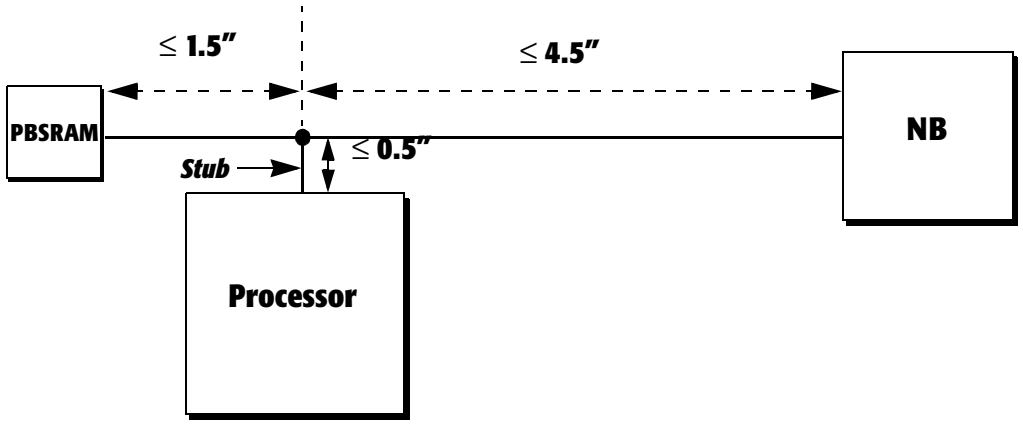


Figure 17. Host Data Bus Routing, Daisy Chain Option 2

Option 3—The third acceptable topology for the host data bus is a star topology as illustrated in Figure 18.

- The total trace length (x+y+z) must be 4.5 inches or less.

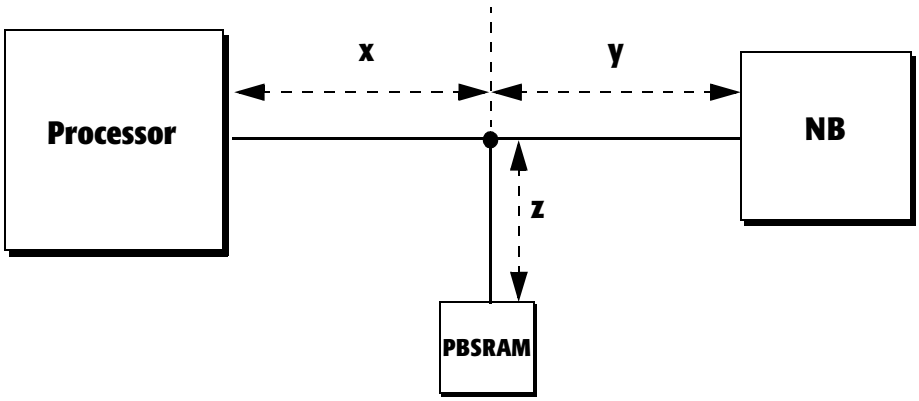


Figure 18. Host Data Bus Routing, Star Topology

Trace length trade-offs for the host data bus topology, daisy chain option 1, are given in Table 14.

Table 14. Host Data Bus Trace Length Trade-offs, Option 1

Signal	Processor to PBSRAM	PBSRAM to NB	Processor to NB	Stub Length	Comment
D[63:0]	1.5 inches	4.5 inches	6.0 inches	0.5 inches	Note
D[63:0]	2.0 inches	4.0 inches	6.0 inches	0.5 inches	Note
D[63:0]	2.5 inches	3.5 inches	6.0 inches	0.5 inches	Note

Note:
These dimensions are maximum trace lengths.

Trace length trade-offs for the host data bus topology, daisy chain option 2, are given in Table 15.

Table 15. Host Data Bus Trace Length Trade-offs, Option 2

Signal	PBSRAM to Processor	Processor to NB	PBSRAM to NB	Stub Length	Comment
D[63:0]	1.5 inches	4.5 inches	6.0 inches	0.5 inches	Note
D[63:0]	2.0 inches	4.0 inches	6.0 inches	0.5 inches	Note
D[63:0]	2.5 inches	3.5 inches	6.0 inches	0.5 inches	Note

Note:
These dimensions are maximum trace lengths.

6.4 Host Multidrop Address Bus

Refer to Figure 19 for an illustration of the host multidrop address bus routing guidelines for systems that use a chipset with an integrated L2 cache tag.

- The trace length between the processor and PBSRAM A must be 3.0 inches or less.
- The trace length between PBSRAM A and PBSRAM B must be 2.0 inches or less.
- The trace length between PBSRAM B and the Northbridge must be 3.0 inches or less.
- The total trace length between the processor and the Northbridge must be 8.0 inches or less.
- The stub to each PBSRAM chip must be 0.5 inch or less.

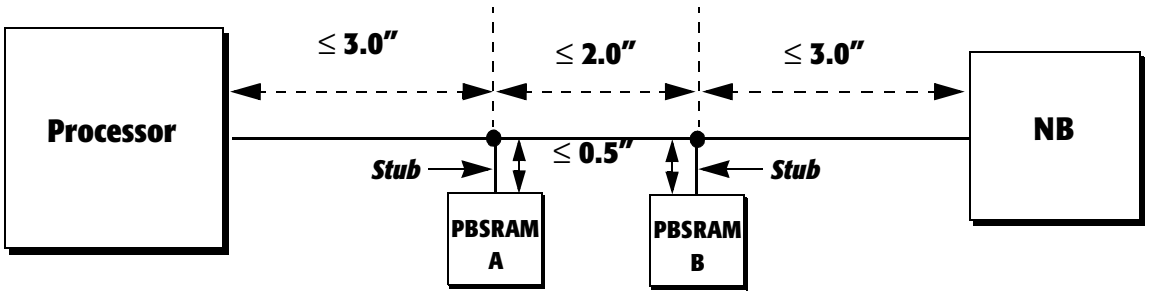


Figure 19. Host Multidrop Address Bus Routing, Integrated L2 Cache Tag

Trace length trade-offs for the host multidrop address bus as illustrated in Figure 19 are given in Table 16.

Table 16. Host Multidrop Address Bus Trace Length Trade-offs

Signal	Processor to PBSRAM A	PBSRAM A to PBSRAM B	PBSRAM B to NB	Processor to NB	Stub Length	Comment
A[n:3]	3.0 inches	2.0 inches	3.0 inches	8.0 inches	0.5 inches	Notes 1, 2
A[n:3]	3.0 inches	1.0 inches	3.0 inches	7.0 inches	0.5 inches	Notes 1, 2
A[n:3]	3.0 inches	3.0 inches	2.0 inches	8.0 inches	0.5 inches	Notes 1, 2

Notes:

1. *The number of address bits routed to the two PBSRAM chips depends on the size of the L2 cache.*
2. *These dimensions are maximum trace lengths.*

Refer to Figure 20 for an illustration of the host multidrop address bus routing guidelines for systems that use a chipset with an external L2 cache tag.

- The trace length between the processor and the PBSRAM chip must be 3.0 inches or less.
- The trace length between the PBSRAM chip and the tag SRAM chip must be 1.0 inch or less.
- The trace length between the tag SRAM chip and the Northbridge must be 4.0 inches or less.
- The total trace length between the processor and the Northbridge must be 8.0 inches or less.
- The stub to the PBSRAM chip and the tag SRAM chip must be 0.5 inch or less.

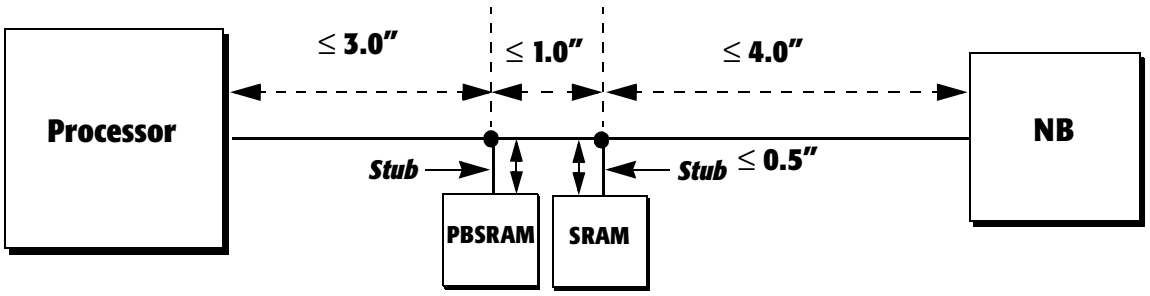


Figure 20. Host Multidrop Address Bus Routing, External L2 Cache Tag

6.5 Host Point-to-Point Address Bus

Refer to Figure 21 for an illustration of the host point-to-point address bus routing guidelines.

- The total trace length between the processor and the Northbridge must be 9.0 inches or less.

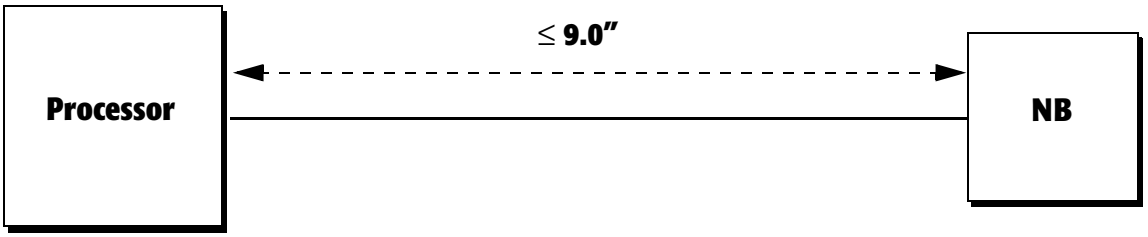


Figure 21. Host Point-to-Point Address Bus Routing

6.6 Host Multidrop Control Signals

The topology recommendation for the processor-sourced multidrop control signals is more flexible than the general topology recommendation provided in Section 6.2 on page 33. In particular, a daisy chain topology is still recommended, but the processor, the PBSRAM chip, and the Northbridge can be routed in any order along the daisy chain.

The byte enables, BE[7:0]#, are examples of multidrop control signals sourced by the processor and routed to a single PBSRAM chip and the Northbridge (refer to Figure 22). ADS# is an example of a multidrop control signal sourced by the processor and routed to each of the PBSRAM chips in a system that uses a chipset with an integrated L2 cache tag (refer to Figure 23).

- The trace length between each component is not critical and can be any length that facilitates the trace routing. However, the total trace length between the components on the ends of the daisy chain must be 8.0 inches or less.
- The stub to the component in the middle of the daisy chain must be 0.5 inch or less.

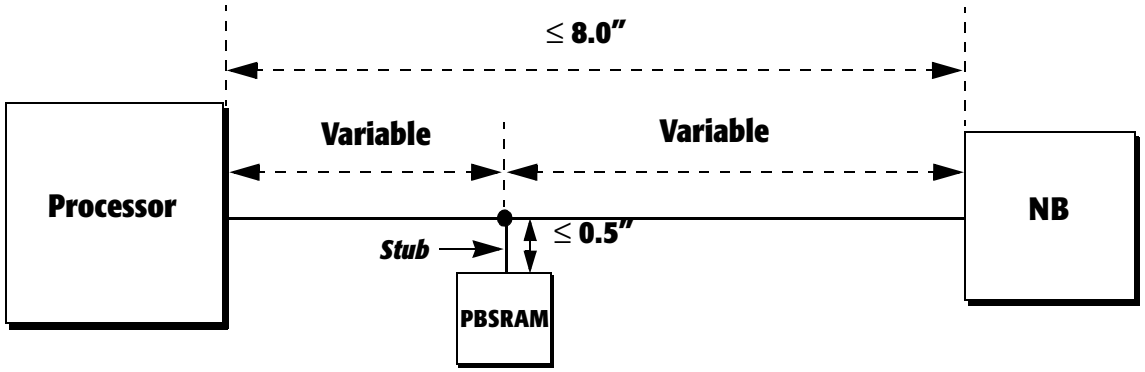


Figure 22. Processor Multidrop Control Signal Routing to PBSRAM/Northbridge

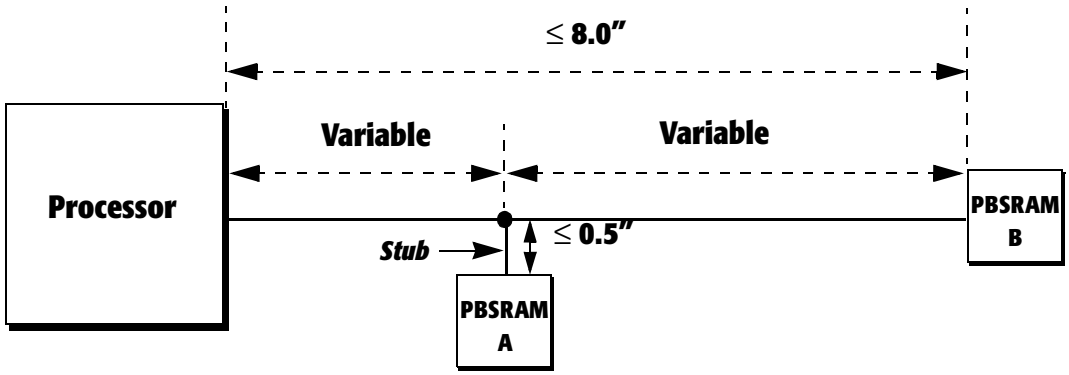


Figure 23. Processor Multidrop Control Signal Routing to PBSRAMs

6.7 Host Point-to-Point Control Signals

Refer to Figure 24 for an illustration of the point-to-point control signal routing guidelines for those signals routed between the processor and the Northbridge. ADSC#, CACHE#, D/C#, HITM#, LOCK#, M/IO#, SMIACT#, and W/R# are examples of point-to-point control signals that are sourced by the processor and routed to the Northbridge. AHOLD, BOFF#, BRDY#, EADS#, and NA# are examples of point-to-point control signals that are sourced by the Northbridge and routed to the processor.

- The total trace length between the processor and the Northbridge must be 6.0 inches or less.

Refer to Figure 25 for an illustration of the point-to-point control signal routing guidelines for those signals routed between the processor and a single PBSRAM chip (systems that use a chipset that requires an external L2 cache tag).

- The total trace length between the processor and the PBSRAM chip must be 6.0 inches or less.

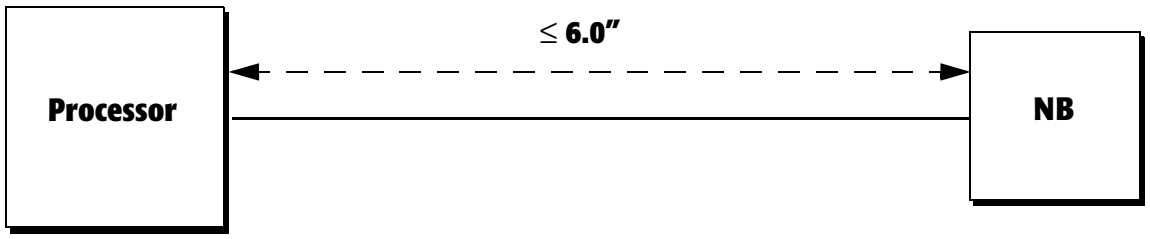


Figure 24. Processor Point-to-Point Control Signal Routing to/from Northbridge

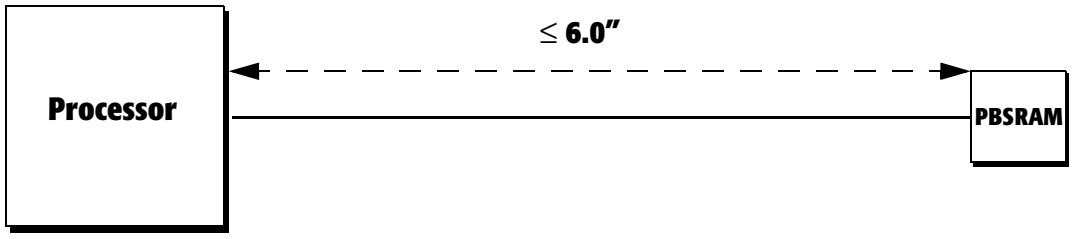


Figure 25. Processor Point-to-Point Control Signal Routing to PBSRAM

6.8 Northbridge Multidrop Control Signals

Refer to Figure 26 for an illustration of the Northbridge-sourced multidrop control signal routing guidelines for systems that contain two PBSRAM chips. BWE#, CADS#, CADV#, CE1#, COE#, and GWE# are examples of multidrop control signals that are sourced by the Northbridge.

- The trace length between the Northbridge and PBSRAM B must be 6.0 inches or less.
- The trace length between PBSRAM B and PBSRAM A must be 1.5 inches or less.
- The total trace length between the Northbridge and PBSRAM A must be 7.5 inches or less.
- The stub to PBSRAM B must be 0.5 inch or less.

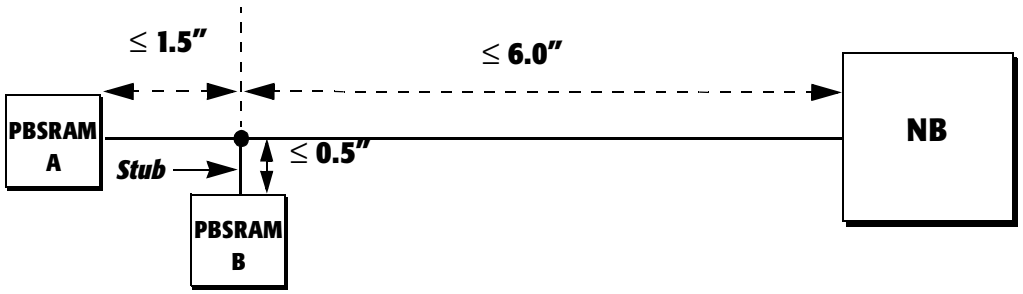


Figure 26. Northbridge Multidrop Control Signal Routing to PBSRAM

6.9 Northbridge Point-to-Point Control Signals

Refer to Figure 27 for an illustration of the Northbridge-sourced point-to-point control signal routing guidelines for systems that contain a single PBSRAM chip (systems that use a chipset that requires an external L2 cache tag). BWE#, CADS#, CADV#, CE1#, COE#, and GWE# are examples of point-to-point control signals that are sourced by the Northbridge.

- The total trace length between the Northbridge and the PBSRAM chip must be 8.0 inches or less.

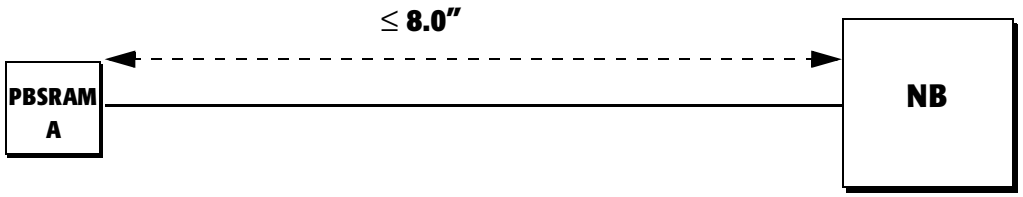


Figure 27. Northbridge Point-to-Point Control Signal Routing to PBSRAM

6.10 Northbridge Tag Address Bus

Refer to Figure 28 for an illustration of the point-to-point tag address (TA) bus routing guidelines.

- The total trace length between the tag SRAM chip and the Northbridge must be 2.5 inches or less.

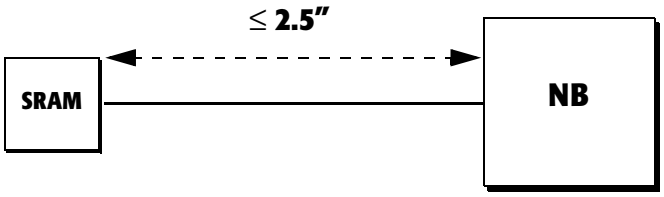


Figure 28. Northbridge Tag Address Bus Routing

6.11 Placement of Board Components Examples

Figures 29 and 30 show examples of the placement of board components.

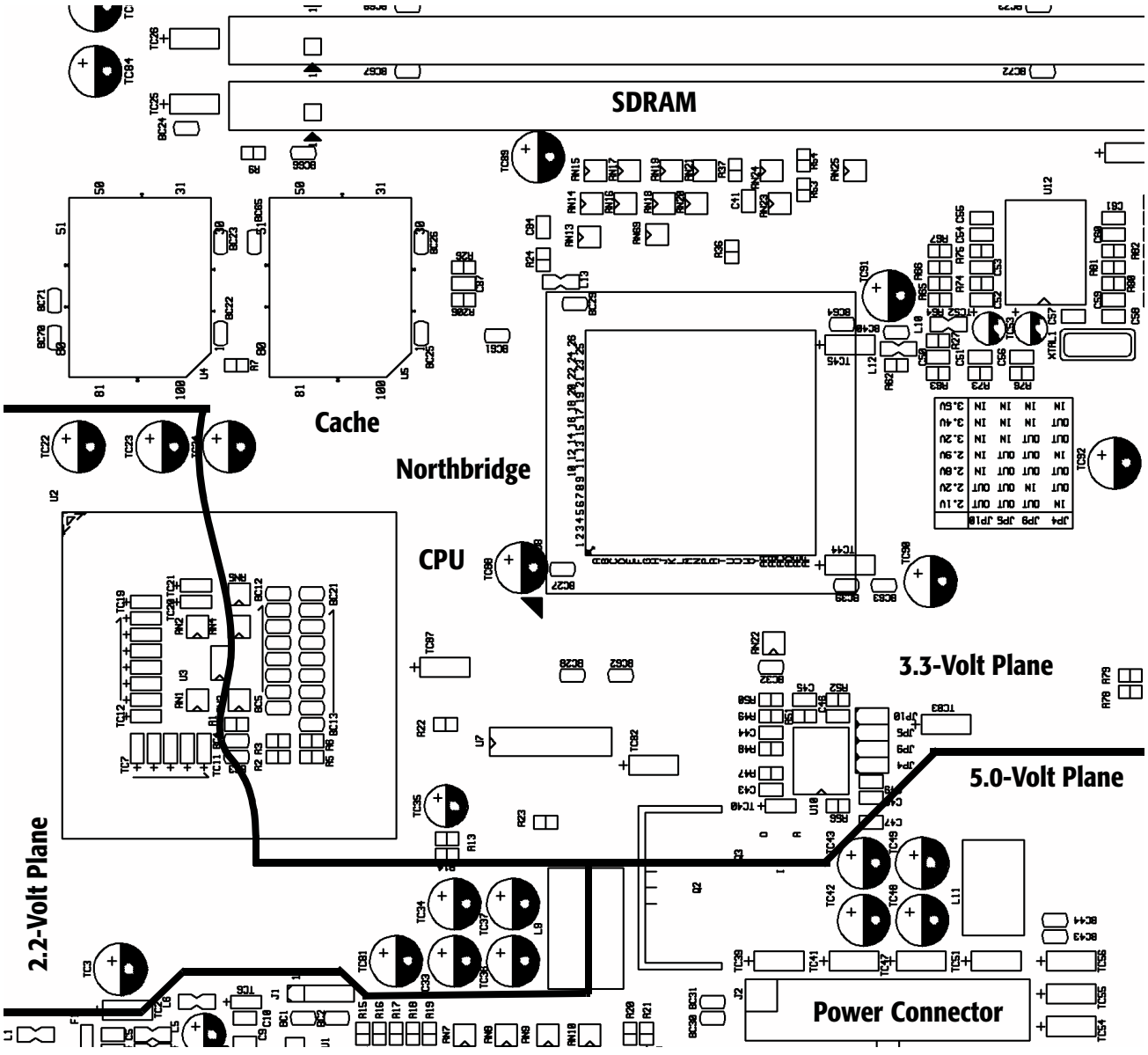


Figure 29. ATX Motherboard (Partial View)

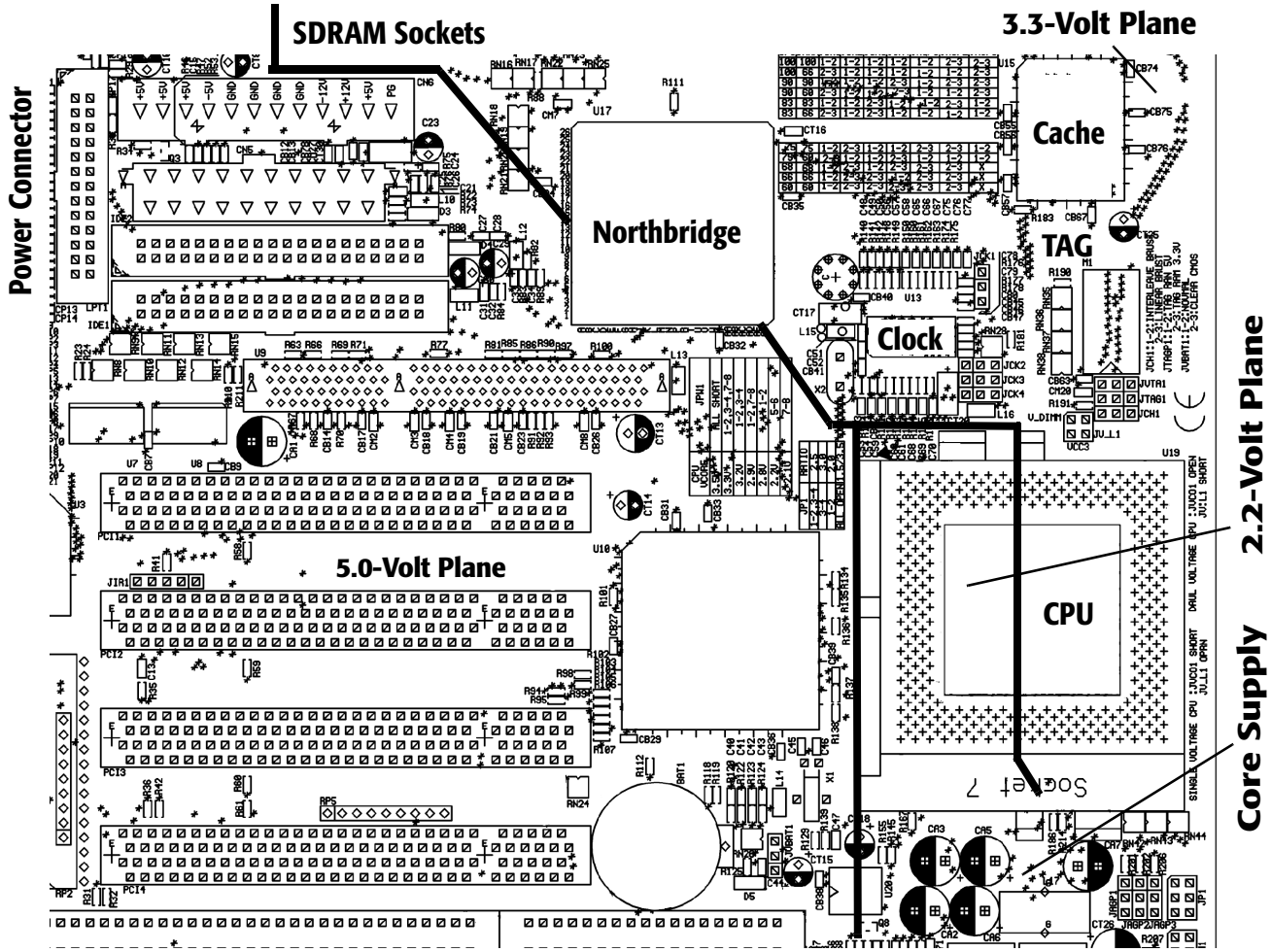


Figure 30. Baby AT Motherboard (Partial View)

7 100-MHz System Timing Analysis

7.1 Setup Timing Analysis

Table 17 through Table 21 combine all of the AC specifications and assumptions included in this document to summarize the setup timing analysis of the 100-MHz components of the system. Note that every trace has a minimum margin—or timing guardband—of 0 ns.

Each table contains the following headings:

- *Signal*—each table contains the output or bidirectional signals from each 100-MHz component that are typically used in systems.
- *Maximum Valid Delay*—these values are taken from "Processor AC Specifications" on page 4 and "Chipset AC Specifications" on page 19.
- *System Delay*—the sum of the worst-case propagation delay (1.75 ns or 2.5 ns for point-to-point and multidrop traces, respectively), maximum clock skew (500 ps) and maximum clock jitter (250 ps).
- *Minimum Setup*—these values are taken from "Processor AC Specifications" on page 4 and "Chipset AC Specifications" on page 19.
- *Cycle Time*—one or two clock periods, depending on the path length.
- *Margin*—the *Cycle Time* minus the sum of *Maximum Valid Delay*, *System Delay*, and *Minimum Setup.*
- *Loads*—the total number of loads (or drops) on this signal.

Table 17. Processor to Northbridge Setup Timing Analysis

Signal	Maximum Valid Delay	System Delay	Minimum Setup	Cycle Time	Margin	Loads	Comment
A[31:3]	4.0 ns	3.25 ns	12.7 ns	20.0 ns	50 ps	2-4	Note 1, 2
ADSC#	4.0 ns	2.50 ns	3.5 ns	10.0 ns	0 ps	2	
BE[7:0]#	4.0 ns	3.25 ns	12.7 ns	20.0 ns	50 ps	3	Note 2
CACHE#	4.0 ns	2.50 ns	13.5 ns	20.0 ns	0 ps	2	Note 2
D/C#	4.0 ns	2.50 ns	3.5 ns	10.0 ns	0 ps	2	
D[63:0]	4.5 ns	3.25 ns	1.7 ns	10.0 ns	550 ps	3	
HITM#	4.0 ns	2.50 ns	13.5 ns	20.0 ns	0 ps	2	Note 2
LOCK#	4.0 ns	2.50 ns	3.5 ns	10.0 ns	0 ps	2	
M/IO#	4.0 ns	2.50 ns	3.5 ns	10.0 ns	0 ps	2	
SMIACT#	4.0 ns	2.50 ns	13.5 ns	20.0 ns	0 ps	2	Note 2
W/R#	4.0 ns	2.50 ns	3.5 ns	10.0 ns	0 ps	2	

Notes:

1. *The loading on the address bus is dependent on the presence of an external L2 tag SRAM, the number of PBSRAM chips used, and the size of the L2 cache.*
2. *This analysis assumes these path lengths are two clocks (20.0 ns).*

Table 18. Processor to PBSRAM Setup Timing Analysis

Signal	Maximum Valid Delay	System Delay	Minimum Setup	Cycle Time	Margin	Loads	Comment
A[n:3]	4.0 ns	3.25 ns	2.2 ns	10.0 ns	550 ps	3-4	Note
ADS#	4.0 ns	3.25 ns	2.2 ns	10.0 ns	550 ps	3	
BE[7:0]#	4.0 ns	3.25 ns	2.2 ns	10.0 ns	550 ps	3	
D[63:0]	4.5 ns	3.25 ns	2.2 ns	10.0 ns	50 ps	3	

Note:

The loading on the address bus, and the number of address bits routed to the PBSRAM chip(s), are dependent on the presence of an external L2 tag SRAM, the number of PBSRAM chips used, and the size of the L2 cache.

Table 19. Northbridge to Processor Setup Timing Analysis

Signal	Maximum Valid Delay	System Delay	Minimum Setup	Cycle Time	Margin	Loads	Comment
A[31:3]	13.7 ns	3.25 ns	3.0 ns	20.0 ns	50 ps	2-4	Note 1
AHOLD	4.0 ns	2.50 ns	3.5 ns	10.0 ns	0 ps	2	
BOFF#	4.0 ns	2.50 ns	3.5 ns	10.0 ns	0 ps	2	
BRDY#	4.5 ns	2.50 ns	3.0 ns	10.0 ns	0 ps	2	
D[63:0]	4.5 ns	3.25 ns	1.7 ns	10.0 ns	550 ps	3	
EADS#	4.5 ns	2.50 ns	3.0 ns	10.0 ns	0 ps	2	
KEN#(INV)	3.7 ns	3.25 ns	3.0 ns	10.0 ns	50 ps	3	Note 2
NA#	5.8 ns	2.50 ns	1.7 ns	10.0 ns	0 ps	2	

Notes:

1. *The loading on the address bus is dependent on the presence of an external L2 tag SRAM, the number of PBSRAM chips used, and the size of the L2 cache.*
2. *The system delay of 3.25 ns assumes that KEN# and INV are sourced from the same pin by the Northbridge. If this is not the case, then INV and KEN# are point-to-point traces and a system delay of 2.5 ns can be used, in which case the maximum allowable valid timing for these signals can be increased to 4.5 ns.*

Table 20. Northbridge to PBSRAM Setup Timing Analysis

Signal	Maximum Valid Delay	System Delay	Minimum Setup	Cycle Time	Margin	Loads	Comment
A[n:3]	13.7 ns	3.25 ns	2.2 ns	20.0 ns	850 ps	3-4	Note 1, 2
BWE#	4.5 ns	3.25 ns	2.2 ns	10.0 ns	50 ps	3	
CADS#	4.5 ns	3.25 ns	2.2 ns	10.0 ns	50 ps	3	
CADV#	4.5 ns	3.25 ns	2.2 ns	10.0 ns	50 ps	3	
CE1#	4.5 ns	3.25 ns	2.2 ns	10.0 ns	50 ps	3	
COE#	4.5 ns	3.25 ns	2.2 ns	10.0 ns	50 ps	3	
D[63:0]	4.5 ns	3.25 ns	2.2 ns	10.0 ns	50 ps	3	
GWE#	4.5 ns	3.25 ns	2.2 ns	10.0 ns	50 ps	3	

Notes:

1. *The loading on the address bus, and the number of address bits routed to the PBSRAM chip(s), are dependent on the presence of an external L2 tag SRAM, the number of PBSRAM chips used, and the size of the L2 cache.*
2. *This analysis assumes this path length is two clocks (20.0 ns).*

Table 21. PBSRAM Data Output Setup Timing Analysis

Signal	Maximum Valid Delay	System Delay	Minimum Setup	Cycle Time	Margin	Loads	Comment
PBSRAM Data to Northbridge							
D[63:0]	5.0 ns	3.25 ns	1.7 ns	10.0 ns	50 ps	3	Note 1
PBSRAM Data to Processor							
D[63:0]	5.0 ns	3.25 ns	1.7 ns	10.0 ns	50 ps	3	Note 2

Notes:

1. *Applies to L2 cache writeback cycles.*
2. *Applies to L2 cache read cycles.*

7.2 Hold Timing Analysis

Table 22 through Table 26 combine all of the AC specifications and assumptions included in this document to summarize the hold timing analysis of the 100-MHz components of the system. Note that every trace has a minimum margin—or timing guardband—of 0 ns.

Each table contains the following headings:

- *Signal*—each table contains the output or bidirectional signals from each 100-MHz component that are typically used in systems.
- *Minimum Valid Delay*—these values are taken from "Processor AC Specifications" on page 4 and "Chipset AC Specifications" on page 19.
- *System Delay*—the best-case propagation delay (1.25 ns for point-to-point and multidrop traces), minus the sum of the maximum clock skew (500 ps) and the maximum clock jitter (250 ps).
- *Minimum Hold*—these values are taken from "Processor AC Specifications" on page 4 and "Chipset AC Specifications" on page 19.
- *Margin*—the sum of the *Minimum Valid Delay* and the *System Delay*, minus the *Minimum Hold.*
- *Loads*—the total number of loads (or drops) on this signal.

Table 22. Processor to Northbridge Hold Timing Analysis

Signal	Minimum Valid Delay	System Delay	Minimum Hold	Margin	Loads	Comment
A[31:3]	1.1 ns	500 ps	1.0 ns	600 ps	2-4	Note
ADSC#	1.0 ns	500 ps	1.0 ns	500 ps	2	
BE[7:0]#	1.0 ns	500 ps	1.0 ns	500 ps	3	
CACHE#	1.0 ns	500 ps	1.0 ns	500 ps	2	
D/C#	1.0 ns	500 ps	1.0 ns	500 ps	2	
D[63:0]	1.3 ns	500 ps	1.0 ns	800 ps	3	
HITM#	1.1 ns	500 ps	1.0 ns	600 ps	2	
LOCK#	1.1 ns	500 ps	1.0 ns	600 ps	2	
M/IO#	1.0 ns	500 ps	1.0 ns	500 ps	2	
SMIACT#	1.0 ns	500 ps	1.0 ns	500 ps	2	
W/R#	1.0 ns	500 ps	1.0 ns	500 ps	2	

Note:
The loading on the address bus is dependent on the presence of an external L2 tag SRAM, the number of PBSRAM chips used, and the size of the L2 cache.

Table 23. Processor to PBSRAM Hold Timing Analysis

Signal	Minimum Valid Delay	System Delay	Minimum Hold	Margin	Loads	Comment
A[n:3]	1.1 ns	500 ps	1.0 ns	600 ps	3-4	Note
ADS#	1.0 ns	500 ps	1.0 ns	500 ps	3	
BE[7:0]#	1.0 ns	500 ps	1.0 ns	500 ps	3	
D[63:0]	1.3 ns	500 ps	1.0 ns	800 ps	3	

Note:
The loading on the address bus, and the number of address bits routed to the PBSRAM chip(s), are dependent on the presence of an external L2 tag SRAM, the number of PBSRAM chips used, and the size of the L2 cache.

Table 24. Northbridge to Processor Hold Timing Analysis

Signal	Minimum Valid Delay	System Delay	Minimum Hold	Margin	Loads	Comment
A[31:3]	1.0 ns	500 ps	1.0 ns	500 ps	2-4	Note
AHOLD	1.0 ns	500 ps	1.0 ns	500 ps	2	
BOFF#	1.0 ns	500 ps	1.0 ns	500 ps	2	
BRDY#	1.0 ns	500 ps	1.0 ns	500 ps	2	
D[63:0]	1.2 ns	500 ps	1.5 ns	200 ps	3	
EADS#	1.0 ns	500 ps	1.0 ns	500 ps	2	
KEN#(INV)	1.0 ns	500 ps	1.0 ns	500 ps	3	
NA#	1.0 ns	500 ps	1.0 ns	500 ps	2	

Note:
The loading on the address bus is dependent on the presence of an external L2 tag SRAM, the number of PBSRAM chips used, and the size of the L2 cache.

Table 25. Northbridge to PBSRAM Hold Timing Analysis

Signal	Minimum Valid Delay	System Delay	Minimum Hold	Margin	Loads	Comment
A[n:3]	1.0 ns	500 ps	1.0 ns	500 ps	3-4	Note
BWE#	1.0 ns	500 ps	1.0 ns	500 ps	3	
CADS#	1.0 ns	500 ps	1.0 ns	500 ps	3	
CADV#	1.0 ns	500 ps	1.0 ns	500 ps	3	
CE1#	1.0 ns	500 ps	1.0 ns	500 ps	3	
COE#	1.0 ns	500 ps	1.0 ns	500 ps	3	
D[63:0]	1.2 ns	500 ps	1.0 ns	700 ps	3	
GWE#	1.0 ns	500 ps	1.0 ns	500 ps	3	

Note:
The loading on the address bus, and the number of address bits routed to the PBSRAM chip(s), are dependent on the presence of an external L2 tag SRAM, the number of PBSRAM chips used, and the size of the L2 cache.

Table 26. PBSRAM Data Output Hold Timing Analysis

Signal	Minimum Valid Delay	System Delay	Minimum Hold	Margin	Loads	Comment
PBSRAM Data to Northbridge						
D[63:0]	1.5 ns	500 ps	1.0 ns	1.0 ns	3	Note 1
PBSRAM Data to Processor						
D[63:0]	1.5 ns	500 ps	1.5 ns	500 ps	3	Note 2

Notes:

1. *Applies to L2 cache writeback cycles.*
2. *Applies to L2 cache read cycles.*