4.0 ELECTRICAL SPECIFICATIONS

4.1 Electrical Connections

This section provides information on electrical connections, absolute maximum ratings, recommended operating conditions, DC characteristics, and AC characteristics. All voltage values in Electrical Specifications are measured with respect to V_{SS} unless otherwise noted.

The M II CPU operates using two power supply voltages—one for the I/O (3.3 V) and one for the core (2.9 V).

4.1.1 Power and Ground Connections and Decoupling

Testing and operating the M II CPU requires the use of standard high frequency techniques to reduce parasitic effects. The high clock frequencies used in the M II CPU and its output buffer circuits can cause transient power surges when several output buffers switch output levels simultaneously. These effects can be minimized by filtering the DC power leads with low-inductance decoupling capacitors, using low impedance wiring, and by utilizing all of the V_{CC} and GND pins. The M II CPU contains 296 pins with 25 pins connected to V_{CC2} (2.9 volts), 28 pins connected to V_{CC3} (3.3 volts), and 53 pins connected to V_{SS} (ground).

4.1.2 Pull-Up/Pull-Down Resistors

Table 4-1 lists the input pins that are internally connected to pull-up and pull-down resistors. The pull-up resistors are connected to V_{CC} and the pull-down resistors are connected to V_{SS}. When unused, these inputs do not require connection to external pull-up or pull-down resistors. The SUSP# pin is unique in that it is connected to a pull-up resistor only when SUSP# is not asserted.

Table 4-1. Pins Connected to Internal Pull-Up and Pull-Down Resistors

SIGNAL	PIN NO.	RESISTOR
BRDYC#	Y3	20-kΩ pull-up
CKMUL0	Y33	20-kΩ pull-down (see text)
CKMUL1	X34	20-kΩ pull-up (see text)
Reserved	AN35	20-kΩ pull-down
Reserved	W35	20-kΩ pull-up
SMI#	AB34	20-kΩ pull-up
SUSP#	Y34	20-kΩ pull-up (see text)
TCK	M34	20-kΩ pull-up
TDI	N35	20-kΩ pull-up
TMS	P34	20-kΩ pull-up
TRST#	Q33	20-kΩ pull-up

4.1.3 Unused Input Pins

All inputs not used by the system designer and not listed in Table 4-1 should be connected either to ground or to V_{CC}. Connect active--high inputs to ground through a 10 kΩ (± 10%) pull-down resistor and active-low inputs to V_{CC} through a 10 kΩ (± 10%) pull-up resistor to prevent possible spurious operation.

4.1.4 NC and Reserved Pins

Pins designated NC have no internal connections. Pins designated RESV or RESERVED should be left disconnected. Connecting a reserved pin to a pull-up resistor, pull-down resistor, or an active signal could cause unexpected results and possible circuit malfunctions.

4.2 Absolute Maximum Ratings

The following table lists absolute maximum ratings for the M II CPU processors. Stresses beyond those listed under Table 4-2 limits may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those listed under “Recommended Operating Conditions” Table 4-3 (Page 4-3) is possible. Exposure to conditions beyond Table 4-2 may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings may also result in reduced useful life and reliability.

Table 4-2. Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS	NOTES
Operating Case Temperature	-65	110	°C	Power Applied
Storage Temperature	-65	150	°C	
Supply Voltage, V_{CC3}	-0.5	4.0	V	
Supply Voltage, V_{CC2}	-0.5	3.3	V	
Voltage On Any Pin	-0.5	V_{CC3} + 0.5	V	Not to exceed Vcc3 max
Input Clamp Current, I_{IK}		10	mA	Power Applied
Output Clamp Current, I_{OK}		25	mA	Power Applied

4.3 Recommended Operating Conditions

Table 4-3 presents the recommended operating conditions for the M II CPU device.

Table 4-3. Recommended Operating Conditions

PARAMETER	MIN	MAX	UNITS	NOTES
T_C Operating Case Temperature	0	70	°C	Power Applied
V_{CC3} Supply Voltage (3.3 V)	3.135	3.465	V	
V_{CC2} Supply Voltage (2.9 V)	2.8	3.0	V	
V_{IH} High-Level Input Voltage (except CLK)	2.00	3.55	V	
V_{IH} CLK High-Level Input Voltage	2.0	5.5	V	
V_{IL} Low-Level Input Voltage	-0.3	0.8	V	
I_{OH} High-Level Output Current		-1.0	mA	$V_O=V_{OH(MIN)}$
I_{OL} Low-Level Output Current		5.0	mA	$V_O=V_{OL(MAX\}}$

4.4 DC Characteristics

Table 4-4. DC Characteristics (at Recommended Operating Conditions) 1 of 2

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{OL} Low-Level Output Voltage			0.4	V	I_{OL} = 5 mA
V_{OH} High-Level Output Voltage	2.4			V	I_{OH} = -1 mA
I_I Input Leakage Current For all pins (except those listed in Table 4-1).			±15	µA	$0 < V_{IN} < V_{CC3}$ Note 1
I_{IH} Input Leakage Current For all pins with internal pull-downs.			200	µA	V_{IH} = 2.4 V Note 1
I_{IL} Input Leakage Current For all pins with internal pull-ups.			-400	µA	V_{IL} = 0.45 V Note 1
C_{IN} Input Capacitance			15	pF	f = 1 MHz*
C_{OUT} Output Capacitance			20	pF	f = 1 MHz*
C_{IO} I/O Capacitance			25	pF	f = 1 MHz*
C_{CLK} CLK Capacitance			15	pF	f = 1 MHz*

*Note: Not 100% tested.

Table 4-5. DC Characteristics (at Recommended Operating Conditions) 2 of 2

PARAMETER	ICC2 MAX	ICC3 MAX	UNITS	NOTES
I_{CC} Active I_{CC}				Notes 1, 2
225 MHz (M II -300)	8580	100	mA	
233 MHz (M II -300)	8800	100		
250 MHz (M II -333)	9500	100		
300 MHz (M II -350)	TBD	TBD		
I_{CCSM} Active I_{CC}				Notes 1, 2, 3
225 MHz (M II -300)	52	100	mA	
233 MHz (M II -300)	54	100		
250 MHz (M II -333)	57	100		
300 MHz (M II -350)	TBD	TBD		
I_{CCSS} Standby I_{CC}				Notes 1, 2, 4
0 MHz (Suspended/CLK Stopped)	30	50.0	mA	

Notes:
1. These values should be used for power supply design. Maximum I_{CC} is determined using the worst-case instruction sequences and functions at maximum Vcc.
2. Frequency (MHz) ratings refer to the internal clock frequency.
3. All inputs at 0.4 or V_{CC3} - 0.4 (CMOS levels). All inputs held static except clock and all outputs unloaded (static I_{OUT} = 0 mA).
4. All inputs at 0.4 or V_{CC3} - 0.4 (CMOS levels). All inputs held static and all outputs unloaded (static I_{OUT} = 0 mA).

Table 4-6. Power Dissipation

PARAMETER	POWER		UNITS	NOTES
	TYP	MAX		
Active Power Dissipation				Note 1
225 MHz (M II -300)	15.0	24.9	W	
233 MHz (M II -300)	15.4	25.5		
250 MHz (M II -333)	16.6	27.6		
300 MHz (M II -350)	TBD	TBD		
Suspend Mode Power Dissipation				Notes 1, 2
225 MHz (M II -300)		0.150	W	
233 MHz (M II -300)		0.152		
250 MHz (M II -333)		0.157		
300 MHz (M II -350)		TBD		
Standby Mode Power Dissipation				Notes 1, 3
0 MHz (Suspended/CLK Stopped)		0.070	W	

Notes:
1. Systems must be designed to thermally dissipate the maximum active power dissipation. Maximum power is determined using the worst-case instruction sequences and functions with Vcc2 = 2.9 V and Vcc3 = 3.3 V.
2. All inputs at 0.4 or V_{CC3} - 0.4 (CMOS levels). All inputs held static except clock and all outputs unloaded (static I_{OUT} = 0 mA).
3. All inputs at 0.4 or V_{CC3} - 0.4 (CMOS levels). All inputs held static and all outputs unloaded (static I_{OUT} = 0 mA).

4.5 AC Characteristics

Tables 4-7 through 4-12 (Pages 4-8 through 4-11) list the AC characteristics including output delays, input setup requirements, input hold requirements and output float delays. These measurements are based on the measurement points identified in Figure 4-1 (Page 4-7) and Figure 4-2 (Page 4-8). The rising clock edge reference level V_{REF} and other reference levels are shown in Table 4-7. Input or output signals must cross these levels during testing.

Figure 4-1 shows output delay (A and B) and input setup and hold times (C and D). Input setup and hold times (C and D) are specified minimums, defining the smallest acceptable sampling window a synchronous input signal must be stable for correct operation.

The JTAG AC timing is shown in Table 4-13 (Page 13) supported by Figures 4-6 (Page 4-13) though 4-8 (Page 4-14).

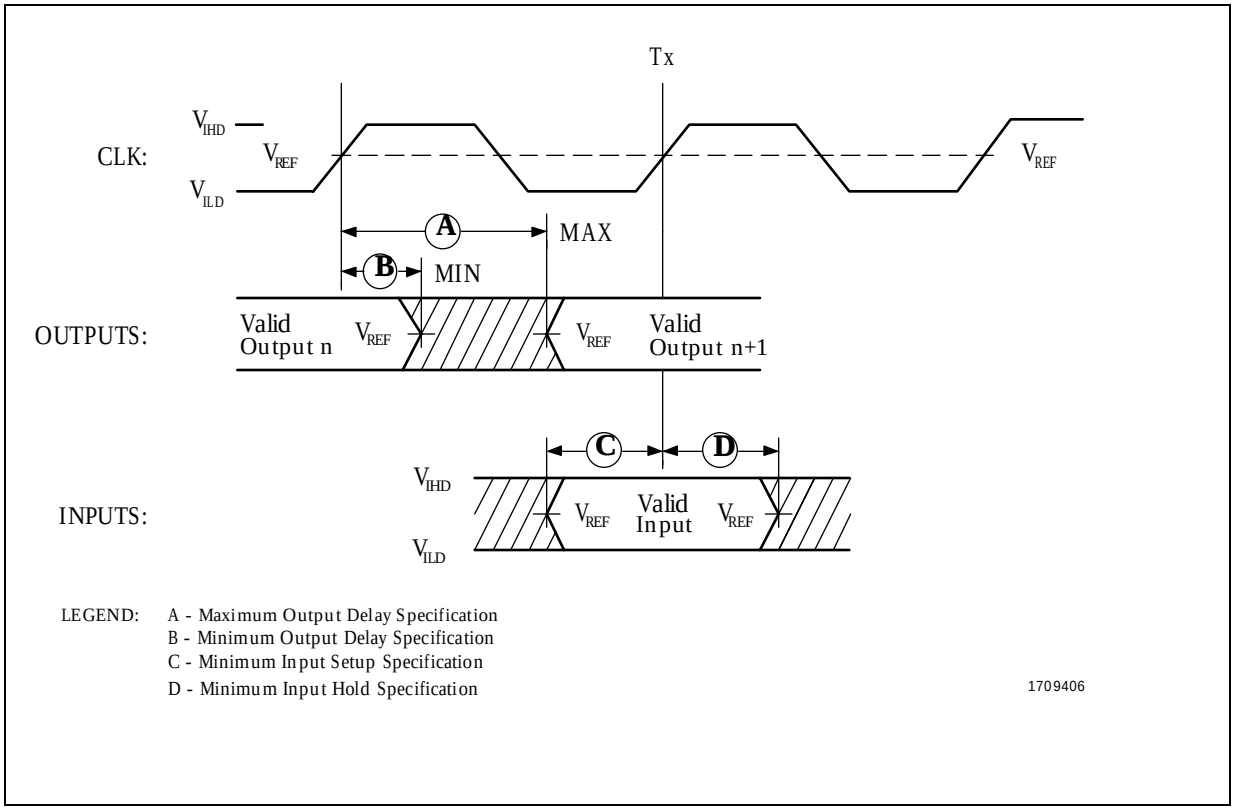

Figure 4-1. Drive Level and Measurement Points for Switching Characteristics

Table 4-7. Drive Level and Measurement Points for Switching Characteristics

SYMBOL	VOLTAGE (Volts)
V_{REF}	1.5
V_{IHD}	2.3
V_{ILD}	0

Note: Refer to Figure 4-1.

Table 4-8. Clock Specifications

T_{CASE} = 0°C to 70°C, See Figure 4-2

	PARAMETER	60-MHz BUS		66-MHz BUS		75-MHz BUS		83-MHz BUS		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f	CLK Frequency		60		66.6		75		83	MHz
T1	CLK Period	16.67		15.0		13.33		12.0		ns
T2	CLK Period Stability		±250		±250		±250		±250	ps
T3	CLK High Time	4.0		4.0		4.0		4.0		ns
T4	CLK Low Time	4.0		4.0		4.0		4.0		ns
T5	CLK Fall Time	0.15	1.5	0.15	1.5	0.15	1.5	0.15	1.5	ns
T6	CLK Rise Time	0.15	1.5	0.15	1.5	0.15	1.5	0.15	1.5	ns

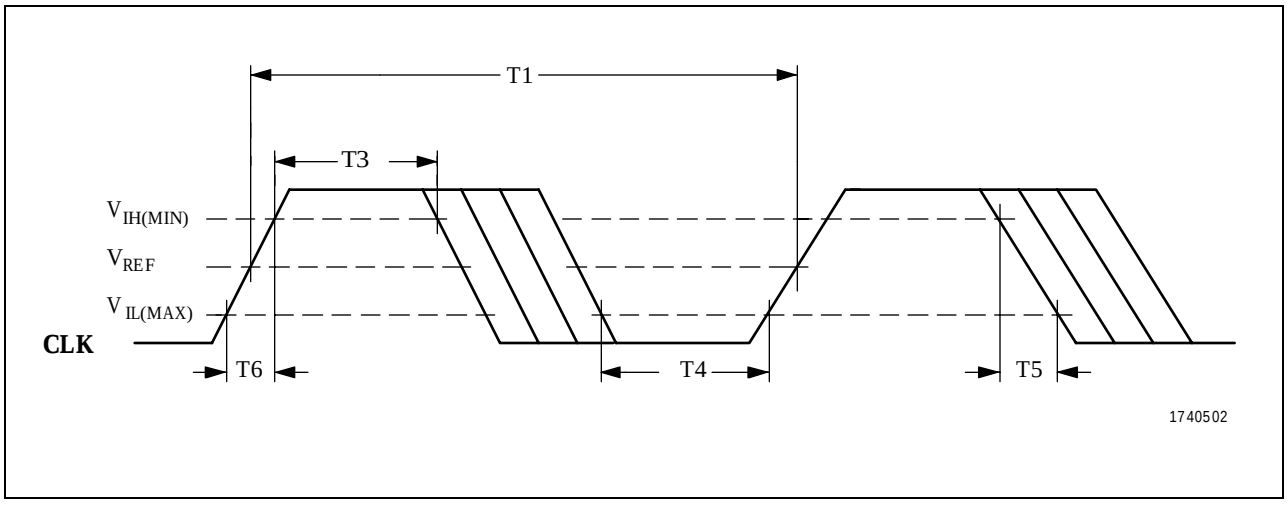

Figure 4-2. CLK Timing and Measurement Points

Table 4-9. Output Valid Delays
C_L = 50 pF, T_{case} = 0°C to 70°C, See Figure 4-3

	PARAMETER	60-MHz BUS		66-MHz BUS		75-MHz BUS		83-MHz BUS		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
T7a	A31-A3	1.0	7.0	1.0	6.3	1.0	6.3	1.0	5.7	ns
T7b	BE7#-BE0#, CACHE#, D/C#, LOCK#, PCD, PWT, SCYC, SMIACT#, W/R#	1.0	7.0	1.0	7.0	1.0	7.0	1.0	6.0	ns
T7c	ADS#	1.0	7.0	1.0	6.0	1.0	6.0	1.0	5.5	ns
T7d	M/IO#	1.0	7.0	1.0	5.9	1.0	5.9	1.0	5.5	ns
T8	ADSC#	1.0	7.0	1.0	7.0	1.0	7.0	1.0	6.5	ns
T9	AP	1.0	8.5	1.0	8.5	1.0	8.5	1.0	7.5	ns
T10	APCHK#, PCHK#, FERR#	1.0	8.3	1.0	7.0	1.0	7.0	1.0	6.5	ns
T11	D63-D0, DP7-DP0 (Write)	1.3	7.5	1.3	7.5	1.3	7.5	1.3	7.0	ns
T12a	HIT#	1.0	8.0	1.0	6.8	1.0	6.8	1.0	6.0	ns
T12b	HITM#	1.1	6.0	1.1	6.0	1.1	6.0	1.1	5.5	ns
T13a	BREQ	1.0	8.0	1.0	8.0	1.0	8.0	1.0	7.0	ns
T13b	HLDA	1.0	8.0	1.0	6.8	1.0	6.8	1.0	6.0	ns
T14	SUSPA#	1.0	8.0	1.0	8.0	1.0	8.0	1.0	7.0	ns

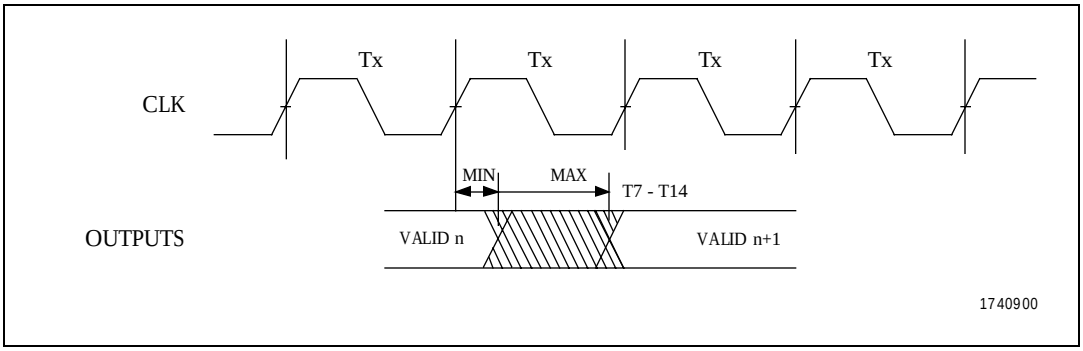

Figure 4-3. Output Valid Delay Timing

Table 4-10. Output Float Delays

C_L = 50 pF, T_{case} = 0°C to 70°C, See Figure 4-5

	PARAMETER	60-MHz BUS		66-MHz BUS		75-MHz BUS		83-MHz BUS		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
T15	A31-A3, ADS#, BE7#-BE0#, CACHE#, D/C#, LOCK#, PCD, PWT, SCYC, SMIACT#, W/R#		10.0		10.0		10.0		10.0	ns
T16	AP		10.0		10.0		10.0		10.0	ns
T17	D63-D0, DP7-DP0 (Write)		10.0		10.0		10.0		10.0	ns

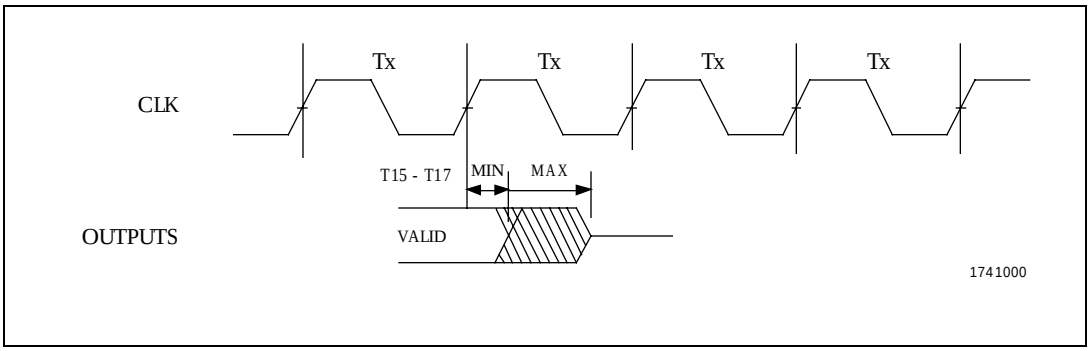

Figure 4-4. Output Float Delay Timing

Table 4-11. Input Setup Times
T_{case} = 0°C to 70°C, See Figure 4-5

SYMBOL	PARAMETER	60-MHz BUS	66-MHz BUS	75-MHz BUS	83-MHz BUS	UNITS
		MIN	MIN	MIN	MIN	
T18a	A20M#,	5.0	5.0	3.3	3.0	ns
T18b	FLUSH#, IGNNE#, SUSP#	5.0	5.0	3.3	3.0	ns
T19a	AHOLD, BOFF#	5.0	5.0	3.3	3.0	ns
T19b	HOLD	5.0	5.0	3.3	3.0	ns
T20	BRDY#	5.0	5.0	3.3	3.0	ns
T21	BRDYC#	5.0	5.0	3.3	3.0	ns
T22a	A31-A3, AP, BE7#-BE0#,	5.0	5.0	3.3	3.0	ns
T22b	AP	5.0	5.0	3.3	3.0	ns
T22c	D63-D0 (Read), DP7-DP0 (Read)	3.0	3.0	3.0	2.7	ns
T23a	EADS#	5.0	5.0	5.0	4.5	ns
T23b	INV	5.0	5.0	5.0	4.5	ns
T24	INTR, NMI, RESET, SMI#, WM_RST	5.0	5.0	5.0	4.5	ns
T25a	EWBE#, NA#, WB/WT#	4.5	4.5	3.0	2.7	ns
T25b	KEN#	4.5	4.5	3.0	2.7	ns

Table 4-12. Input Hold Times
T_{case} = 0°C to 70°C, See Figure 4-5

SYMBOL	PARAMETER	60-MHz BUS	66-MHz BUS	75-MHz BUS	83-MHz BUS	UNITS
		MIN	MIN	MIN	MIN	
T27	A20M#, FLUSH#, IGNNE#, SUSP#	1.0	1.0	1.0	1.0	ns
T28a	AHOLD, BOFF#	1.0	1.0	1.0	1.0	ns
T28b	HOLD	1.0	1.0	1.0	1.0	ns
T29	BRDY#	1.0	1.0	1.0	1.0	ns
T30	BRDYC#	1.0	1.0	1.0	1.0	ns
T31a	A31-A3, AP, BE7#-BE0#,	1.0	1.0	1.0	1.0	ns
T31b	AP	1.0	1.0	1.0	1.0	ns
T31c	D63-D0 (Read), DP7-DP0 (Read)	2.0	1.5	1.5	1.5	ns
T32	EADS#, INV	1.0	1.0	1.0	1.0	ns
T33	INTR, NMI, RESET, SMI#, WM_RST	1.0	1.0	1.0	1.0	ns
T34	EWBE#, KEN#, NA#, WB/WT#	1.0	1.0	1.0	1.0	ns

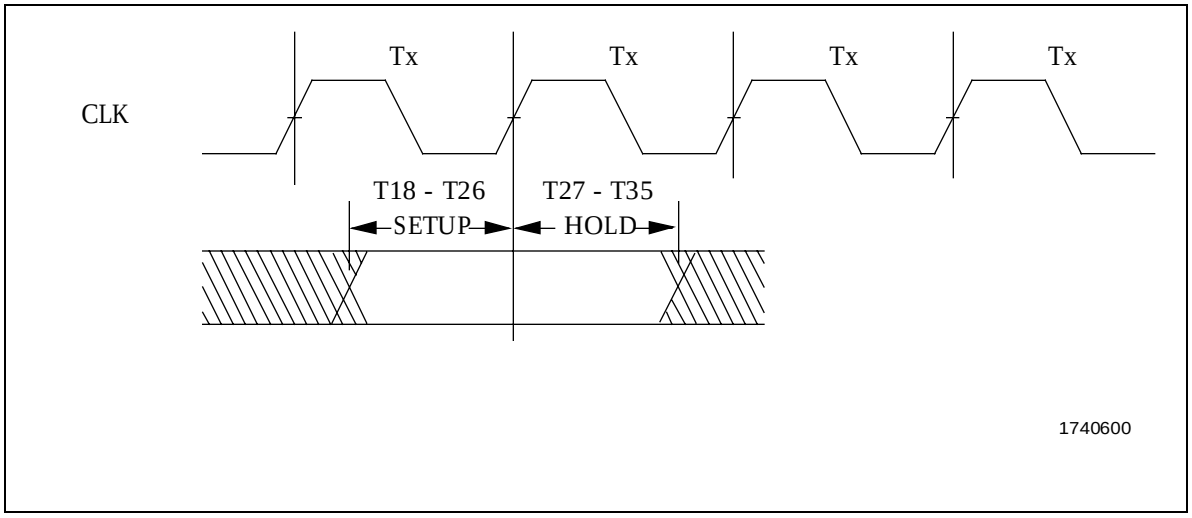

Figure 4-5. Input Setup and Hold Timing

Table 4-13. JTAG AC Specifications

SYMBOL	PARAMETER	ALL BUS FREQUENCIES		UNITS	FIGURE
		MIN	MAX		
	TCK Frequency (MHz)		20	ns	
T36	TCK Period	50		ns	4-6
T37	TCK High Time	25		ns	4-6
T38	TCK Low Time	25		ns	4-6
T39	TCK Rise Time		5	ns	4-6
T40	TCK Fall Time		5	ns	4-6
T41	TDO Valid Delay	3	20	ns	4-7
T42	Non-test Outputs Valid Delay	3	20	ns	4-7
T43	TDO Float Delay		25	ns	4-7
T44	Non-test Outputs Float Delay		25	ns	4-7
T45	TRST# Pulse Width	40		ns	4-8
T46	TDI, TMS Setup Time	20		ns	4-7
T47	Non-test Inputs Setup Time	20		ns	4-7
T48	TDI, TMS Hold Time	13		ns	4-7
T49	Non-test Inputs Hold Time	13		ns	4-7

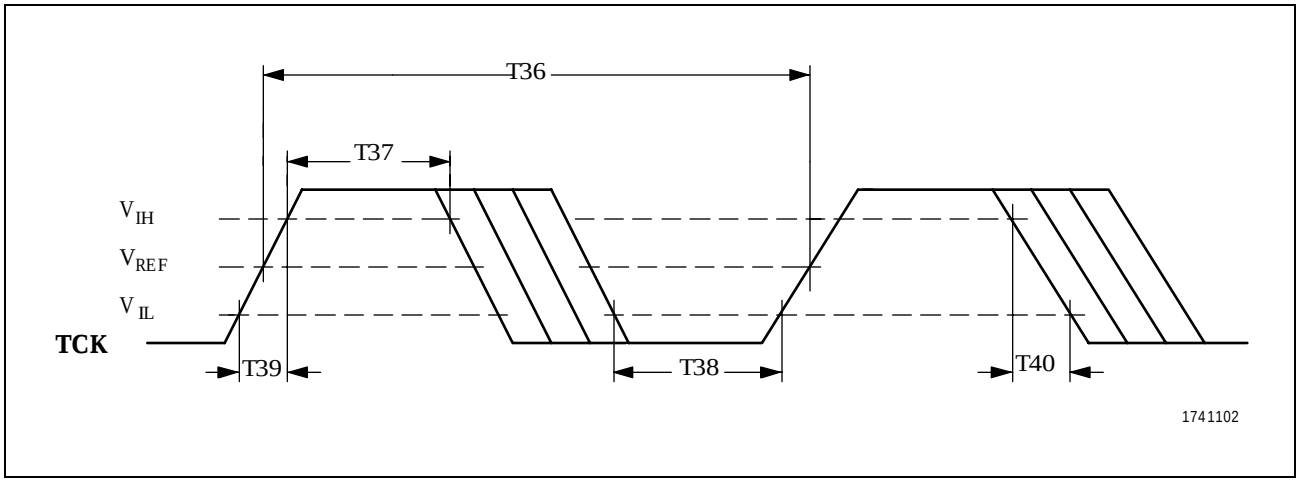

Figure 4-6. TCK Timing and Measurement Points

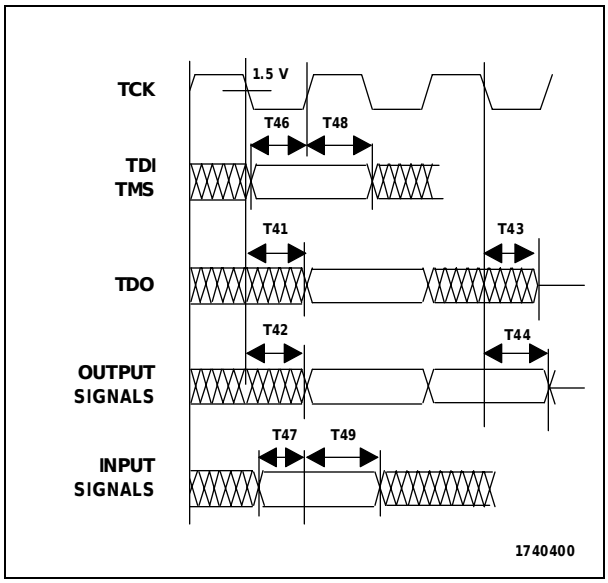

Figure 4-7. JTAG Test Timings

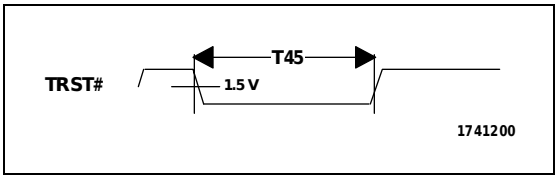

Figure 4-8. Test Reset Timing