Plug and Play with the IBM 486DX2 Processor

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Application Note

Introduction

The IBM 486DX2 processor is pin and plug compatible with most existing Intel 486DX and 486DX2 motherboards. However, in some cases, the actual implementation of the memory controller chip or chipset and the pinout of the socket can cause the IBM 486DX2 to not function properly. This application note is intended to outline the steps necessary for the IBM 486DX2 to "plug and play" and to clarify the differences between the pin-outs and pin functions. In some cases and for best performance, the IBM 486DX2 may require changes to BIOS. These BIOS changes will not be covered in this application note.

The first step in understanding this problem is to realize what the IBM 486DX2 is compatible with in regards to the Intel® 486 processor. The instruction set, physical bus structure, paging operation, and architectural registers are all directly compatible. However, there are enhanced features on the IBM 486DX2 that either are not present (write-back cache) or are in a different form. These differences account for both the pin-out and pin function differences. The rest of this application note details these differences, the actual pin-out differences on both the PGA and QFP package styles, and then gives a description of how to Plug and Play using the PGA package in an Intel designed system.

Pin and System Function Differences:

System Management Mode (SMM): In the System Management Mode the IBM 486DX2 can be set to have the hardware interface function identically to the Intel SL486DX2. If the SL-compatible mode is set, then SMIADS# and SMI# will operate identically to the SL486DX2 signals SMIACT# and SMI# respectively. This SL-compatible mode is available in the 3.3 volt version of the IBM 486DX2 and is entered by setting a bit in one of the configuration registers.

Even with the SL-compatible mode set, the IBM 486DX2 is not software compatible in regards to SMM mode. These differences are detailed in the SMM Software Differences section of this application note.

Suspend Processor Operation: The SUSP# pin of the IBM 486DX2 and the STPCLK# input pin of the SL486DX2 are used for the same function, stopping the processor to conserve power, but implement this in a different manner. The STPCLK# pin of the SL486DX2 processor shuts down most of the processor but maintains power to the bus unit so that snooping for the internal cache can continue. Complete power-down of the processor is accomplished by stopping the clock. In this case the processor will not snoop the bus. The SUSP# pin of the IBM 486DX2 also shuts down the processor, however, it also shuts down the bus unit. Therefore, no snooping can occur.

This difference can be handled in the BIOS by either flushing the cache before going into suspend mode if the write-back feature of the internal cache is enabled, or upon resuming power to the processor if in write-through mode.

In power-down mode the signals SUSPA# is an output that is not available on the SL486DX2. This signal can be left disconnected since it is an output.

Warm Reset Function: The WM_RST pin on the IBM 486DX2, like the SRESET pin on the Intel SL486DX2, is used to accomplish a soft processor reset. The IBM 486DX2 does not flush the cache automatically like the SL486DX2 does, however, if the INVAL pin is enabled and high during a WM_RST, then the cache is flushed. This INVAL pin is connected to a no-connect pin on the Intel SL486DX2 pin-out. It has an internal pull-up resistor, so that if left unconnected it will be sampled as a 1 or true. The INVAL pin is enabled by setting a bit in one of the machine specific registers.

Another difference between the WM_RST pin and the SRESET pin is that the WM_RST pin is asynchronous to the processor, while the SRESET pin is synchronous to the processor and waits until the instruction completes before being accomplished.

Write-Back Cache Coherency: The write-back pins INVAL and HITM# are required to keep the write-back internal cache coherent with the main memory. These pins are not present on the SL486DX2 but these functions or some similar method will be required on any future processor that uses an internal write-back cache.

PGA Package Pin-Out Differences

There are 16 pin-out differences between the current IBM 486DX2 and the Intel SL486DX2. Pins that are not listed are identical between the two pin-outs. These differences are detailed below.

Physical Pin-Out:

Pin	Current BL486DX2	Intel SL486DX2
A3	NC	TCK
A10	SUSPA#	NC
A12	SMI#	NC
A13	RPLSET1	INT NC
A14	NC	TDI
B10	NC	SMI#
B12	TEST	NC
B13	WM_RST	NC
B14	NC	TMS
B16	NC	TDO
C10	SMADS#	SRESET
C12	RPLSET0	SMIACT#
C13	RPLVAL#	NC
G15	SUSP#	STPCLK#
R17	HITM#	NC
S4	INVAL	NC

This group of pins can then be divided up into several areas; system management pins, write-back cache pins, test and miscellaneous pins.

The test and miscellaneous pins are shown below. The differences are due to either processor dependencies or because a pin is not connected in one of the configurations.

Pin	Current BL486DX2	Intel SL486DX2
A3	NC	TCK
A14	NC	TDI
B12	TEST	NC
B14	NC	TMS
B16	NC	TDO

The TCK, TDI, TMS, and TDO pins are used for JTAG testing and are not available on the IBM 486DX2. The TEST pin of the IBM 486DX2 is undefined.

The next group of pins refers to power management and for the write-back cache and non-catastrophic reset.

Pin	Current BL486DX2	Intel SL486DX2
B13	WM_RST	NC
C10	SMADS#	SRESET
C12	RPLSET0	SMIACT#
A12	SMI#	NC
B10	NC	SMI#
G15	SUSP#	STPCLK#
A10	SUSPA#	NC
A13	RPLSET1	INT NC
C13	RPLVAL	# NC
R17	HITM#	NC
S4	INVAL	NC

The first group of pins shows the mismatch between the non-catastrophic reset functions (WM_RST and SRESET). Although they share the same purpose, they are not identical in function and do not share the same pin. Likewise, for the System Management Mode output acknowledgment function (SMADS# and SMIACT#), they share the same purpose but not the same pin. The next two pins are identical in function (SMI#), however the pins are not the same.

On the next pin, G15, the signal names between the IBM 486DX2 and the SL486DX2 are similar but not identical. These differences were explained in the previous section. The SUSPA# pin is an output of the IBM 486DX2 acknowledging suspend mode, it is not present on the SL486DX2.

The pins in the final section all have no connection on the Intel SL486DX2 side, these are outputs or inputs that have to do with the write-back cache function present only on the IBM 486DX2.

The INT NC refers to an internal no connection. This means that a system designer can route through this pin with any signal and not cause a problem. As shown in the pin descriptions, this is not true on the IBM 486DX2.

QFP Package Pin-Out Differences

According to the most recent data books available, there are no compatibility problems with the IBM 486DX2 and the Intel SL486DX2 or the Intel 486DX4 processors in the QFP format. There is a potential problem with any future releases of Intel processors with write-back cache capability, since new external pins are required to fully support this feature.

The following list details the 15 differences in pin-outs between these processors. Note, that all differences are matched with a no-connect pin on the corresponding pin of the other processor. The similar pin matches are as defined earlier in this paper.
Physical Pin-Out:

Pin	Current BL486DX2	Intel SL486DX2	Intel 486DX4
3	NC	Vcc*	Vcc5
11	NC	NC	CLKMUL
18	NC	TCK	TCK
58	WM_RST	SRESET	SRESET
59	SMADS#	SMIACT#	SMIACT#
63	RPLSET0	NC	NC
64	RPLSET1	NC	NC
67	INVAL	NC	NC
68	NC	TD0	TD0
70	RPLVAL#	NC	NC
71	SUSPA#	NC	NC
73	SUSP#	STPCLK#	STPCLK#
96	HITM#	NC	NC
167	NC	TMS	TMS
168	NC	TDI	TDI

* This Vcc is for I/O voltage sensitivities (either 3.3V or 5V inputs).

Plug and Play with the IBM 486DX2 in PGA Form

There are four steps in getting your IBM 486DX2 to "plug and play", the first step is to read the documentation for your planar. Determine if there are any particular configuration steps such as jumpers or setup information that must be changed for the IBM 486DX2. If the documentation refers to the Cyrix DX2, use these configuration steps to configure the motherboard as the Cyrix DX2 is the same as the IBM 486DX2. If there is no reference to either the Cyrix DX2 or the IBM 486DX2 then make sure the board is setup for an Intel 486DX2.

The second step is to determine if the controller chip or chipset is compatible with the IBM 486DX2. Our FAX-Back service contains an application note (#40006) that states all of the compatible chipsets. Obtain a copy of this application note and determine if the chipset that is on your motherboard is compatible from the list. If you found configuration information from your motherboard documentation in the previous step then it is probable that your chipset is compatible and need not be checked.

The memory controller chip or chipset is usually a surface-mounted integrated circuit larger than everything else on the motherboard except for the processor. The numbers on the top of the I.C. show the chipset number and manufacturer. These items are then checked against the list from the application note on chipsets.

The next step is to try out the processor. Install the processor with the correct pin 1 orientation and reassemble your chassis. Now try to power-up your computer. The minor changes between the IBM 486DX2 and the Intel 486DX2 will not cause any type of electrical short to damage the processor or planar. If the computer boots up to the DOS prompt, congratulations, you are now running with the state-of-the-art Blue Lightning DX2 processor.

However, if the system does not boot, the next step is to rewire the socket to connect some signals that may be unconnected due to the pin-out differences of the IBM 486DX2 and the Intel 486DX2. A third application note is available on the FAX-Back service (#40004) that details a design of a universal socket for both the IBM 486DX2 and the Intel 486DX2. In our case since the board has already been designed, an interposer socket can temporarily make the wiring changes required. Three machine pin sockets with the 168 pinout of an 486DX2 are needed. The three sockets will be wired together and then plugged between the IBM 486DX2 and the existing socket. This will allow our changes to be connected to the IBM 486DX2 without having to cut any traces on the motherboard.

The top socket will be wired to the bottom socket and the middle socket will have some pins removed to disconnect some of the pins from being directly connected. These sockets are wired as shown in figure 1 below. Care must be taken to insure that the wires are connected to the correct pins and that the socket orientation (top or bottom) is taken into account while assembling this interposer.

Once the interposer is completed and checked, plug the IBM 486DX2 into the top socket with the correct pin 1 orientation. Then plug both the interposer and processor into the motherboard. This assembly is shown in Figure 2.

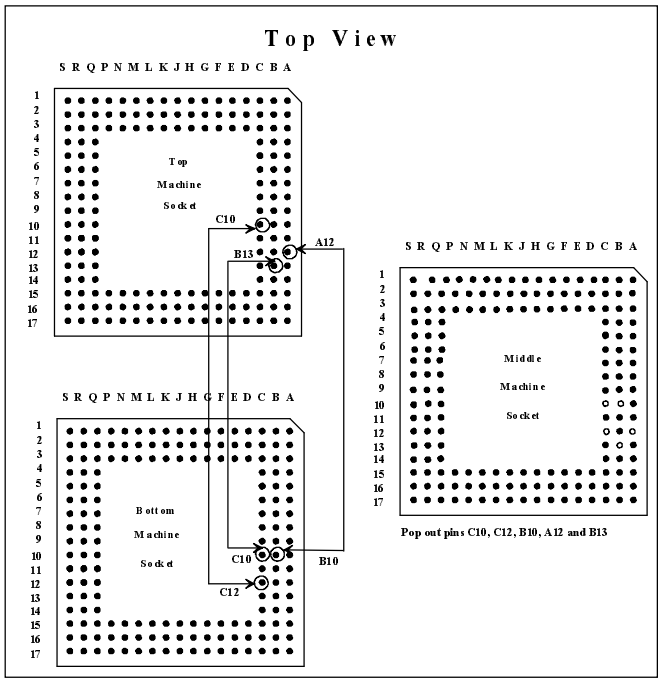

Figure 1.

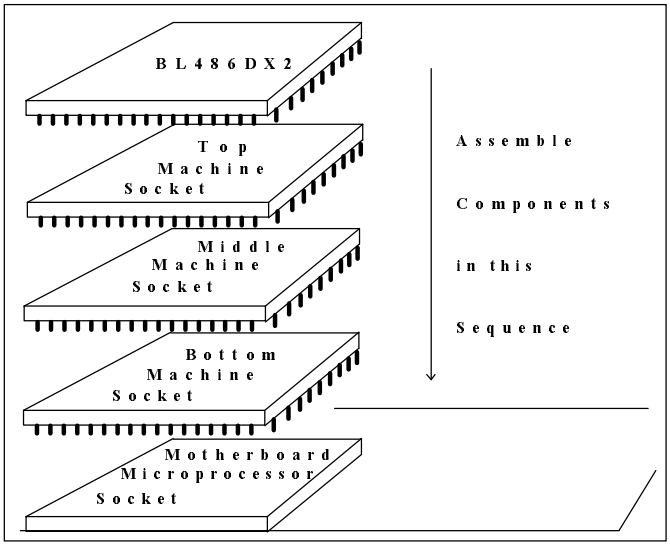

Figure 2.

Now reassemble your computer and power it up. If the wiring and other changes were done correctly no power shorts should occur. The computer should now power-up to the DOS prompt.

Finally, if the computer does not boot, the BIOS is probably the cause. Since there are several sources for BIOS code and the source code is usually not available, this problem is beyond the scope of this application note.

SMM Software Differences:

Hardware Compatibility Setup: The SMI# pin on the IBM 486DX2 is identical to the SMI# pin on the SL486DX2 if CCR3(3)=1 and this pin is asserted at least 2 CLK cycles before entering SMM mode. To perform I/O trapping, SMI# must be asserted at least 3 cycles before RDY#/BRDY# is asserted. The SMADS# pin on the IBM 486DX2 is functionally identical to the SMIACT# pin on the SL486DX2 if CCR3(3)=1.

Software Configuration of SMM of the IBM 486DX2: The CCR1, CCR3 and SMAR configuration registers must be initialized by software, usually BIOS. Configuration registers are accessed by writing an 8-bit index to I/O port 22h, followed by an I/O read or I/O write to I/O port 23h. The indices are C1h (CCR1), C3h (CCR3), CDh (SMAR bits 23:16), CEh (SMAR bits 15:8) and CFh (SMAR bits 7:0).

CCR3(3)=1	SMM_MODE bit Makes SMM pins compatible to the SL486DX2.
CCR3(1)	NMIEN bit Enables NMI during SMM mode. Same as issuing IRET during SMM mode on the SL486DX2.
CCR1(1)=1	SMI bit Enables SMI# and SMADS# pins.
SMAR(23:4)	Starting address bits A31:A12 for SMM memory space. Bits A11:A0 are assumed to be zero. This is the SMM base address (start of SMM service routine)
SMAR(3:0)	Size of SMM memory space. Ranges from 4KB to 32MB. Starting address must be a multiple of the SMM memory size.

The location of the SMM header for the IBM 486DX2 is determined from SMAR(23:4) and SMAR(3:0). The header is 48 bytes located in a block of memory at the top of SMM address space, from

SMM base address + size of SMM memory - 48

to

SMM base address + size of SMM memory - 1

The SMM service routine is located at the SMM base address.

For the SL486DX2 the header is relocatable with a default range of 0003FE00h - 0003FFFFh, and the service routine is relocatable with a default of 00038000h.

The system designer must determine the proper location for the service routine and initialize the SMAR register appropriately.

Changes to the SMM Routine When Using the IBM 486DX2 in SMM Mode: For IBM 486DX2, the following architectural registers are saved in the header area upon entering SMM mode: CS, EIP, next EIP, EFLAGS, CR0, DR7. In addition, the IBM 486DX2 saves I/O Trap Restart information in the header.

For IBM 486DX2, the following architectural registers have defined values (all others have unpredictable values):

CS=SMM base specified by SMAR; CS limit set to 4GB
EIP=00000000h
EFLAGS=00000002h
CR0=60000010h
DR7=00000400h

The SL486DX2 saves the following architectural registers in the header area when entering SMM mode: general registers (EAX, EBX, ECX, EDX, ESI, EDI, EBP, ESP), segment registers (CS, SS, DS, ES, FS, GS), EIP, EFLAGS, CR0, CR3, GDT base, IDT base, system segment registers (TR, LDTR). In addition, the SL486DX2 saves the following information in the header: Auto Halt Restart, I/O Trap Restart, SMM revision ID, SMM base address relocation.

For SL486DX2, the following architectural registers have defined values (all others have unpredictable values):

CS=3000h
SS=0000h
DS=0000h
ES=0000h
FS=0000h
GS=0000h
EIP=00008000h
EFLAGS=00000002h
CR0 bits 0,2,3,31 cleared; others unmodified
DR6=00000000h

Any assumptions made by the SMM routine about the CPU state must be reviewed. Registers which are modified by the SMM routine must be saved and restored inside the routine if they are not saved in the header. Since the SL486DX2 saves a greater portion of the CPU state to the

SMM header, it is possible that SMM routines written for SL486DX2 may have to be modified to work with IBM 486DX2.

Using the I/O Trap feature of SMM: When an I/O instruction causes an SMM interrupt, the IBM 486DX2 stores in the header the type of instruction (IN, INSx, OUT, OUTSx, REP types), write data size, write address, write data and value of index register (ESI or EDI) before instruction was executed. By reading this information, the SMM routine can recognize when an I/O instruction causes the interrupt and either force the instruction to restart or monitor data written to the port.

The SL486DX2 does not save I/O information in the header. It can automatically force I/O instructions to restart by setting a bit in the header, but it cannot monitor data written to these ports. Therefore, the SMM routine can be made more robust when switching from the SL486DX2 to the IBM 486DX2.

Summary:

This application note discusses the differences between the Blue Lightning DX2 and the Intel SL486DX2 processors. It also defines the steps necessary to get the Blue Lightning DX2 processor in the PGA package to plug and play in most existing Intel 486DX2 motherboards. For more complete information on the IBM 486DX2 consult the DataBook and refer to other application notes and White Papers available on the FAX-Back service.

References:

1. **Blue Lightning 486DX2 Databook**, IBM Microelectronics, 1994.

2. **Intel 486 DX2 Microprocessor Data Book**, Intel Corporation, 2/1994.

3. **Intel 486 DX4 Microprocessor Data Book**, Intel Corporation, 2/1994.

4. **Intel SL Enhanced Intel 486 Microprocessor Data Sheet Addendum**, Intel Corporation, 1993.

5. **Microprocessors, Vol. 2**, Intel Corporation, 1994.