Applications Note

Guide for Adapting Intel and AMD Designed Motherboards for the IBM 6x86MX Microprocessor

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Introduction

The IBM 6x86MX™ microprocessor[1] is plug compatible with existing motherboards for the Intel Pentium® processor[2] with MMX technology[3] and the AMD K6™ processor[4] with MMX technology. This document describes the pin and functional differences between these three processors and outlines the steps necessary to run the IBM 6x86MX processor in boards which were designed for the other processors.

In some cases, the IBM 6x86MX processor[5] requires changes to the BIOS, power regulator and CPU cooling solution to work efficiently in these boards. For these items please consult the following applications notes:

- #40250 and #40251*: IBM 6x86MX Microprocessor BIOS Writer's Guide*
- #40253: *Thermal Solutions for the IBM 6x86MX Microprocessor*
- #40255: *Voltage Regulators for the IBM 6x86MX Microprocessor*

It is important to understand the areas of similarity between these processors. All three are available in a PGA package which plugs into Socket 7. Most I/O pins perform the same function for the three processors. Internally the processors are similar. The physical bus structure, paging operation and architectural registers are all compatible. The instruction set is compatible with the exception of a few instructions that are described later in this document. All three processors support the x86 and MMX instruction sets. The remainder of this document describes the pin and functional differences between these processors.

Pin Differences

While the IBM 6x86MX processor and the Intel P55C processor use the 296-pin PGA package, the AMD K6 processor has an additional 25 pins to fully utilize the 321-pin capacity of Socket 7. The 25 new pins on the AMD K6 processor are grouped as follows:

14 for **Vss**, **2** for **Vcc2**, **4** for **Vcc3**, **4** as **NC**, and **1** called **KEY**.

The 25 extra pins on the K6 processor are for power (20 pins), mechanical guidance (1 pin) and no-connects (4 pins). The pin named “KEY” is not an electrically active pin, its function is to mechanically guide the chip when being plugged in the socket. Overall, the impact of these new pins is minimal on adapting the IBM 6x86MX CPU on system boards designed for the AMD K6 processor. Therefore, the following discussion concentrates on the differences among the IBM 6x86MX processor, Intel P55C and AMD K6 on the 296-pin basis.

The pin differences are divided into five subgroups: clock mode selection, multiprocessor support, processor initialization, breakpoint/performance monitoring and power management. Table 1 lists the pin differences.

1. The IBM 6x86MX microprocessor was designed by Cyrix Corp., and manufactured by IBM Microelectronics

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2. *Intel Pentium Processor Family Developer’s Manual.* Volume 3: Architecture and Programming Manual.

Intel Corporation, 1995.

3. *Pentium Processor Family Developer’s Manual.* Intel Corporation, 1997
4. *AMD-K6 MMX Processor Data Sheet.* Advanced Micro Devices, 1997
5. *IBM 6x86 Microprocessor Databook.* IBM Microelectronics, 1997

Function	Pin #	IBM 6x86MX[5]	Intel P55C[3]	AMD K6[4]	Description (I/O: I=input, O=output)
Clock Mode	W35	RSVD	NC	BF2	K6: Core/Bus frequency ratio (I)
	X34	CLKMUL1	BF1	BF1	Core/Bus frequency ratio (I)
	Y33	CLKMUL0	BF0	BF0	Core/Bus frequency ratio (I)
Multiprocessor	H34	NC	PICCLK	INC	P55C: Programmable Interrupt Controller Clock (I)
	J33	NC	PICD0 DPEN#	RSVD	P55C: Programmable Interrupt Data Line 0 (I/O)
	L35	NC	PICD1/ API-CEN	RSVD	P55C: Programmable Interrupt Data Line 1 (I/O)
	Q35	NC	CPUTYP	RSVD	P55C: Identifies CPU as primary or dual (I)
	AA3	NC	PHIT#	RSVD	P55C: Private hit (I/O)
	AC3	NC	PHITM#	RSVD	P55C: Hit to a modified line (O)
	AD4	NC	PBGNT#	RSVD	P55C: Private bus grant (I/O)
	AE3	NC	PBREQ#	RSVD	P55C: Private bus request (I/O)
	AE35	NC	D/P#	RSVD	P55C: Dual/primary processor indication (O)
Error Detection/ Test/Debug	P4	NC	IERR#	RSVD	P55C: Internal Error (parity) (O)
	Q3	PM0	PM0/BP0	RSVD	P55C: Performance Monitor data bit 0 (O)
	R4	PM1	PM1/BP1	RSVD	P55C: Performance Monitordata bit 1 (O)
	S3	NC	BP2	RSVD	P55C: Breakpoint match 2 (O)
	S5	NC	BP3	RSVD	P55C: Breakpoint match 3 (O)
	Z34	NC	PEN#	INC	P55C: Parity enable (I)
	AC5	NC	PRDY	RSVD	P55C: Probe ready (O)
	AC35	NC	R/S#	INC	P55C: Run/Stop (I)
	AL7	NC	BUSCHK#		P55C: Bus check (I)
Power Management	V34	SUSP#	STPCLK#	STPCLK#	IBM 6x86MX: Suspend Request (I) P55C & K6: Stop internal clock (I)
	W33	SUSPA#	NC	NC	IBM 6x86MX: Suspend Acknowledge (O)
Power	A3	NC	INC	Vss	K6: ground pin
	B2	NC	INC	Vcc2	K6: power pin for the core
	AL1	VCC2DET	VCC2DET#	VCC2DET	Vcc2 detect (O), even
Reset	AA33	WM_RST	INIT	INIT	IBM 6x86MX: Warm reset (I) P55C & K6: Initialization (I)
Reserved/ No Connect	S33	RSVD	NC	NC	
	S35	RSVD	NC	NC	
	Y35	RSVD	RESVD	INC	P55C: Not defined
	AN35	RSVD	NC	NC	
Note: (RSVD = Reserved; NC & INC = No Connect)					

Table 1: Pin differences among the IBM 6x86MX, Intel P55C and AMD K6 microprocessors

Clock Mode Select

The IBM 6x86MX processor uses two pins (Y33 and X34 for signals CLKMUL0 and CLKMUL1) to control the clock mode, which is the same as Intel P55C processor, although Intel uses the signal names BF0 and BF1. Both the IBM 6x86MX processor and Intel P55C processor implement these two pins in a similar way, the only difference is that 6x86MX processor supports 3.5x clock mode while Intel P55C reserves this selection. On the other hand, AMD's K6 has one additional pin (W35, the signal is called BF2) for clock mode control. On all three processors, the clock mode inputs are sampled at RESET for core-to-bus frequency control. Table 2 lists the truth table for the core-to-bus frequency ratio selections. From the clock mode control point of view, virtually no change is needed to plug an the IBM 6x86MX processor in a system designed for Intel P55C. **Care needs to be taken when plugging the IBM 6x86MX processor into a board designed for an AMD K6 processor to ensure that pin W35 (reserved on the IBM 6x86MX processor) floats**. When pin W35 is set to 1 on the AMD K6 processor, the clock mode selection matches the IBM 6x86MX processor (as shown in Table 2). When pin W35 is set to 0 on the AMD K6, the following combinations of X34 and Y33 generate

core-to-bus frequency ratios of 4.0, 4.5, 5.0 and 5.5.

Pin X34	Pin Y33	IBM 6x86MX[5]	Intel P55C[3]	AMD K6[4]
6x86MX: CLKMUL1 P55C: BF1 K6: BF1	6x86MX:CLKMUL0 P55C: BF0 K6: BF0			Pin W35: BF2 for K6 only
0	0	2.5	2.5	W35 = 1, 2.5 W35 = 0, 4.5
0	1	3	3	W35 = 1, 3 W35 = 0, 5
1	0	2	2	W35 = 1, 2 W35 = 0, 4
1	1	3	Reserved	W35 = 1, 3.5 W35 = 0, 5.5
Note: 0 means the pin is driven logically low, and 1 means the pin is driven logically high.				

Table 2: Clock mode selection for the IBM 6x86MX, Intel P55C and AMD K6 processors

Multiprocessor Support

There are a group of pins on the Intel P55C processor for dual processor implementation. Since the IBM 6x86MX and AMD K6 processors do not support multiprocessor design, these pins are simply No Connects on the IBM 6x86MX processor and reserved on the AMD K6 processor. Therefore, the **IBM 6x86MX processor will not plug and run in a multiprocessor system.**

Processor Initialization

The IBM 6x86MX, Intel P55C and AMD K6 microprocessors are initialized in similar ways. RESET is an active high signal for full initialization, and WM_RST (IBM 6x86MX processor) or INIT (Intel P55C and AMD K6 processors) are active high signals for partial initialization.

The RESET sequence is as follows. At system power up, RESET must remain asserted for at least 1 ms after Vcc and CLK reach their specified AC and DC limits. During normal operation (after power-up), RESET must be asserted 15 CLK cycles to be recognized. Asserting RESET suspends all operations in progress, invalidates internal caches, and clears the write buffers, floating point state, MMX state and all registers. Modified cache lines are not written back. Output signals are driven to their reset value within two CLKs of the rising edge of RESET. The IBM 6x86MX, Intel P55C and AMD K6 microprocessors are similar in that outputs and bi-directional signals common to these chips have the same reset state. The falling edge of RESET determines the mode of operation. Table 3 lists the signals are sampled at that time.

Signal Name	Pin	Operation	Processor
FLUSH#	AN7	If 0, tri-state test mode. All outputs except TDO, Vcc2DET and bidis float until the next RESET.	IBM 6x86MX[5], Intel P55C[3]& AMD K6[4]
WM_RST or INIT	AA33	If 1, BIST performed prior to program execution. Take 2^{19} CLK cycles. Register EAX=0 if all tests pass. If an internal parity error is detected during BIST on the Intel P55C, the CPU will assert IERR# (pin P4) and attempt to shut down.	IBM 6x86MX, Intel P55C & AMD K6
BRDYC#	Y3	Determine the drive strength for certain output signals.	Intel P55C & AMD K6

Table 3: Signals sampled at the falling edge of RESET

WM_RST (IBM 6x86MX processor) and INIT (Intel P55C and AMD K6 processors) perform a partial CPU reset. These signals differ from RESET in that the contents of the on-chip cache, write buffers, configuration registers, floating point and MMX registers remain unchanged. WM_RST and INIT are implemented through the same pin and are fully compatible.

Breakpoints and Performance Monitors

Breakpoints

The IBM 6x86MX processor, Intel P55C and AMD K6 microprocessors all allow breakpoints to be programmed through debug registers, but only the Intel P55C processor has output pins (using pins Q3, R4, S3 and S5 for BP0-BP3) to identify when a breakpoint match occurs. The IBM 6x86MX processor and the AMD K6 processor indicate breakpoint matches in software through register DR6.

Performance Monitors

The IBM 6x86MX processor and the Intel P55C processor use the same pins (Q3 and R4) for performance monitoring, while the AMD K6 processor does not have performance monitor output pins. The IBM 6x86MX processor asserts PM0 and PM1 to indicate at least one overflow or event occurred in the associated Performance Monitor Counter (0-1). The Intel P55C processor does the same thing as the IBM 6x86MX processor except it also uses pins Q3 and R4 to indicate breakpoint matches.

Power Management

The IBM 6x86MX processor, Intel P55C and AMD K6 all use pin AB34 for signal SMI# as input to force the processor save the CPU sate and enter the defined system management state. They all use pin AG3 for signal SMIACT# as output to indicate that the processor is operating in system management mode. All three can stop the internal clock through pin V33. The IBM 6x86MX processor calls the signal for pin V33 as SUSP#, while the Intel P55C and AMD K6 processors name this pin as STPCLK#. Asserting this pin causes the processor to stop execution at the next instruction boundary and then stop the internal clock. The difference to implement this pin is that the IBM 6x86MX processor requires the BIOS to enable SUSP# by setting an internal configuration bit (CCR2 bit 7). In addition, the IBM 6x86MX processor has pin W33 (SUSPA#) as output to indicate that the processor has entered low power suspend mode. The Intel P55C and AMD K6 processors do not have the SUSPA# output signal.

Behavioral Differences

Bus State Machine

There is one difference between the bus state machines for these processors. For any two consecutive non-pipelined (NA# negated) bus cycles, the Intel P55C and AMD K6 processors have an idle cycle between the last data transfer of the first cycle and the ADS# for the second cycle. Referring to the state diagram in the *Intel Pentium Processor Family Developer's Manual*[3] on page 6-11 for the Intel P55C, the processor moves from state "T2" to state "Ti" and then to state "T1". Likewise, the state diagram for the AMD K6 processor in the *AMD-K6 MMX Processor Data Sheet*[4] on page 6-3 shows that it moves from state "Data" to state "Idle" to state "Addr". In the same situation, the IBM 6x86MX processor does not insert an idle cycle. The IBM 6x86MX processor moves from state "T2" to state "T1" for all cycles except a cache inquiry hit on modified data (HITM# asserted). The net effect, under the conditions described above, is that the IBM 6x86MX processor initiates bus cycles at different rates than the Intel P55C and the AMD K6 processors, so **the system chipset must be able to operate under different rates of bus initiation.**

Misaligned Accesses

These processors define misaligned transfers differently. The three processors define a misaligned transfer as a non-cacheable memory cycle or an I/O cycle that crosses a specified address boundary. All three processors indicate a misaligned transfer by asserting SCYC at the start of the bus cycle. The difference is that the IBM 6x86MX processor calls the transfer misaligned **only** if the data crosses an 8-byte boundary. Meanwhile, the Intel P55C and AMD K6 processors call the transfer misaligned if 2-byte or 4-byte transfers cross a 4-byte boundary or 8-byte transfers cross an 8-byte boundary.

This means that **the IBM 6x86MX processor requires only one bus cycle** (with appropriate byte enables active) for transfers of 2-bytes or 4-bytes that cross a 4-byte boundary while **the Intel P55C and AMD K6 processors require two bus cycles** to transfer the same information. This difference results in lower bus activity for the IBM 6x86MX processor under these conditions.

INVD Instruction

When the Intel P55C and AMD K6 processors execute INVD, they invalidate the internal cache. This occurs even if the cache contains modified data, which may cause data coherency problems. **The IBM 6x86MX processor executes INVD identical to the WBINVD instruction**, writing all modified cache data to external memory prior to invalidating the internal cache.

System Management Mode (SMM)

All three processors support SMM and support the same hardware protocol, where the SMI# pin is an asynchronous falling edge-triggered hardware interrupt and SMIACT# is an output acknowledge signal

driven active by the processor during SMM mode. They exit SMM via the RSM instruction. The differences (discussed below) are **resolved in software by changing the BIOS and SMM routine** whenever the IBM 6x86MX processor replaces the other two processors.

On the IBM 6x86MX processor, the SMI# and SMIACT# pins must be enabled in BIOS before use. The other processors always recognize these pins. To enable these pins on the IBM 6x86MX processor, the BIOS sets a special configuration bit (CCR1 bit 1) in the IBM 6x86MX processor. In addition, the IBM 6x86MX processor requires BIOS to set up configuration registers (CCR1 bit 7, CCR5 bit 5, ARR3, RCR3) to define the SMM base address and size of SMM memory space.

The IBM 6x86MX processor offers nine instructions for SMM which are not supported by the other processors: SMINT, RDSHR, WRSHR, SVDC, RSDC, SVLDT, RSLDT, SVTS, and RSTS. The SMINT instruction is a software interrupt which provides an alternative to using the hardware interrupt to enter SMM mode. RDSHR and WRSHR relocate the SMM header to a place other than the top of SMM memory (SMM base address + FFFFh). SVDC, RSDC, SVLDT, RSLDT, SVTS and RSTS are instructions which may be added to the SMM handler to save and restore the entire CPU state. This is useful for BIOS writers because the contents of the SMM header differs among these processors and this provides a simple way to save the entire IBM 6x86MX CPU state prior to servicing the interrupt.

The IBM 6x86MX processor offers two types of SMM hardware protocols: SL-Compatible Mode and Cyrix Enhanced Mode. The type is selected by writing a configuration bit (CCR6 bit 0) in the 6x86MX processor. The default is SL-Compatible Mode which is similar in operation to the other processors. In SL-Compatible Mode, the SMI#-SMIACT# pins behave as described earlier in this section. In Cyrix Enhanced Mode, the SMI# signal is level-sensitive and SMIACT# no longer indicates that the CPU is in SMM mode. In Cyrix Enhanced Mode, SMIACT# is asserted during each SMM memory bus cycle and de-asserted for all other cycles. Cyrix Enhanced SMM provides new features, including cacheability of SMM memory and support for nested SMIs.

In summary, when adapting systems to use the 6x86MX processor the BIOS must set up configuration registers to enable SMM operation, understand the organization of the SMM header and determine the initial register settings upon entering SMM. The latter two items may require modification to the SMM service routine.

CPUID Instruction

All three processors support the CPUID instruction but each processor returns a different vendor ID string when CPUID is executed. The vendor ID string for the IBM 6x86MX processor is "CyrixInstead". All three processors enable the CPUID instruction at power-up. In addition, the IBM 6x86MX processor can disable CPUID execution after power-up by writing a configuration bit (CCR4 bit 7).

Model Specific Registers

All three processors support Model Specific Registers, although they differ in which features are supported. To use MSRs, the MSR address is loaded into the ECX register and an instruction (RDMSR or WRMSR) is executed to transfer 64 bits of data between the selected MSR and EDX:EAX. The table below shows the MSRs supported by each processor.

Model Specific Register	MSR Address	Processor Support		
		IBM 6x86MX[5]	AMD K6[4]	Intel P55C[2,3]
Machine Check Address Register (MCAR)	00h	No	Yes	Yes
Machine Check Type Register (MCTR)	01h	No	Yes	Yes
TR1 (parity reversal register)	02h	No	No	Yes
Scratch Pad RAM (cache line data)	03h	Yes	No	No
Scratch Pad RAM (cache line address)	04h	Yes	No	No
Scratch Pad RAM (cache line control) or TR3 (cache test data)	05h	Yes Scratch Pad RAM TR3 access via MOV	No	Yes TR3
TR4 (cache test tag)	06h	No TR4 access via MOV	No	Yes

Table 4: Model Specific Registers

TR5 (cache test control)	07h	No TR5 access via MOV	No	Yes
TR6 (TLB test linear address)	08h	No TR6 access via MOV	No	Yes
TR7 (TLB test control & phys addr 31-12)	09h	No TR7 access via MOV	No	Yes
TR9 (BTB test tag)	0Bh	No	No	Yes
TR10 (BTB test target)	0Ch	No	No	Yes
TR11 (BTB test control)	0Dh	No	No	Yes
TR12 (core feature disable)	0Eh	No	Yes	Yes
Time Stamp Counter	10h	Yes	Yes	Yes
Counter Event Selection and Control Register	11h	Yes	No	Yes
Performance Counter #0	12h	Yes	No	Yes
Performance Counter #1	13h	Yes	No	Yes
Extended Feature Enable Register (EFER)	C0000080h	No	Yes	No
SYSCALL Target Address Register (STAR)	C0000081h	No	Yes	No
Write Handling Control Register (WHCR)	C0000082h	No Write Alloc via CCR5	Yes	No

Table 4: Model Specific Registers

Note that the IBM 6x86MX processor is the only processor that supports Scratch Pad RAM, otherwise known as "cache line locking". This feature allows a set of lines in the L1 cache to be defined as private cpu memory to store critical data or code. Locked lines do not go through cache coherency protocol so they are not subject to snooping, invalidate, write-back, flush or replacement.

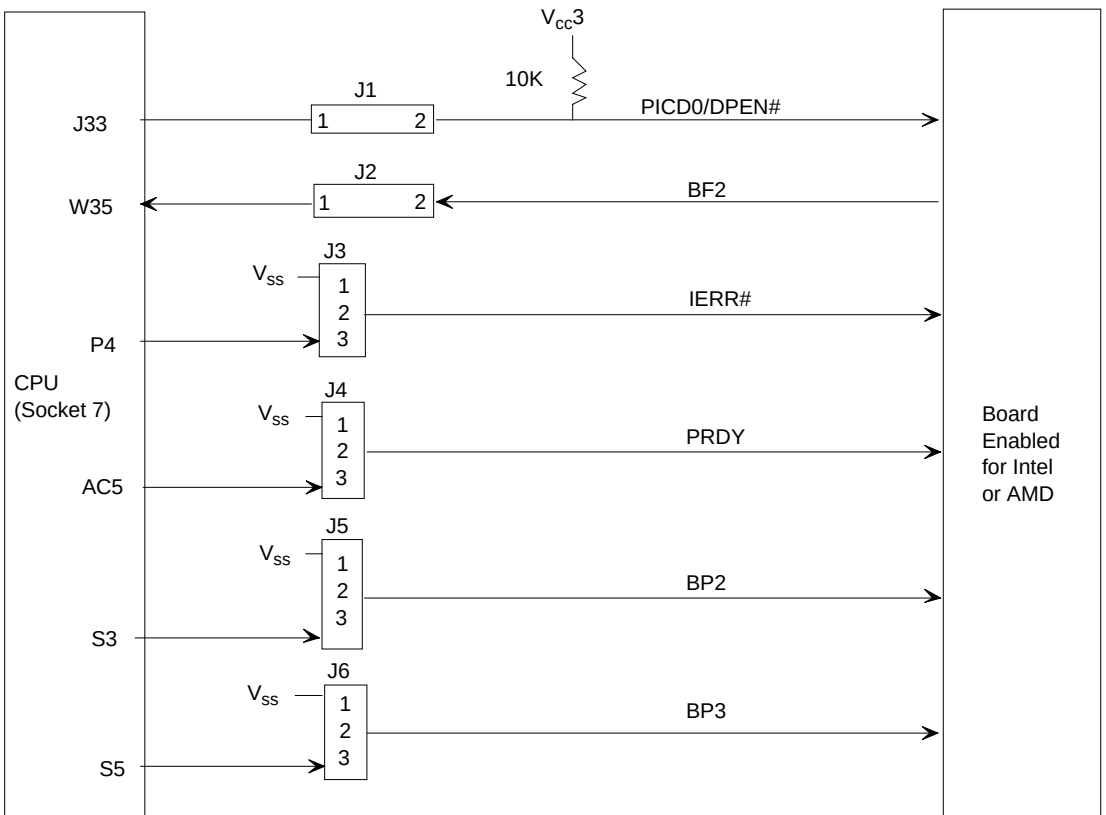
All three processors support the Time Stamp Counter at MSR 10h. The IBM 6x86MX and Intel P55C processors also support the RDTSC instruction to access this same data. The AMD K6 processor does not support Performance Monitor Counters (MSR 11-13 or the RDPMC instruction) which the IBM 6x86MX and Intel P55C processors use to monitor internal core events.

To test the L1 cache, the Intel P55C processor supports TR3-TR5 at MSR addresses 05h-07h. The IBM 6x86MX processor supports TR3-TR5 in a similar manner using the MOV instruction. The AMD K6 processor does not support TR3-TR5.

The Translation Lookaside Buffer is tested using TR6-TR7 on the Intel P55C and the IBM 6x86MX processors. The Intel P55C processor implements these registers at MSR addresses 08h-09h. The IBM 6x86MX processor supports TR6-TR7 in a similar manner through the MOV instruction. AMD K6 does not support TR6-TR7.

Both the IBM 6x86MX and AMD K6 processors support the Write Allocate feature. When this feature is enabled the processor allocates a new line in the L1 cache whenever it has a pending memory write cycle and the line does not exist in the cache. This feature is enabled on the IBM 6x86MX processor by writing a configuration bit (CCR5 bit 0). On the AMD K6 processor, this feature is controlled through MSR C0000082h.

Figure 1. Common Socket Specification



Jumper Settings

Jumper	M2	P55C	K6
J1	Open	1-2	Open
J2	Open	Don't care	1-2
J3	1-2	2-3	1-2
J4	1-2	2-3	1-2
J5	1-2	2-3	1-2
J6	1-2	2-3	1-2

Conclusion

It is fairly simple to modify Socket 7 boards to support the IBM 6x86MX processor. With a few jumper switches to handle pin differences and BIOS changes to enable the IBM 6x86MX processor features, boards can fully support the IBM 6x86MX processor. There are some behavioral differences between the processors discussed in this application note which software writers and chipset designers must consider as they develop their products.

References

1. *IBM 6x86MX Microprocessor Databook*, IBM Corporation, 1997.
2. *Pentium Processor with MMX Technology.* Intel Corporation, 1997.
3. *Pentium Processor Family Developer's Manual*, Volume 3: Architecture and Programming Manual. Intel Corporation, 1995.
4. *Pentium Processor Family Developer's Manual*. Intel Corporation, 1997.
5. *AMD-K6 MMX Processor Data Sheet*. Advanced Micro Devices, 1997.

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