SPECIAL ENVIRONMENT PENTIUM® PROCESSOR WITH VOLTAGE REDUCTION TECHNOLOGY

- **32-Bit CPU with 64-Bit Data Bus**
- **Superscalar Architecture**
    - **Two Pipelined Integer Units Are Capable of 2 Instructions/Clock**
    - **Pipelined Floating Point Unit**
- **Separate Code and Data Caches**
    - **8K Code, 8K Writeback Data**
    - **MESI Cache Protocol**
- **Advanced Design Features**
    - **Branch Prediction**
    - **Virtual Mode Extensions**
- **Compatible with Large Intel Architecture Software Base**
- **Low Voltage BiCMOS Silicon Technology**
- **4M Pages for Increased TLB Hit Rate**

- **IEEE 1149.1 Boundary Scan**
- **Internal Error Detection Features**
- **SL Enhanced Power Management Features**
    - **System Management Mode**
    - **Clock Control**
- **Voltage Reduction Technology**
    - **2.9V V_{CC} for Core Supply**
    - **3.3V V_{CC} for I/O Buffer Supply**
- **Fractional Bus Operation**
    - **133-MHz Core / 66-MHz Bus**
    - **120-MHz Core / 60-MHz Bus**
    - **100-MHz Core / 50-MHz Bus**
- **3 QML Qualified Temperature Ranges**
    - **SE1/Q (-55°C to +125°C)**
    - **SE3/Q (-40°C to +110°C)**
    - **SE5/Q (-40°C to +85°C)**

The Special Environment Pentium® processor provides high performance processing to harsh environment applications. By maintaining binary code compatibility with previous Intel Architecture processors, the Pentium processor supports cost-efficient performance upgrades. The processor's superscalar architecture offers superior processing with the ability to execute two instructions per clock cycle. Branch prediction and on-chip cache memory also increase processing performance. Separate code and data caches reduce memory conflicts while remaining software-transparent. The pipelined floating-point unit delivers workstation-level computing.

Built on Intel's advanced low voltage BiCMOS silicon technology, the Special Environment Pentium processor has 3.3 million transistors. The processor supports low power features such as system management mode (SMM), clock control, and voltage reduction technology (VRT).

September, 1996 Order Number: 271352-003

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The Special Environment Pentium Processor may contain design defects or errors known as errata. Current characterized errata are available on request.

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SPECIAL ENVIRONMENT PENTIUM® PROCESSOR WITH VOLTAGE REDUCTION TECHNOLOGY

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1.0 INTRODUCTION

Intel is manufacturing a Special Environment version of the latest low power Pentium® processor. The Pentium processor with voltage reduction technology (VRT) allows the processor to "talk" to industry standard 3.3-volt components while its inner core, operating at 2.9 volts, consumes less power. The Special Environment Pentium processor is offered in a ceramic Staggered Pin Grid Array (SPGA) package.

This document should be used in conjunction with the following related Pentium processor documents.

- *Pentium® Processor Family Developer's Manual, Volume 1: Pentium® Processors* (Order #241428)
- *Pentium® Processor Family Developer's Manual, Volume 3: Architecture and Programming Manual* (Order #241430)
- *Pentium® Processor Specification Update* (Order #242480)

2.0 MICROPROCESSOR ARCHITECTURE OVERVIEW

The Special Environment Pentium processor extends the Intel Pentium microprocessor family while remaining compatible with a host of other Intel products.

The Pentium processor family consists of the Special Environment and Mobile Pentium processors with voltage reduction technology (described in this document), the original mobile Pentium processor, and the various desktop Pentium processors. "Pentium processor" will be used in this document to refer to the entire Pentium processor family in general.

The Special Environment Pentium processor family architecture contains all of the features of the Intel486™ CPU family. In addition, it provides significant enhancements and additions, including the following:

- Superscalar Architecture
- Dynamic Branch Prediction
- Pipelined Floating-Point Unit
- Improved Instruction Execution Time
- Separate 8 K Code and 8 K Data Caches
- Writeback MESI Protocol in the Data Cache
- 64-Bit Data Bus
- Bus Cycle Pipelining
- Address Parity
- Internal Parity Checking
- Execution Tracing
- Performance Monitoring
- IEEE 1149.1 Boundary Scan
- System Management Mode
- Virtual Mode Extensions
- Voltage Reduction Technology
- SL Power Management Features

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2.1 Special Environment Pentium Processor Family Architecture

The Pentium processor instruction set includes the complete Intel486 CPU family instruction set with extensions for additional functionality. All application software written for the Intel386™ and Intel486 family microprocessors will run on Pentium processors without modification. In addition, the on-chip memory management unit (MMU) is completely compatible with the Intel386 family and Intel486 family of CPUs.

To increase performance, Pentium processors implement many architectural enhancements. Two instruction pipelines and the floating-point unit are capable of independent operation. Each pipeline issues frequently used instructions in a single clock. Together, the dual pipes can issue two integer instructions in one clock, or one floating-point instruction (under certain circumstances, two floating-point instructions) in one clock.

To support dynamic branch prediction, the processor uses two prefetch buffers. One buffer prefetches code in a linear fashion. The other prefetches code according to the Branch Target Buffer (BTB). Instruction code is almost always prefetched before it is needed for execution.

The processor's floating-point unit has been completely redesigned. Faster algorithms provide up to ten times the Intel486 CPU floating-point performance for common operations including add, multiply and load. Many applications can achieve five times the performance or more with instruction scheduling and overlapped (pipelined) execution.

To meet performance goals, Pentium processors integrate separate code and data caches on-chip. Each 8 Kbyte cache is 2-way set associative with a 32-byte line size. To translate linear addresses to physical addresses, each cache has a dedicated Translation Lookaside Buffer (TLB). The data cache is configurable to be writeback or writethrough on a line-by-line basis and follows the MESI protocol. The data cache tags are triple ported to support two data transfers and an inquire cycle in the same clock. The code cache is an inherently write-protected cache. The code cache tags are also triple ported to support snooping and split line accesses. Individual pages can be configured as cacheable or non-cacheable by software or hardware. Furthermore, the caches can be enabled or disabled by software or hardware.

Burst read and burst writeback cycles are supported by the Pentium processor through its 64-bit data bus. In addition, bus cycle pipelining has been added to allow two bus cycles to be in progress simultaneously. The Pentium processor's MMU contains optional extensions to the architecture which allow 2-Mbyte and 4-Mbyte page sizes.

Pentium processors have significant data integrity and error detection capabilities. Data parity checking is supported on a byte-by-byte basis. Address parity checking and internal parity checking features have been added along with a new exception, the machine check exception.

As more functions are integrated on-chip, the complexity of board level testing is increased. To address this, Pentium processors have increased test and debug capability. In addition to implementing IEEE Boundary Scan (Standard 1149.1) circuitry, Pentium processors specify four breakpoint pins that correspond to each of the debug registers and externally indicate a breakpoint match. When an instruction has completed execution or a branch has been taken, execution tracing provides external indications to the debugger.

System Management Mode (SMM) has been implemented with some extensions to the SMM architecture. Enhancements to the virtual 8086 mode increase performance by reducing the number of times it is necessary to trap a virtual mode monitor.

2.2 Functional Block Diagram

The block diagram (Figure 1) shows the two instruction pipelines, the "u" pipe and "v" pipe. The u-pipe can execute all integer and floating-point instructions. The v-pipe can execute simple integer instructions and the FXCH floating-point instructions.

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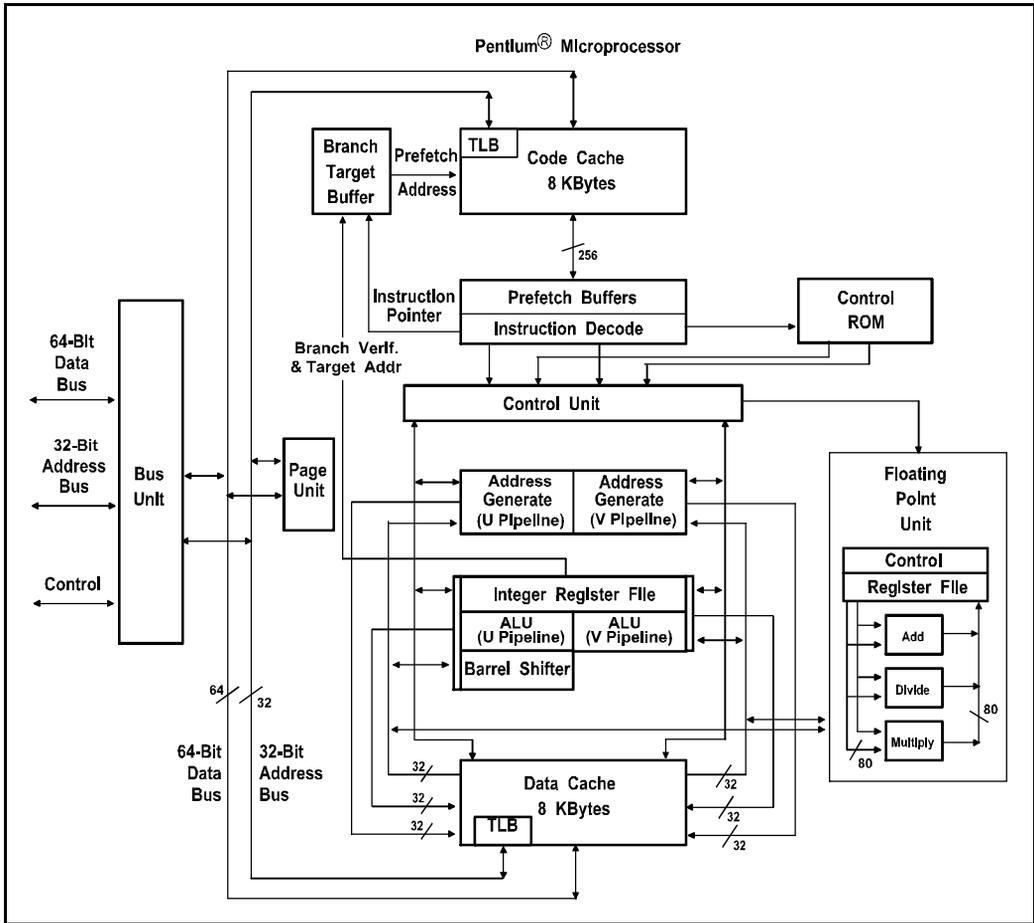
Figure 1. Pentium® Processor Block Diagram

The data cache has two ports, one for each of the two pipes (the tags are triple ported to allow simultaneous inquire cycles). The data cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to the physical addresses.

The code cache, branch target buffer, and prefetch buffers are responsible for providing raw instructions to the execution units. Instructions are fetched from the code cache or from the external bus. The code cache TLB translates linear addresses to physical addresses used by the code cache. Branch addresses are stored by the branch target buffer.

The decode unit decodes the prefetched instructions. The control ROM contains the microcode which controls the sequence of operations. The control ROM unit has direct control over both pipelines.

Pentium processors contain a pipelined floating-point unit that provides a significant floating-point performance advantage over previous generations of processors.

The architectural features introduced in this section are more fully described in *the Pentium® Processor Family Developer's Manual, Volume 3* (Order #241430).

The Special Environment Pentium processor implements all the advanced features of the 3.3 V Pentium processor excluding the following:

• Dual Processing (DP) Support
• Advanced Programmable Interrupt Controller (APIC)
• Master/Checker Functional Redundancy Support
• OverDrive® Processor Support

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3.0   PINOUT

3.1   Special Environment Pentium Processor Pinout
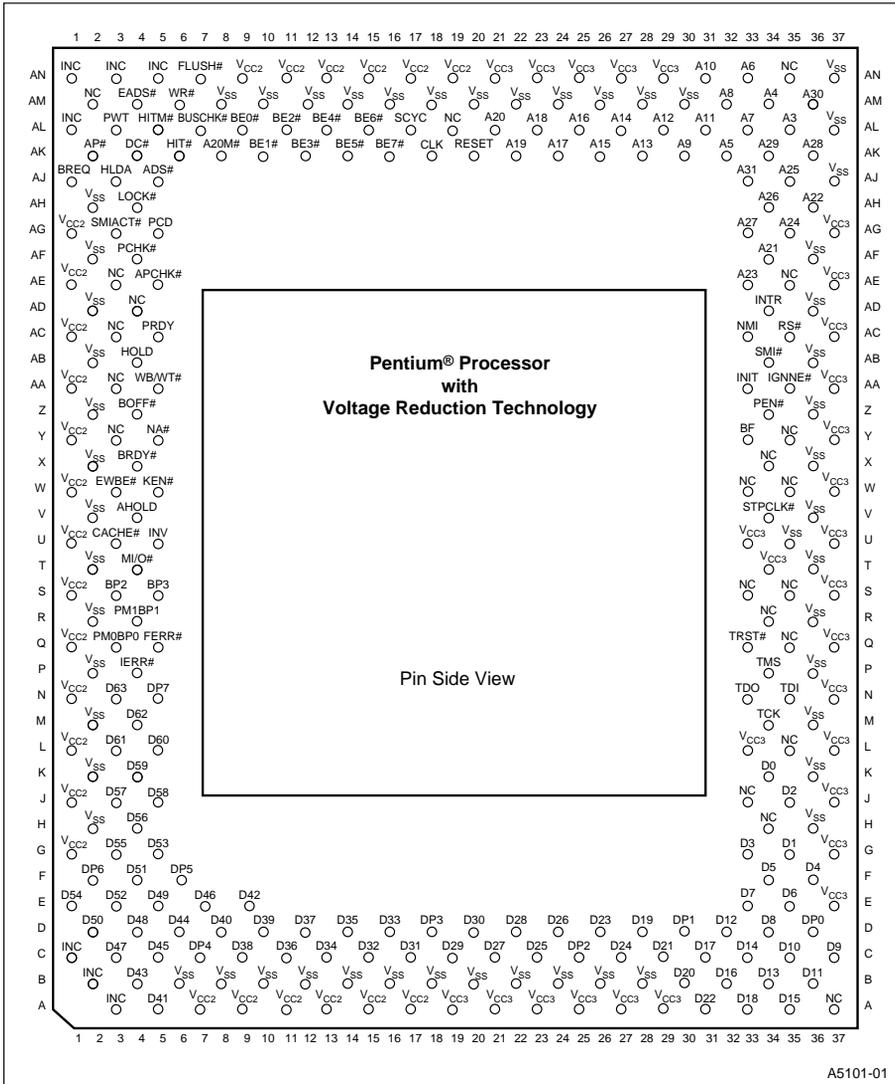
Figure 2. SPGA Pentium® Processor with Voltage Reduction Technology Pinout—Pin Side View

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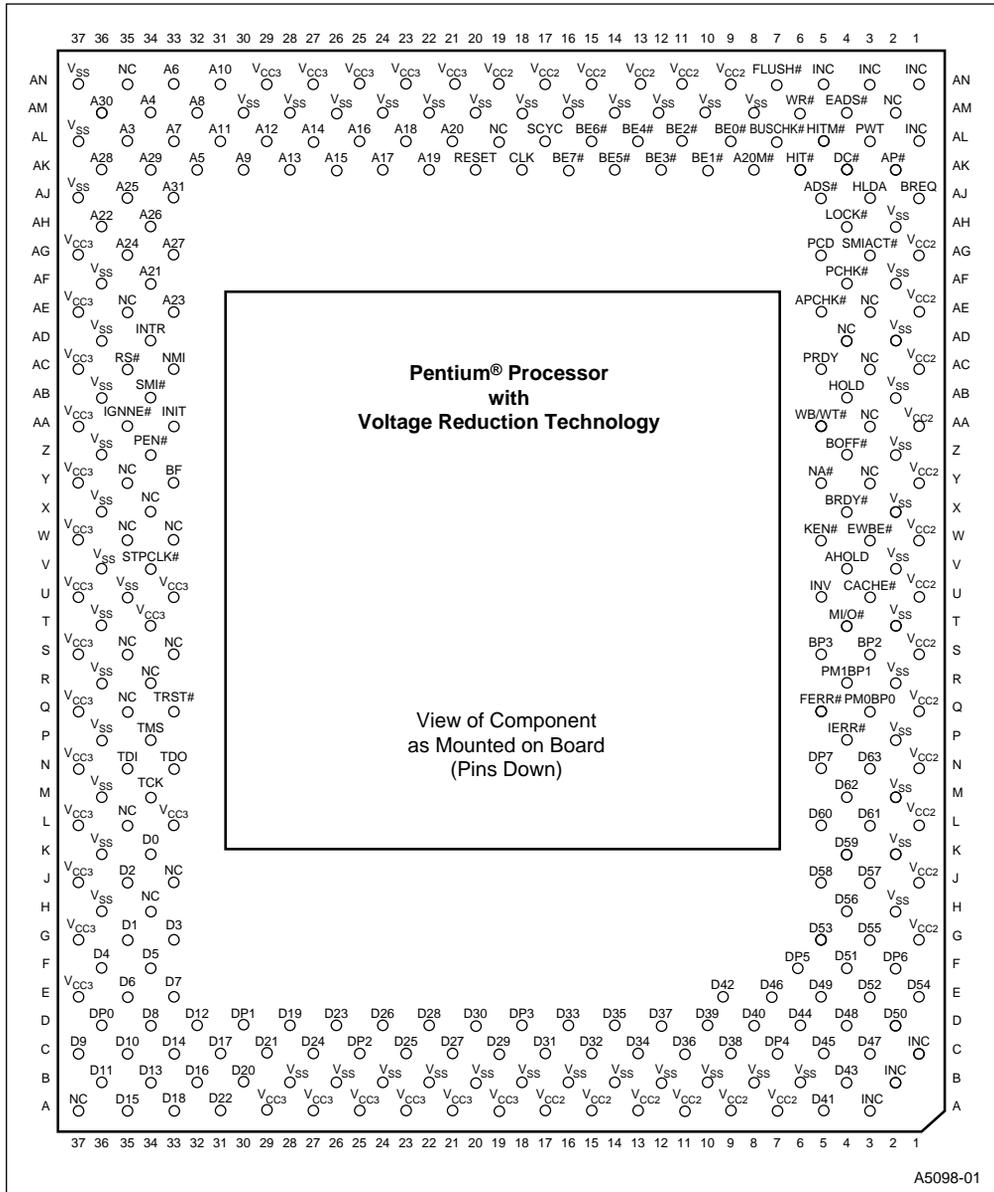
Figure 3. SPGA Pentium® Processor with Voltage Reduction Technology Pinout—Top Side View

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Table 1. Pin Cross Reference by Pin Name

Address									
Name	**Location**	**Name**	**Location**	**Name**	**Location**	**Name**	**Location**	**Name**	**Location**
A3	AL35	A9	AK30	A15	AK26	A21	AF34	A27	AG33
A4	AM34	A10	AN31	A16	AL25	A22	AH36	A28	AK36
A5	AK32	A11	AL31	A17	AK24	A23	AE33	A29	AK34
A6	AN33	A12	AL29	A18	AL23	A24	AG35	A30	AM36
A7	AL33	A13	AK28	A19	AK22	A25	AJ35	A31	AJ33
A8	AM32	A14	AL27	A20	AL21	A26	AH34		

Data									
D0	K34	D13	B34	D26	D24	D39	D10	D52	E03
D1	G35	D14	C33	D27	C21	D40	D08	D53	G05
D2	J35	D15	A35	D28	D22	D41	A05	D54	E01
D3	G33	D16	B32	D29	C19	D42	E09	D55	G03
D4	F36	D17	C31	D30	D20	D43	B04	D56	H04
D5	F34	D18	A33	D31	C17	D44	D06	D57	J03
D6	E35	D19	D28	D32	C15	D45	C05	D58	J05
D7	E33	D20	B30	D33	D16	D46	E07	D59	K04
D8	D34	D21	C29	D34	C13	D47	C03	D60	L05
D9	C37	D22	A31	D35	D14	D48	D04	D61	L03
D10	C35	D23	D26	D36	C11	D49	E05	D62	M04
D11	B36	D24	C27	D37	D12	D50	D02	D63	N03
D12	D32	D25	C23	D38	C09	D51	F04		

Control							
Name	**Location**	**Name**	**Location**	**Name**	**Location**	**Name**	**Name**
A20M#	AK08	BREQ	AJ01	FLUSH#	AN07	PEN#	Z34
ADS#	AJ05	BUSCHK#	AL07	HIT#	AK06	PM0/BP0	Q03
AHOLD	V04	CACHE#	U03	HITM#	AL05	PM1/BP1	R04
AP	AK02	D/C#	AK04	HLDA	AJ03	PRDY	AC05
APCHK#	AE05	DP0	D36	HOLD	AB04	PWT	AL03
BE0#	AL09	DP1	D30	IERR#	P04	R/S#	AC35
BE1#	AK10	DP2	C25	IGNNE#	AA35	RESET	AK20
BE2#	AL11	DP3	D18	INIT	AA33	SCYC	AL17
BE3#	AK12	DP4	C07	INTR/LINT0	AD34	SMI#	AB34
BE4#	AL13	DP5	F06	INV	U05	SMIACT#	AG03

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Table 1. Pin Cross Reference by Pin Name (Continued)

Name	Location	Name	Location	Name	Location	Name	Location
BE5#	AK14	DP6	F02	KEN#	W05	TCK	M34
BE6#	AL15	DP7	N05	LOCK#	AH04	TDI	N35
BE7#	AK16	EADS#	AM04	M/IO#	T04	TDO	N33
BOFF#	Z04	EWBE#	W03	NA#	Y05	TMS	P34
BP2	S03	FERR#	Q05	NMI/LINT1	AC33	TRST#	Q33
BP3	S05	DP6	F02	PCD	AG05	W/R#	AM06
BRDY#	X04	DP7	N05	PCHK#	AF04	WB/WT#	AA05
BE7#	AK16			M/IO#	T04	TMS	P34
BOFF#	Z04			NA#	Y05	TRST#	Q33
Clock Control							
CLK	AK18	BF	Y33	STPCLK#	V34		
V$_{CC}$2[1]							
A17		A07		Q01		AA01		AN11
A15		G01		S01		AC01		AN13
A13		J01		U01		AE01		AN15
A11		L01		W01		AG01		AN17
A09		N01		Y01		AN09		AN19
V$_{CC}$3							
A19		AA37		AN25		L33		U33
A21		AC37		AN27		L37		U37
A23		AE37		AN29		N37		W37
A25		AG37		E37		Q37		Y37
A27		AN21		G37		S37		
A29		AN23		J37		T34		
NC[2]							
A37		AE03		AN35		Q35		W33
AA03		AE35		H34		R34		W35
AC03		AL19		J33		S33		Y03
AD04		AM02		L35		S35		Y35

NOTES:

1. These V$_{CC}$2 pins are 3.3 V V$_{CC}$ pins for the SPGA 3.3 V Pentium processor. For the SPGA Pentium processor with voltage reduction technology, these pins are 2.9 V V$_{CC}$2 supplies for the SPGA core.

2. NC pins should be left unconnected. Connection of these pins may result in component failure or incompatibility with processor steppings.

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3.2   Design Notes

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to $V_{CC}3$. Unused active HIGH inputs should be connected to GND (V_{SS}).

No Connect (NC) pins must remain unconnected. Connection of NC pins may result in component failure or incompatibility with processor steppings.

3.3   Quick Pin Reference

This section gives a brief functional description of each of the pins. **Note that all input pins must meet their AC/DC specifications to guarantee proper functional behavior**.

The # symbol at the end of a signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage. When a # symbol is not present after the signal name, the signal is active, or asserted, at the high voltage level.

For detailed pin descriptions, see the *Pentium® Processor Family Developer's Manual, Volume 1: Pentium® Processors* (Order #241428).

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Table 2. Quick Pin Reference

Symbol	Type	Name and Function
A20M#	I	When the **address bit 20 mask** pin is asserted, the Pentium® processor emulates the address wraparound at 1 Mbyte which occurs on the 8086. When A20M# is asserted, the processor masks physical address bit 20 (A20) before performing a lookup to the internal caches or driving a memory cycle on the bus. The effect of A20M# is undefined in protected mode. A20M# must be asserted only when the processor is in real mode.
A31-A3	I/O	As outputs, the **address** lines of the processor along with the byte enables define the physical area of memory or I/O accessed. The external system drives the inquire address to the processor on A31-A5.
ADS#	O	The **address status** indicates that a new valid bus cycle is currently being driven by the processor.
AHOLD	I	In response to the assertion of **address hold**, the processor will stop driving the address lines (A31-A3), and AP in the next clock. The rest of the bus will remain active so data can be returned or driven for previously issued bus cycles.
AP	I/O	**Address parity** is driven by the processor with even parity information on all processor generated cycles in the same clock that the address is driven. Even parity must be driven back to the processor during inquire cycles on this pin in the same clock as EADS# to ensure that correct parity check status is indicated.
APCHK#	O	The **address parity check** status pin is asserted two clocks after EADS# is sampled active if the processor has detected a parity error on the address bus during inquire cycles. APCHK# will remain active for one clock each time a parity error is detected.
BE7#-BE5# BE4#-BE0#	O I/O	The **byte enable** pins are used to determine which bytes must be written to external memory, or which bytes were requested by the CPU for the current cycle. The byte enables are driven in the same clock as the address lines (A31-3).

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Table 2. Quick Pin Reference (Continued)

Symbol	Type	Name and Function
BF	I	**Bus Frequency** determines the bus-to-core ratio. BF is sampled at RESET, and cannot be changed until another non-warm (1 ms) assertion of RESET. Additionally, BF must not change values while RESET is active. For proper operation of the processor, this pin should be strapped high or low. When BF is strapped to V_{CC}, the processor will operate at a 2/3 bus/core frequency ratio. When BF is strapped to V_{SS}, the processor will operate to a 1/2 bus/core frequency ratio. If BF is left floating, the processor defaults to a 2/3 bus/core ratio.
BOFF#	I	The **backoff** input is used to abort all outstanding bus cycles that have not yet completed. In response to BOFF#, the processor will float all pins normally floated during bus hold in the next clock. The processor remains in bus hold until BOFF# is negated, at which time the Pentium processor restarts the aborted bus cycle(s) in their entirety.
BP[3:2] PM/BP[1:0]	O	The **breakpoint** pins (BP3-0) correspond to the debug registers, DR3-DR0. These pins externally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches. BP1 and BP0 are multiplexed with the **performance monitoring** pins (PM1 and PM0). The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
BRDY#	I	The **burst ready** input indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted the processor data in response to a write request. This signal is sampled in the T2, T12 and T2P bus states. BRDY# is sampled at RESET to appropriately configure the I/O buffer sizes.
BREQ	O	The **bus request** output indicates to the external system that the processor has internally generated a bus request. This signal is always driven whether or not the processor is driving its bus.
BUSCHK#	I	The **bus check** input allows the system to signal an unsuccessful completion of a bus cycle. If this pin is sampled active, the processor will latch the address and control signals in the machine check registers. If, in addition, the MCE bit in CR4 is set, the processor will vector to the machine check exception. BUSCHK# must be held inactive (high) at the falling edge of RESET.
CACHE#	O	For processor-initiated cycles, the **cache** pin indicates internal cacheability of the cycle (if a read), and indicates a burst writeback cycle (if a write). If this pin is driven inactive during a read cycle, the processor will not cache the returned data, regardless of the state of the KEN# pin. This pin is also used to determine the cycle length (number of transfers in the cycle).
CLK	I	The **clock** input provides the fundamental timing for the processor. Its frequency is the operating frequency of the processor external bus and requires TTL levels. All external timing parameters except TDI, TDO, TMS, and TRST# are specified with respect to the rising edge of CLK. NOTE: It is recommended that CLK begin 150 ms after V_{CC} reaches its proper operating level. This recommendation is only to assure the long term reliability of the device.

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Table 2. Quick Pin Reference (Continued)

Symbol	Type	Name and Function
D/C#	O	The **data/code** output is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.
D63-D0	I/O	These are the 64 **data lines** for the processor. Lines D7-D0 define the least significant byte of the data bus; lines D63-D56 define the most significant byte of the data bus. When the CPU is driving the data lines, they are driven during the T2, T12 or T2P clocks for that cycle. During reads, the CPU samples the data bus when BRDY# is returned.
DP7-DP0	I/O	These are the **data parity** pins for the processor. There is one for each byte of the data bus. They are driven by the processor with even parity information on writes in the same clock as write data. Even parity information must be driven back to the Pentium processor with voltage reduction technology on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the processor. DP7 applies to D63-D56; DP0 applies to D7-D0.
EADS#	I	This signal indicates that a valid **external address** has been driven onto the processor address pins to be used for an inquire cycle.
EWBE#	I	The **external write buffer empty** input, when inactive (high), indicates that a write cycle is pending in the external system. When the processor generates a write and EWBE# is sampled inactive, the processor will hold off all subsequent writes to all E- or M-state lines in the data cache until all write cycles have completed, as indicated by EWBE# being active.
FERR#	O	The **floating-point error** pin is driven active when an unmasked floating-point error occurs. FERR# is similar to the ERROR# pin on the Intel387© math coprocessor. FERR# is included for compatibility with systems using DOS-type floating-point error reporting.
FLUSH#	I	When asserted, the **cache flush** input forces the processor to write back all modified lines in the data cache and invalidate its internal caches. A Flush Acknowledge special cycle will be generated by the processor indicating completion of the writeback and invalidation. NOTE: If FLUSH# is sampled low when RESET transitions from high to low, tristate test mode is entered.
HIT#	O	The **hit** indication is driven to reflect the outcome of an inquire cycle. If an inquire cycle hits a valid line in either the data or instruction cache, this pin is asserted two clocks after EADS# is sampled asserted. If the inquire cycle misses the cache, this pin is negated two clocks after EADS#. This pin changes its value only as a result of an inquire cycle and retains its value between the cycles.
HITM#	O	The **hit to a modified line** output is driven to reflect the outcome of an inquire cycle. It is asserted after inquire cycles which resulted in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.

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Table 2. Quick Pin Reference (Continued)

Symbol	Type	Name and Function
HLDA	O	The **bus hold acknowledge** pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that the processor has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA will be driven inactive and the processor will resume driving the bus. If the processor has a bus cycle pending, it will be driven in the same clock that HLDA is de-asserted.
HOLD	I	In response to the **bus hold request**, the processor will float most of its output and input/output pins and assert HLDA after completing all outstanding bus cycles. The processor will maintain its bus in this state until HOLD is de-asserted. HOLD is not recognized during LOCK cycles. The processor will recognize HOLD during reset.
IERR#	O	The **internal error** pin is used to indicate internal parity errors. If a parity error occurs on a read from an internal array, the processor will assert the IERR# pin for one clock and then shutdown.
IGNNE#	I	This is the **ignore numeric error** input. This pin has no effect when the NE bit in CR0 is set to 1. When the CR0.NE bit is 0, and the IGNNE# pin is asserted, the processor will ignore any pending unmasked numeric exception and continue executing floating-point instructions for the entire duration that this pin is asserted. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one of FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the processor will execute the instruction in spite of the pending exception. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one other than FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the processor will stop execution and wait for an external interrupt.
INIT	I	The processor **initialization** input pin forces the processor to begin execution in a known state. The processor state after INIT is the same as the state after RESET except that the internal caches, write buffers, and floating-point registers retain the values they had prior to INIT. INIT may NOT be used in lieu of RESET after power up.
		If INIT is sampled high when RESET transitions from high to low, the processor will perform built-in self test prior to the start of program execution.
INTR	I	An active **maskable interrupt** input indicates that an external interrupt has been generated. If the IF bit in the EFLAGS register is set, the processor will generate two locked interrupt acknowledge bus cycles and vector to an interrupt handler after the current instruction execution is completed. INTR must remain active until the first interrupt acknowledge cycle is generated to assure that the interrupt is recognized.
INV	I	The **invalidation** input determines the final cache line state (S or I) in case of an inquire cycle hit. It is sampled together with the address for the inquire cycle in the clock EADS# is sampled active.
KEN#	I	The **cache enable** pin is used to determine whether the current cycle is cacheable or not and is consequently used to determine cycle length. When the processor generates a cycle that can be cached (CACHE# asserted) and KEN# is active, the cycle will be transformed into a burst line fill cycle.

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Table 2. Quick Pin Reference (Continued)

Symbol	Type	Name and Function
LOCK#	O	The **bus lock** pin indicates that the current bus cycle is locked. The processor will not allow a bus hold when LOCK# is asserted (but AHOLD and BOFF# are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the BRDY# is returned for the last locked bus cycle. LOCK# is guaranteed to be de-asserted for at least one clock between back-to-back locked cycles.
M/IO#	O	The **memory/input-output** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles.
NA#	I	An active **next address** input indicates that the external memory system is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The processor will issue ADS# for a pending cycle two clocks after NA# is asserted. The processor supports up to two outstanding bus cycles.
NMI	I	The **non-maskable interrupt** request signal indicates that an external non-maskable interrupt has been generated.
PCD	O	The **page cache disable** pin reflects the state of the PCD bit in CR3; Page Directory Entry or Page Table Entry. The purpose of PCD is to provide an external cacheability indication on a page-by-page basis.
PCHK#	O	The **parity check** output indicates the result of a parity check on a data read. It is driven with parity status two clocks after BRDY# is returned. PCHK# remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned.
PEN#	I	The **parity enable** input (along with CR4.MCE) determines whether a machine check exception will be taken as a result of a data parity error on a read cycle. If this pin is sampled active in the clock, a data parity error is detected. The processor will latch the address and control signals of the cycle with the parity error in the machine check registers. If, in addition, the machine check enable bit in CR4 is set to "1", the processor will vector to the machine check exception before the beginning of the next instruction.
PM/BP[1:0]	O	These pins function as part of the performance monitoring feature. The breakpoint 1-0 pins are multiplexed with the **performance monitoring 1-0** pins. The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
PRDY	O	The **probe ready** output pin indicates that the processor has stopped normal execution in response to the R/S# pin going active or Probe Mode being entered.
PWT	O	The **page writethrough** pin reflects the state of the PWT bit in CR3, the page directory entry, or the page table entry. The PWT pin is used to provide an external writeback indication on a page-by-page basis.
R/S#	I	The **run / stop** input is an asynchronous, edge-sensitive interrupt used to stop the normal execution of the processor and place it into an idle state. A high to low transition on the R/S# pin will interrupt the processor and cause it to stop execution at the next instruction boundary.

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Table 2. Quick Pin Reference (Continued)

Symbol	Type	Name and Function
RESET	I	**RESET** forces the processor to begin execution at a known state. All the processor internal caches will be invalidated upon the RESET. Modified lines in the data cache are not written back. FLUSH# and INIT are sampled when RESET transitions from high to low to determine if tristate test mode will be entered or if BIST will be run. BRDY# is sampled when RESET transitions from high to low to determine the I/O buffer size.
SCYC	O	The **split cycle** output is asserted during misaligned LOCKed transfers to indicate that more than two cycles will be locked together. This signal is defined for locked cycles only. It is undefined for cycles which are not locked.
SMI#	I	The **system management interrupt** causes a system management interrupt request to be latched internally. When the latched SMI# is recognized on an instruction boundary, the processor enters System Management Mode.
SMIACT#	O	An active **system management interrupt active** output indicates that the processor is operating in System Management Mode.
STPCLK#	I	Assertion of the **stop clock** input signifies a request to stop the internal clock of the Pentium processor with voltage reduction technology thereby causing the core to consume less power. When the CPU recognizes STPCLK#, the processor will stop execution on the next instruction boundary, unless superseded by a higher priority interrupt, and generate a Stop Grant Acknowledge cycle. When STPCLK# is asserted, the processor will still respond to external snoop requests.
TCK	I	The **testability clock** input provides the clocking function for the processor boundary scan in accordance with the IEEE Boundary Scan interface (Standard 1149.1). It is used to clock state information and data into and out of the processor during boundary scan.
TDI	I	The **test data input** is a serial input for the test logic. TAP instructions and data are shifted into the processor on the TDI pin on the rising edge of TCK when the TAP controller is in an appropriate state.
TDO	O	The **test data output** is a serial output of the test logic. TAP instructions and data are shifted out of the processor on the TDO pin on TCK's falling edge when the TAP controller is in an appropriate state.
TMS	I	The value of the **test mode select** input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes.
TRST#	I	When asserted, the **test reset** input allows the TAP controller to be asynchronously initialized.

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Table 2. Quick Pin Reference (Continued)

Symbol	Type	Name and Function
$V_{CC}2$	I	These pins are the 2.9 V power inputs to the Pentium processor with voltage reduction technology.
$V_{CC}3$	I	These pins are the 3.3 V power inputs to the Pentium processor with voltage reduction technology.
V_{SS}	I	These pins are the ground inputs to the Pentium processor with voltage reduction technology.
W/R#	O	**Write/read** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. W/R# distinguishes between write and read cycles.
WB/WT#	I	The **writeback/writethrough** input allows a data cache line to be defined as writeback or writethrough on a line-by-line basis. As a result, it determines whether a cache line is initially in the S or E state in the data cache.

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3.4   Pin Reference Tables

Table 3. Output Pins

Name	Active Level	When Floated
ADS#	Low	Bus Hold, BOFF#
APCHK#	Low	
BE7#-BE5#	Low	Bus Hold, BOFF#
BREQ	High	
CACHE#	Low	Bus Hold, BOFF#
FERR#	Low	
HIT#	Low	
HITM#	Low	
HLDA	High	
IERR#	Low	
LOCK#	Low	Bus Hold, BOFF#
M/IO#, D/C#, W/R#	n/a	Bus Hold, BOFF#
PCHK#	Low	
BP3-BP2, PM1/BP1, PM0/BP0	High	
PRDY	High	
PWT, PCD	High	Bus Hold, BOFF#
SCYC	High	Bus Hold, BOFF#
SMIACT#	Low	
TDO	n/a	All states except Shift-DR and Shift-IR

NOTE: All output and input/output pins are floated during tristate test mode (except TDO).

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Table 4. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal Resistor	Qualified
A20M#	Low	Asynchronous		
AHOLD	High	Synchronous		
BF	High	Synchronous/RESET	Pullup	
BOFF#	Low	Synchronous		
BRDY#	Low	Synchronous	Pullup	Bus State T2, T12, T2P
BUSCHK#	Low	Synchronous	Pullup	BRDY#
CLK	n/a			
EADS#	Low	Synchronous		
EWBE#	Low	Synchronous		BRDY#
FLUSH#	Low	Asynchronous		
HOLD	High	Synchronous		
IGNNE#	Low	Asynchronous		
INIT	High	Asynchronous		
INTR	High	Asynchronous		
INV	High	Synchronous		EADS#
KEN#	Low	Synchronous		First BRDY#/NA#
NA#	Low	Synchronous		Bus State T2,TD,T2P
NMI	High	Asynchronous		
PEN#	Low	Synchronous		BRDY#
R/S#	n/a	Asynchronous	Pullup	
RESET	High	Asynchronous		
SMI#	Low	Asynchronous	Pullup	
STPCLK#	Low	Asynchronous	Pullup	
TCK	n/a		Pullup	
TDI	n/a	Synchronous/TCK	Pullup	TCK
TMS	n/a	Synchronous/TCK	Pullup	TCK
TRST#	Low	Asynchronous	Pullup	
WB/WT#	n/a	Synchronous		First BRDY#/NA#

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Table 5. Input/Output Pins

Name	Active Level	When Floated[1]	Qualified (when an input)	Internal Resistor
A31-A3	n/a	Address Hold, Bus Hold, BOFF#	EADS#	
AP	n/a	Address Hold, Bus Hold, BOFF#	EADS#	
BE4#-BE0#	Low	Bus Hold, BOFF#	RESET	Pulldown[2]
D63-D0	n/a	Bus Hold, BOFF#	BRDY#	
DP7-DP0	n/a	Bus Hold, BOFF#	BRDY#	

NOTES:

1. All output and input/output pins are floated during tristate test mode (except TDO).

2. †BE3#-BE0# have pulldowns during RESET only.

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3.5   Pin Grouping According to Function

Table 6 organizes the pins with respect to their function.

Table 6. Pin Functional Grouping

Function	Pins
Clock	CLK
Initialization	RESET, INIT, BF
Address Bus	A31-A3, BE7# - BE0#
Address Mask	A20M#
Data Bus	D63-D0
Address Parity	AP, APCHK#
Data Parity	DP7-DP0, PCHK#, PEN#
Internal Parity Error	IERR#
System Error	BUSCHK#
Bus Cycle Definition	M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK#
Bus Control	ADS#, BRDY#, NA#
Page Cacheability	PCD, PWT
Cache Control	KEN#, WB/WT#
Cache Snooping/Consistency	AHOLD, EADS#, HIT#, HITM#, INV
Cache Flush	FLUSH#
Write Ordering	EWBE#
Bus Arbitration	BOFF#, BREQ, HOLD, HLDA
Interrupts	INTR, NMI
Floating-Point Error Reporting	FERR#, IGNNE#
System Management Mode	SMI#, SMIACT#
TAP Port	TCK, TMS, TDI, TDO, TRST#
Breakpoint/Performance Monitoring	PM0/BP0, PM1/BP1, BP3-BP2
Clock Control	STPCLK#
Probe Mode	R/S#, PRDY

ADVANCE INFORMATION

4.0 DC SPECIFICATIONS

4.1 Absolute Maximum Ratings

The Special Environment Pentium processor's absolute maximum ratings are listed in Table 7. The values are stress ratings only. Functional operation at the maximum ratings is not implied nor guaranteed. Functional operating conditions are given in the AC and DC specification tables.

Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields

Table 7. Absolute Maximum Ratings

Case temperature under bias	−65°C to 125°C
Storage temperature	−65°C to 150°C
2.9 V Supply voltage with respect to VSS	-0.5 V to +4.1 V
3 V Supply voltage with respect to VSS	-0.5 V to +4.6 V
3 V Only Buffer DC Input Voltage-0.5 V to $V_{CC}3$	-0.5 to $V_{CC}3$ + 0.5; not to exceed 4.6 V[2]
5 V Safe Buffer DC Input Voltage	-0.5 V to 6.5 V[1,3]

NOTES:

1. Applies to CLK.
2. Applies to all Special Environment Pentium processor inputs except CLK.
3. See Table 10.

NOTICE: This document contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.	***WARNING:** Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.2 Operating Conditions

Table 8. Operating Temperatures and Supply Voltages

Symbol	Description	Min	Max	Units
$V_{CC}3$	Digital 3.3 V Supply Voltage	3.135	3.465	V
$V_{CC}2$	Digital 2.9 V Supply Voltage	2.735	3.065	V
T_C (SE1/Q)	Case Temperature for SE1/Q Product	-55	+125	°C
T_C (SE3/Q)	Case Temperature for SE3/Q Product	-40	+110	°C
T_C (SE5/Q)	Case Temperature for SE5/Q Product	-40	+85	°C

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4.2.1　3.3 V Input and Output

The Special Environment Pentium processor operates at 2.9 V internally while the I/O interface operates at 3.3 V. However, the CLK input may be 3.3 V or 5 V. Since the 3.3 V (5 V safe) input levels defined in Table 10 are the same as 5 V TTL levels, the CLK input is compatible with existing 5 V clock drivers.

Inputs and outputs meet 3.3 V JEDEC standard levels. They are also TTL-compatible, although the input buffers cannot tolerate voltage swings above the $V_{IN}3$ maximum. If your system support components use TTL-compatible inputs, they will interface to the Special Environment Pentium processor without extra logic since the processor drives according to the 5 V TTL-specification (but not beyond 3.3 V).

For Special Environment Pentium processor inputs, the voltage must not exceed the 3.3 V $V_{IH}3$ maximum specification. System support components can consist of 3.3 V devices or open-collector devices. Since they typically meet 5 V TTL specifications, 3.3 V support components may interface to the processor. In an open-collector configuration, the external resistor may be biased with the CPU V_{CC}; as the CPU's V_{CC} changes from 5 V to 3.3 V, so does this signals maximum drive.

4.2.2　Power Sequencing

There is no specific sequence required for powering up or powering down the $V_{CC}2$ and $V_{CC}3$ power supplies. However, for compatibility with future processors, it is recommended that the $V_{CC}2$ and $V_{CC}3$ power supplies be either both on or both off within one second of each other.

4.2.3　Power and Ground

For clean on-chip power distribution, the Special Environment Pentium processor has 25 $V_{CC}2$ (2.9 V power), 28 $V_{CC}3$ (3.3 V power) and 53 V_{SS} (ground) inputs. Power and ground connections must be made to all external $V_{CC}2$, $V_{CC}3$ and V_{SS} pins. On the circuit board all $V_{CC}2$ pins must be connected to a 2.9 V V_{CC2} plane (or island) and all $V_{CC}3$ pins must be connected to a 3.3 V $V_{CC}3$ plane. All V_{SS} pins must be connected to a V_{SS} plane. Please refer to Table 1 for the list of $V_{CC}2$, $V_{CC}3$ and V_{SS} pins.

4.2.4　Connection Specifications

All NC pins must remain unconnected.

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to $V_{CC}3$. Unused active high inputs should be connected to ground.

4.2.5　Power Dissipation

The power dissipation specification in Table 12 is provided for design of thermal solutions during operation in a sustained maximum level. This is the worst-case power the device would dissipate in a system for a sustained period of time. This number is used for design of a thermal solution for the device.

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Table 9. SPGA 3.3 V DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL3}	Input Low Voltage	−0.3	0.8	V	TTL Level (3)
V_{IH3}	Input High Voltage	2.0	$V_{CC}3+0.3$	V	TTL Level (3)
V_{OL3}	Output Low Voltage		0.4	V	TTL Level (1) (3)
V_{OH3}	Output High Voltage	2.4		V	TTL Level (2) (3)
$I_{CC}2$	Power Supply Current from 2.9 V core supply		2085 2300 2575	mA	@100 MHz (4) (5) @120 MHz (4) @133 MHz (4)
$I_{CC}3$	Power Supply Current from 3.3 V I/O buffer supply		182 220 255	mA	@100 MHz (4) (5) @120 MHz (4) @133 MHz (4)

NOTES:

1. Parameter measured at 4 mA.

2. Parameter measured at 3 mA.

3. 3.3 V TTL levels apply to all signals except CLK.

4. This value should be used for power supply design. It was estimated for a worst-case instruction mix and V_{CC} + 165 mV. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes occurring during transitions from stop clock to full active modes. For more information, refer to section 5.1.

5. Guaranteed by design.

Table 10. 3.3 V (5 V Safe) DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IL}5$	Input Low Voltage	−0.3	0.8	V	TTL Level (1)
$V_{IH}5$	Input High Voltage	2.0	5.55	V	TTL Level (1)

NOTES:

1. Applies to CLK only.

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Table 11. Input and Output Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Capacitance		15	pF	(4)
C_O	Output Capacitance		20	pF	(4)
$C_{I/O}$	I/O Capacitance		25	pF	(4)
C_{CLK}	CLK Input Capacitance		15	pF	(4)
C_{TIN}	Test Input Capacitance		15	pF	(4)
C_{TOUT}	Test Output Capacitance		20	pF	(4)
C_{TCK}	Test Clock Capacitance		15	pF	(4)
I_{LI}	Input Leakage Current		±15	µA	$0 < V_{IN} < V_{CC}3$ (1)
I_{LO}	Output Leakage Current		±15	µA	$0 < V_{IN} < V_{CC}3$ (1)
I_{IH}	Input Leakage Current		200	µA	$V_{IN} = 2.4$ V (3)
I_{IL}	Input Leakage Current		−400	µA	$V_{IN} = 0.4$ V (2)

NOTES:

1. This parameter is for input without pull up or pull down.

2. This parameter is for input with pull up.

3. This parameter is for input with pull down.

4. Guaranteed by design.

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Table 12. Power Dissipation Requirements for Thermal Solution Design

Parameter	Maximum Typical[1]	Absolute Maximum[2]	Unit	Notes
Active Power Dissipation	4.6	5.7	Watts	@100 MHz (5)
	5.3	6.7		@120 MHz
	6.0	7.6		@133 MHz
Stop Grant and Auto Halt Powerdown Power Dissipation		1.2	Watts	@100 MHz (3) (5)
		1.2		@120 MHz (3)
		1.3		@133 MHz (3)
Stop Clock Power Dissipation	.02	0.05	Watts	(4)

NOTES:

1. The maximum typical power dissipation is the highest measurement taken while the processor ran application specific code. This value is highly dependent upon the specific system configuration. These measurements are taken with a 3.1 V core supply voltage and a 3.3 V peripheral supply voltage. Currently, this value is an estimate.
2. This is the absolute maximum power dissipation measured while the processor ran worse case test vectors in the lab.
3. Stop Grant/Auto Halt Powerdown Power Dissipation is determined by asserting the STPCLK# pin or executing the HALT instruction.
4. Stop Clock Power Dissipation is determined by asserting the STPCLK# pin and then removing the external CLK input.
5. Guaranteed by design.

5.0   AC Specifications

The Special Environment Pentium processor's AC specifications consist of setup times, hold times, and valid delays at 0 pF. All AC specifications are valid for $V_{CC}2$ = 2.9 V ± 165 mV and $V_{CC}3$ = 3.3 V ± 165 mV.

5.1   Decoupling Recommendations

Transient power surges can occur as the processor is executing instruction sequences or driving large loads. To mitigate these high frequency transients, liberal high frequency decoupling capacitors should be placed near the processor.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the processor and decoupling capacitors as much as possible.

These capacitors should be evenly distributed around each component on the 3.3 V plane and the 2.9 V plane (or island). Capacitor values should be chosen to ensure they eliminate both low and high frequency noise components.

Power transients also occur as the processor rapidly transitions from a low level of power consumption to a much higher level (or high to low power). A typical example would be entering or exiting the Stop Grant state. Another example would be executing a HALT instruction, causing the processor to enter the Auto HALT Powerdown state, or transitioning from HALT to the Normal state. All of these examples may cause abrupt changes in the power being consumed by the processor. Note that the Auto HALT Powerdown feature is always enabled even when other power management features are not implemented.

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Bulk storage capacitors with a low ESR (Effective Series Resistance) in the 10 to 100 µF range are required to maintain a regulated supply voltage during the interval between the time the current load changes and the point that the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel.

These capacitors should be placed near the processor (on the 3.3 V plane and the 2.9 V plane (or island)) to ensure that these supply voltages stay within specified limits during changes in the supply current during operation.

For more detailed information, please contact Intel or refer to the *Pentium® Processor with Voltage Reduction Technology: Power Supply Design Considerations for Mobile Systems* application note (Order #242558).

5.2 AC Specifications: 50 MHz Bus

The AC specifications given in Table 13 consists of output delays, input setup requirements and input hold requirements for a 50 MHz external bus. All AC specifications (with the exception of those for the TAP signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5 V for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct operation.

Table 13. AC Specifications for 50 MHz Bus Operation†

Symbol	Parameter	Min	Max	Unit	Figure	Notes‡
	Frequency	25.0	50.0	MHz		
t_{1a}	CLK Period	20.0	40.0	ns	4	
t_{1b}	CLK Period Stability		±250	ps		(1), (19)
t_2	CLK High Time	4.0		ns	4	@2 V, (1)
t_3	CLK Low Time	4.0		ns	4	@0.8 V, (1)
t_4	CLK Fall Time	0.15	1.5	ns	4	(2.0 V–0.8 V), (1), (5)
t_5	CLK Rise Time	0.15	1.5	ns	4	(0.8 V–2.0 V), (1), (5)
t_{6a}	ADS#, PWT, PCD, BE7-BE0#, M/IO#, D/C#, CACHE#, SCYC, W/R# Valid Delay	1.0	7.0	ns	5	(22)
t_{6b}	AP Valid Delay	1.0	8.5	ns	5	(22)
t_{6c}	A31-A3, LOCK# Valid Delay	1.1	7.0	ns	5	(22)
t_7	ADS#, AP, A31-A3, PWT, PCD, BE7-BE0#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	ns	6	(1))
t_8	APCHK#, IERR#, FERR#, PCHK# Valid Delay	1.0	8.3	ns	5	(4), (22)
t_9	BREQ, HLDA, SMIACT# Valid Delay	1.0	8.0	ns	5	(4), (22)

†Not 100% tested. Guaranteed by design.
‡Refer to the corresponding note entry in Table 16.

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Table 13. AC Specifications for 50 MHz Bus Operation† (Continued)

Symbol	Parameter	Min	Max	Unit	Figure	Notes‡
t_{10a}	HIT# Valid Delay	1.0	8.0	ns	5	(22)
t_{10b}	HITM# Valid Delay	1.1	6.0	ns	5	(22)
t_{11a}	PM1-PM0, BP3-BP0 Valid Delay	1.0	10.0	ns	5	(22)
t_{11b}	PRDY Valid Delay	1.0	8.0	ns	5	(22)
t_{12}	D63-D0, DP7-DP0 Write Data Valid Delay	1.3	8.5	ns	5	(22)
t_{13}	D63-D0, DP3-DP0 Write Data Float Delay		10.0	ns	6	(1)
t_{14}	A31-A5 Setup Time	6.5		ns	7	(20)
t_{15}	A31-A5 Hold Time	1.0		ns	7	
t_{16a}	INV, AP Setup Time	5.0		ns	7	
t_{16b}	EADS# Setup Time	6.0		ns	7	
t_{17}	EADS#, INV, AP Hold Time	1.0		ns	7	
t_{18a}	KEN# Setup Time	5.0		ns	7	
t_{18b}	NA#, WB/WT# Setup Time	4.5		ns	7	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		ns	7	
t_{20}	BRDY# Setup Time	5.0		ns	7	
t_{21}	BRDY# Hold Time	1.0		ns	7	
t_{22a}	BOFF# Setup Time	5.5		ns	7	
t_{22b}	AHOLD# Setup Time	6.0		ns	7	
t_{23}	AHOLD, BOFF# Hold Time	1.0		ns	7	
t_{24}	BUSCHK#, EWBE#, HOLD, PEN# Setup Time	5.0		ns	7	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		ns	7	
t_{25b}	HOLD Hold Time	1.5		ns	7	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		ns	7	(11), (15)
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		ns	7	(12)
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		ns	7	(11), (15), (16)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		ns	7	(12)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		(14), (16)

†Not 100% tested. Guaranteed by design.
‡Refer to the corresponding note entry in Table 16.

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Table 13. AC Specifications for 50 MHz Bus Operation† (Continued)

Symbol	Parameter	Min	Max	Unit	Figure	Notes‡
t_{31}	R/S# Setup Time	5.0		ns	7	(11), (15), (16)
t_{32}	R/S# Hold Time	1.0		ns	7	(12)
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		(14), (16)
t_{34}	D63–D0, DP7–DP0 Read Data Setup Time	3.8		ns	7	
t_{35}	D63–D0, DP7–DP0 Read Data Hold Time	1.5		ns	7	
t_{36}	RESET Setup Time	5.0		ns	8	(11), (15)
t_{37}	RESET Hold Time	1.0		ns	8	(12)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15		CLKs	8	(16)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		ms	8	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		ns	8	(11), (15), (16)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		ns	8	(12)
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	8	To RESET falling edge (15)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, BRDY#, BUSCHK#) Hold Time, Async.	2.0		CLKs	8	To RESET falling edge (21)
t_{42c}	Reset Configuration Signal (BRDY#, BUSCHK#) Setup Time, Async.	3.0		CLKs	8	To RESET falling edge (21)
t_{42d}	Reset Configuration Signal (BRDY#, BUSCHK#) Hold Time, RESET driven synchronously	1.0		ns	8	To RESET falling edge (1), (21)
t_{43a}	BF Setup Time	1.0		ms	8	(18) to RESET falling edge
t_{43b}	BF Hold Time	2.0		CLKs	8	(18) to RESET falling edge
t_{44}	TCK Frequency		16.0	MHz		
t_{45}	TCK Period	62.5		ns	4	
t_{46}	TCK High Time	25.0		ns	4	@2 V, (1)
t_{47}	TCK Low Time	25.0		ns	4	@0.8 V, (1)
t_{48}	TCK Fall Time		5.0	ns	4	(2.0 V–0.8 V), (1), (8), (9)

†Not 100% tested. Guaranteed by design.
‡Refer to the corresponding note entry in Table 16.

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Table 13. AC Specifications for 50 MHz Bus Operation† (Continued)

Symbol	Parameter	Min	Max	Unit	Figure	Notes‡
t_{49}	TCK Rise Time		5.0	ns	4	(0.8 V–2.0 V), (1), (8), (9)
t_{50}	TRST# Pulse Width	40.0		ns	10	(1), Asynchronous
t_{51}	TDI, TMS Setup Time	5.0		ns	9	(7)
t_{52}	TDI, TMS Hold Time	13.0		ns	9	(7)
t_{53}	TDO Valid Delay	3.0	20.0	ns	9	(8), (22)
t_{54}	TDO Float Delay		25.0	ns	9	(1), (8)
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	ns	9	(3), (8), (10), (22)
t_{56}	All Non-Test Outputs Float Delay		25.0	ns	9	(1), (3), (8), (10)
t_{57}	All Non-Test Inputs Setup Time	5.0		ns	9	(3), (7), (10)
t_{58}	All Non-Test Inputs Hold Time	13.0		ns	9	(3), (7), (10)

†Not 100% tested. Guaranteed by design.
‡Refer to the corresponding note entry in Table 16.

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5.3 AC Specifications: 60 MHz Bus

The AC specifications given in Table 14 consists of output delays, input setup requirements and input hold requirements for a 60 MHz external bus. All AC

specifications (with the exception of those for the TAP signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5 V for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct operation.

Table 14. AC Specifications for 60 MHz Bus Operation†

Symbol	Parameter	Min	Max	Unit	Figure	Notes‡
	Frequency	30.0	60.0	MHz		
t_{1a}	CLK Period	16.67	33.33	ns	4	
t_{1b}	CLK Period Stability		±250	ps		(1), (19)
t_2	CLK High Time	4.0		ns	4	@2 V, (1)
t_3	CLK Low Time	4.0		ns	4	@0.8 V, (1)
t_4	CLK Fall Time	0.15	1.5	ns	4	(2.0 V–0.8 V), (1), (5)
t_5	CLK Rise Time	0.15	1.5	ns	4	(0.8 V–2.0 V), (1), (5)
t_{6a}	ADS#, PWT, PCD, BE7-BE0#, M/IO#, D/C#, CACHE#, SCYC, W/R# Valid Delay	1.0	7.0	ns	5	(22)
t_{6b}	AP Valid Delay	1.0	8.5	ns	5	(22)
t_{6c}	LOCK# Valid Delay	1.1	7.0	ns	5	(22)
t_{6d}	A31-A3, Valid Delay	1.1	6.3	ns	5	(22)
t_7	ADS#, AP, A31-A3, PWT, PCD, BE7-BE0#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	ns	6	(1)
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	ns	5	(4), (22)
t_{8b}	PCHK# Valid Delay	1.0	7.0	ns	5	(4), (22)
t_{9a}	BREQ, HLDA Valid Delay	1.0	8.0	ns	5	(4), (22)
t_{9b}	SMIACT# Valid Delay	1.0	7.6	ns	5	(22)
t_{10a}	HIT# Valid Delay	1.0	8.0	ns	5	(22)
t_{10b}	HITM# Valid Delay	1.1	6.0	ns	5	(22)
t_{11a}	PM1-PM0, BP3-BP0 Valid Delay	1.0	10.0	ns	5	(22)
t_{11b}	PRDY Valid Delay	1.0	8.0	ns	5	(22)

†Not 100% tested. Guaranteed by design.
‡Refer to the corresponding note entry in Table 16.

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Table 14. AC Specifications for 60 MHz Bus Operation†

Symbol	Parameter	Min	Max	Unit	Figure	Notes‡
t_{12}	D63-D0, DP7-DP0 Write Data Valid Delay	1.3	7.5	ns	5	(22)
t_{13}	D63-D0, DP3-DP0 Write Data Float Delay		10.0	ns	6	(1)
t_{14}	A31-A5 Setup Time	6.0		ns	7	(20)
t_{15}	A31-A5 Hold Time	1.0		ns	7	
t_{16a}	INV, AP Setup Time	5.0		ns	7	
t_{16b}	EADS# Setup Time	5.5		ns	7	
t_{17}	EADS#, INV, AP Hold Time	1.0		ns	7	
t_{18a}	KEN# Setup Time	5.0		ns	7	
t_{18b}	NA#, WB/WT# Setup Time	4.5		ns	7	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		ns	7	
t_{20}	BRDY# Setup Time	5.0		ns	7	
t_{21}	BRDY# Hold Time	1.0		ns	7	
t_{22}	AHOLD, BOFF# Setup Time	5.5		ns	7	
t_{23}	AHOLD, BOFF# Hold Time	1.0		ns	7	
t_{24}	BUSCHK#, EWBE#, HOLD, PEN# Setup Time	5.0		ns	7	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		ns	7	
t_{25b}	HOLD Hold Time	1.5		ns	7	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		ns	7	(11), (15)
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		ns	7	(12)
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		ns	7	(11), (15), (16)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		ns	7	(12)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		(14), (16)
t_{31}	R/S# Setup Time	5.0		ns	7	(11), (15), (16)
t_{32}	R/S# Hold Time	1.0		ns	7	(12)
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		(14), (16)
t_{34}	D63–D0, DP7–DP0 Read Data Setup Time	3.0		ns	7	

†Not 100% tested. Guaranteed by design.
‡Refer to the corresponding note entry in Table 16.

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Table 14. AC Specifications for 60 MHz Bus Operation†

Symbol	Parameter	Min	Max	Unit	Figure	Notes‡
t_{35}	D63–D0, DP7–DP0 Read Data Hold Time	1.5		ns	7	
t_{36}	RESET Setup Time	5.0		ns	8	(11), (15)
t_{37}	RESET Hold Time	1.0		ns	8	(12)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15		CLKs	8	(16)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		ms	8	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		ns	8	(11), (15), (16)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		ns	8	(12)
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	8	To RESET falling edge (15)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, BRDY#, BUSCHK#) Hold Time, Async.	2.0		CLKs	8	To RESET falling edge (21)
t_{42c}	Reset Configuration Signal (BRDY#, BUSCHK#) Setup Time, Async.	3.0		CLKs	8	To RESET falling edge (21)
t_{42d}	Reset Configuration Signal (BRDY#, BUSCHK#) Hold Time, RESET driven synchronously	1.0		ns	8	To RESET falling edge (1), (21)
t_{43a}	BF Setup Time	1.0		ms	8	(18) to RESET falling edge
t_{43b}	BF Hold Time	2.0		CLKs	8	(18) to RESET falling edge
t_{44}	TCK Frequency		16.0	MHz		
t_{45}	TCK Period	62.5		ns	4	
t_{46}	TCK High Time	25.0		ns	4	@2 V, (1)
t_{47}	TCK Low Time	25.0		ns	4	@0.8 V, (1)
t_{48}	TCK Fall Time		5.0	ns	4	(2.0 V–0.8 V), (1), (8), (9)
t_{49}	TCK Rise Time		5.0	ns	4	(0.8 V–2.0 V), (1), (8), (9)
t_{50}	TRST# Pulse Width	40.0		ns	10	(1), Asynchronous

†Not 100% tested. Guaranteed by design.
‡Refer to the corresponding note entry in Table 16.

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Table 14. AC Specifications for 60 MHz Bus Operation†

Symbol	Parameter	Min	Max	Unit	Figure	Notes‡
t_{51}	TDI, TMS Setup Time	5.0		ns	9	(7)
t_{52}	TDI, TMS Hold Time	13.0		ns	9	(7)
t_{53}	TDO Valid Delay	3.0	20.0	ns	9	(8), (22)
t_{54}	TDO Float Delay		25.0	ns	9	(1), (8)
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	ns	9	(3), (8), (10), (22)
t_{56}	All Non-Test Outputs Float Delay		25.0	ns	9	(1), (3), (8), (10)
t_{57}	All Non-Test Inputs Setup Time	5.0		ns	9	(3), (7), (10)
t_{58}	All Non-Test Inputs Hold Time	13.0		ns	9	(3), (7), (10)

†Not 100% tested. Guaranteed by design.
‡Refer to the corresponding note entry in Table 16.

5.4   AC Specifications: 66 MHz Bus

The AC specifications given in Table 15 consist of output delays, input setup requirements and input hold requirements for a 66 MHz external bus. All AC specifications (with the exception of those for the TAP signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5 V for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct operation.

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Table 15. AC Specifications for 66 MHz Bus Operation

Symbol	Parameter	Min	Max	Unit	Figure	Notes‡
	Frequency	33.33	66.6	MHz		
t_{1a}	CLK Period	15.0	30.0	ns	4	
t_{1b}	CLK Period Stability		±250	ps		(1), (19)
t_2	CLK High Time	4.0		ns	4	@2 V, (1)
t_3	CLK Low Time	4.0		ns	4	@0.8 V, (1)
t_4	CLK Fall Time	0.15	1.5	ns	4	(2.0 V–0.8 V), (1)
t_5	CLK Rise Time	0.15	1.5	ns	4	(0.8 V–2.0 V), (1)
t_{6a}	PWT, PCD, BE7-BE0#, D/C#, W/R#, CACHE#, SCYC Valid Delay	1.0	7.0	ns	5	(22)
t_{6b}	AP Valid Delay	1.0	8.5	ns	5	(22)
t_{6c}	LOCK# Valid Delay	1.1	7.0	ns	5	(22)
t_{6d}	ADS# Valid Delay	1.0	6.0	ns	5	(22)
t_{6e}	A31-A3 Valid Delay	1.1	6.3	ns	5	(22)

‡Refer to the corresponding note entry in Table 16.

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Table 15. AC Specifications for 66 MHz Bus Operation

Symbol	Parameter	Min	Max	Unit	Figure	Notes‡
t_{6f}	M/IO# Valid Delay	1.0	5.9	ns	5	(22)
t_7	ADS#, AP, A31-A3, PWT, PCD, BE7-BE0#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	ns	6	(1)
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	ns	5	(4), (22)
t_{8b}	PCHK# Valid Delay	1.0	7.0	ns	5	(4), (22)
t_{9a}	BREQ Valid Delay	1.0	8.0	ns	5	(4), (22)
t_{9b}	SMIACT# Valid Delay	1.0	7.3	ns	5	(4), (22)
t_{9c}	HLDA Valid Delay	1.0	6.8	ns	5	(4), (22)
t_{10a}	HIT# Valid Delay	1.0	6.8	ns	5	(22)
t_{10b}	HITM# Valid Delay	1.1	6.0	ns	5	(22)
t_{11a}	PM1-PM0, BP3-BP0 Valid Delay	1.0	10.0	ns	5	(22)
t_{11b}	PRDY Valid Delay	1.0	8.0	ns	5	(22)
t_{12}	D63-D0, DP7-DP0 Write Data Valid Delay	1.3	7.5	ns	5	(22)
t_{13}	D63-D0, DP3-DP0 Write Data Float Delay		10.0	ns	6	(1)
t_{14}	A31-A5 Setup Time	6.0		ns	7	(20)
t_{15}	A42-A5 Hold Time	1.0		ns	7	
t_{16a}	INV, AP Setup Time	5.0		ns	7	
t_{16b}	EADS# Setup Time	5.0		ns	7	
t_{17}	EADS#, INV, AP Hold Time	1.0		ns	7	
t_{18a}	KEN# Setup Time	5.0		ns	7	
t_{18b}	NA#, WB/WT# Setup Time	4.5		ns	7	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		ns	7	
t_{20}	BRDY# Setup Time	5.0		ns	7	
t_{21}	BRDY# Hold Time	1.0		ns	7	
t_{22}	AHOLD, BOFF# Setup Time	5.5		ns	7	
t_{23}	AHOLD, BOFF# Hold Time	1.0		ns	7	
t_{24a}	BUSCHK#, EWBE#, HOLD, Setup Time	5.0		ns	7	
t_{24b}	PEN# Setup Time	4.8		ns	7	

‡Refer to the corresponding note entry in Table 16.

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Table 15. AC Specifications for 66 MHz Bus Operation

Symbol	Parameter	Min	Max	Unit	Figure	Notes‡
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		ns	7	
t_{25b}	HOLD Hold Time	1.5		ns	7	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		ns	7	(11), (15)
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		ns	7	(12)
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		ns	7	(11), (15), (16)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		ns	7	(12)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		(14), (16)
t_{31}	R/S# Setup Time	5.0		ns	7	(11), (15), (16)
t_{32}	R/S# Hold Time	1.0		ns	7	(12)
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		(14), (16)
t_{34}	D63–D0, DP7–DP0 Read Data Setup Time	2.8		ns	7	
t_{35}	D63-D0, DP7-DP0 Read Data Hold Time	1.5		ns	7	
t_{36}	RESET Setup Time	5.0		ns	8	(11), (15)
t_{37}	RESET Hold Time	1.0		ns	8	(12)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15.0		CLKs	8	(16)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		ms	8	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		ns	8	(11), (15), (16)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		ns	8	(12)
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	8	To RESET falling edge (15)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, BRDY#, BUSCHK#) Hold Time, Async.	2.0		CLKs	8	To RESET falling edge (21)
t_{42c}	Reset Configuration Signal (BRDY#, BUSCHK#) Setup Time, Async.	3.0		CLKs	8	To RESET falling edge (21)

‡Refer to the corresponding note entry in Table 16.

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Table 15. AC Specifications for 66 MHz Bus Operation

Symbol	Parameter	Min	Max	Unit	Figure	Notes‡
t_{42d}	Reset Configuration Signal (BRDY#, BUSCHK#) Hold Time, RESET driven synchronously	1.0		ns	8	To RESET falling edge (1), (21)
t_{43a}	BF Setup Time	1.0		ms	8	(18) to RESET falling edge
t_{43b}	BF Hold Time	2.0		CLKs	8	(18) to RESET falling edge
t_{44}	TCK Frequency		16.0	MHz		
t_{45}	TCK Period	62.5		ns	4	
t_{46}	TCK High Time	25.0		ns	4	@2 V, (1)
t_{47}	TCK Low Time	25.0		ns	4	@0.8 V, (1)
t_{48}	TCK Fall Time		5.0	ns	4	(2.0 V–0.8 V), (1), (8), (9)
t_{49}	TCK Rise Time		5.0	ns	4	(0.8 V–2.0 V), (1), (8), (9)
t_{50}	TRST# Pulse Width	40.0		ns	10	(1), Asynchronous
t_{51}	TDI, TMS Setup Time	5.0		ns	9	(7)
t_{52}	TDI, TMS Hold Time	13.0		ns	9	(7)
t_{53}	TDO Valid Delay	3.0	20.0	ns	9	(8), (22)
t_{54}	TDO Float Delay		25.0	ns	9	(1), (8)
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	ns	9	(3), (8), (10), (22)
t_{56}	All Non-Test Outputs Float Delay		25.0	ns	9	(1), (3), (8), (10)
t_{57}	All Non-Test Inputs Setup Time	5.0		ns	9	(3), (7), (10)
t_{58}	All Non-Test Inputs Hold Time	13.0		ns	9	(3), (7), (10)

‡Refer to the corresponding note entry in Table 16.

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5.5 AC Specifications: Notes and Figures

Table 16. AC Timing Notes

Notes 2, 6 and 13 are general and apply to all standard TTL signals used with the Pentium processor family.

1. Not 100% tested. Guaranteed by design.

2. TTL input test waveforms are assumed to be 0 to 3 V transitions with 1 V/ns rise and fall times.

3. Non-test outputs and inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.

4. APCHK#, FERR#, HLDA, IERR#, LOCK#, and PCHK# are glitch-free outputs. Glitch-free signals monotonically transition without false transitions (i.e., glitches).

5. 0.8 V/ns ≤ CLK input rise/fall time ≤ 8 V/ns.

6. 0.3 V/ns ≤ input rise/fall time ≤ 5 V/ns.

7. Referenced to TCK rising edge.

8. Referenced to TCK falling edge.

9. 1 ns can be added to the maximum TCK rise and fall times for every 10 MHz of frequency below 33 MHz.

10. During probe mode operation, do not use the boundary scan timings (t_{55-58}).

11. Setup time is required to guarantee recognition on a specific clock.

12. Hold time is required to guarantee recognition on a specific clock.

13. All TTL timings are referenced from 1.5 V.

14. To guarantee proper asynchronous recognition, the signal must have been de-asserted (inactive) for a minimum of two clocks before being returned active and must meet the minimum pulse width.

15. This input may be driven asynchronously.

16. When driven asynchronously, RESET, NMI, FLUSH#, R/S#, INIT, and SMI# must be de-asserted (inactive) for a minimum of two clocks before being returned active.

17. The D/C#, M/IO#, W/R#, CACHE#, and A31-A5 signals are sampled only on the CLK that ADS# is active.

18. BF should be strapped to $V_{CC}3$ or left floating.

19. These signals are measured on the rising edge of adjacent CLKs at 1.5 V. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 KHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices.

20. Timing (t_{14}) is required for external snooping (e.g., address setup to the CLK in which EADS# is sampled active).

21. BUSCHK# is used as a reset configuration signal to select buffer size.

22. Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal flight time delays.

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T_v = t5, t49

T_w = t4, t48

T_x = t3, t47

T_y = t1, t45

T_z = t2, t46

PP0051
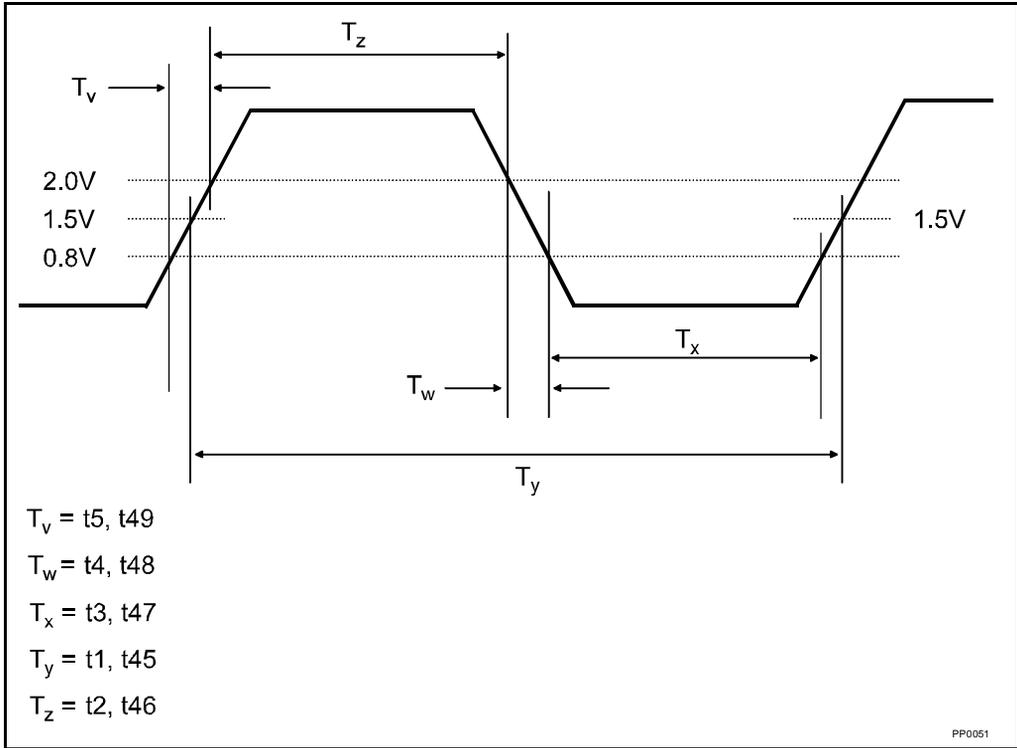
Figure 4. Clock Waveform

T_x = t6, t8, t9, t10, t11, t12

PP0052 Valid Delay Timings
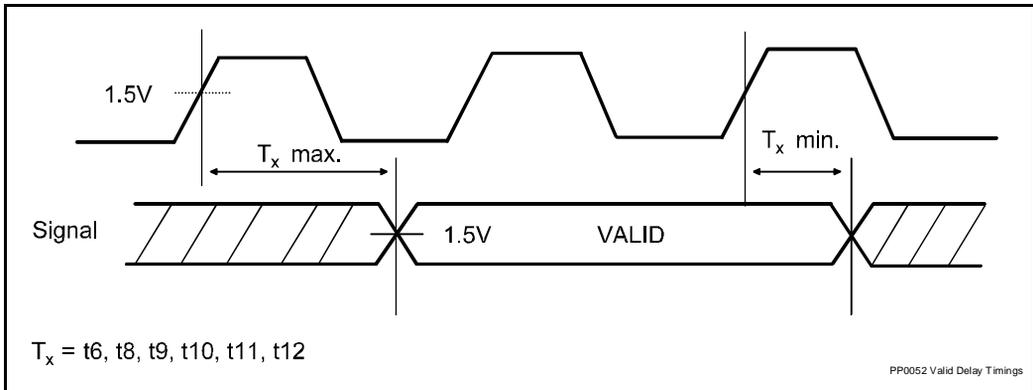
Figure 5. Valid Delay Timings

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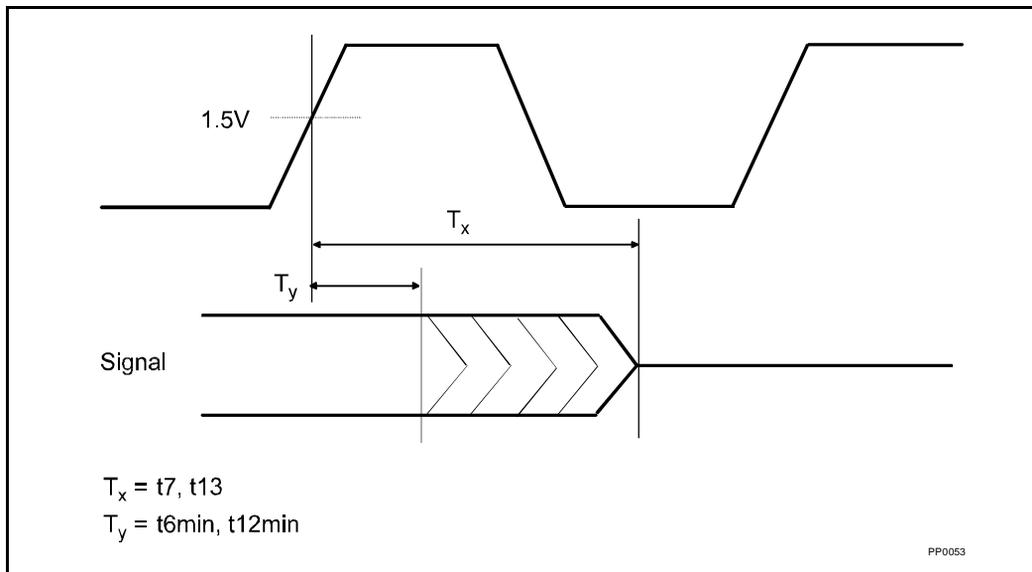
Figure 6. Float Delay Timings
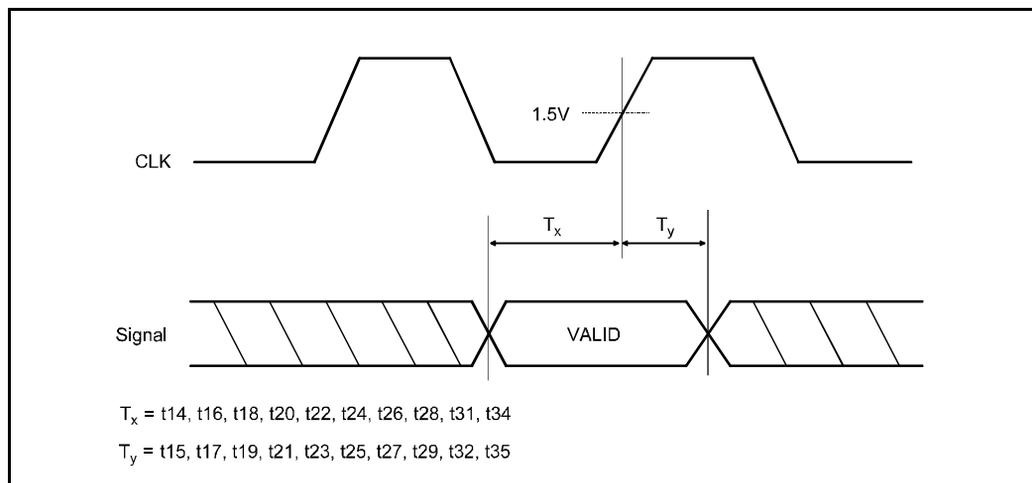
Figure 7. Setup and Hold Timings

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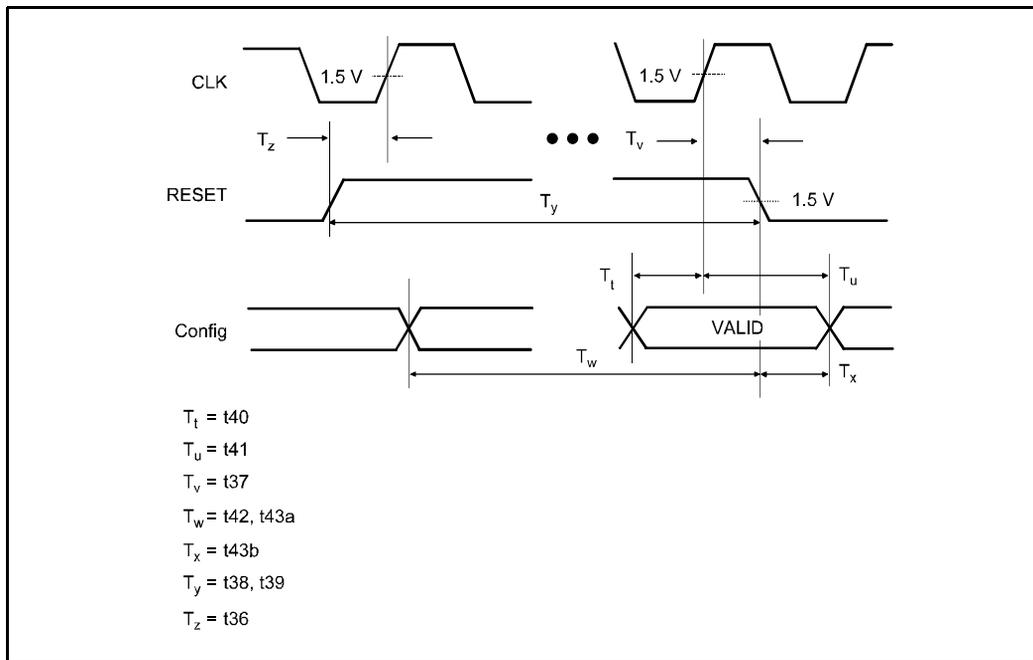
Figure 8. Reset and Configuration Timings

T_t = t40
T_u = t41
T_v = t37
T_w = t42, t43a
T_x = t43b
T_y = t38, t39
T_z = t36
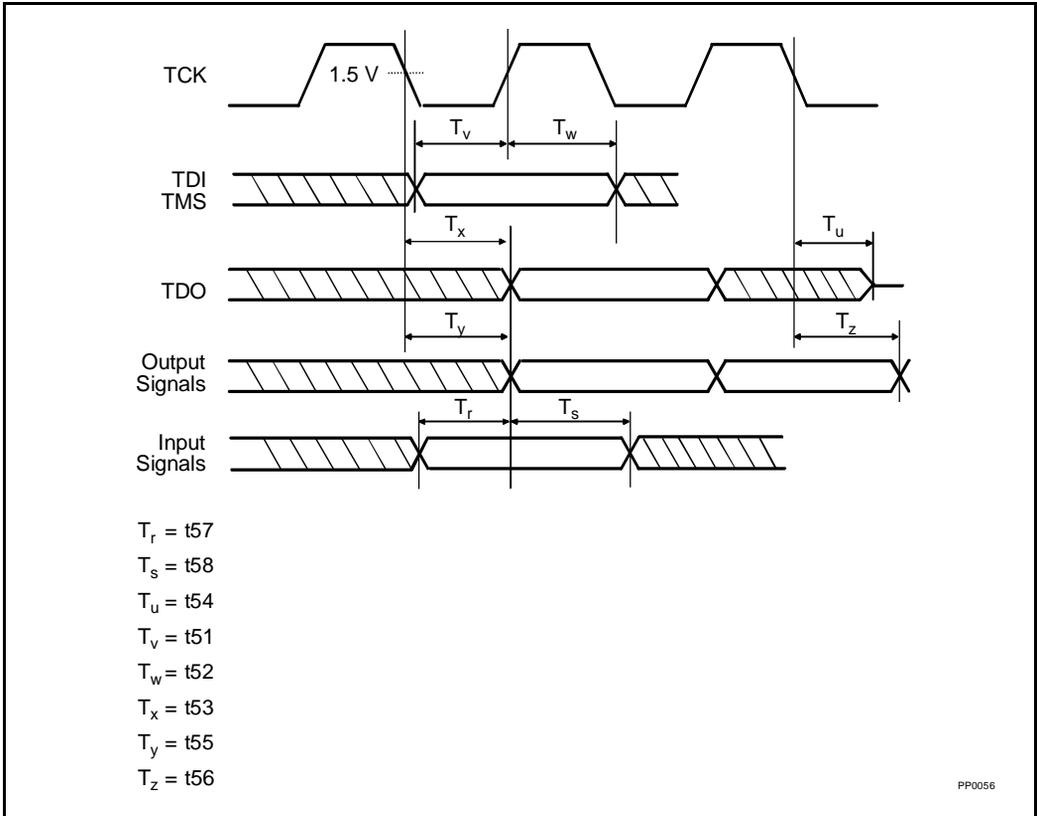
**Figure 9. Test Timings**
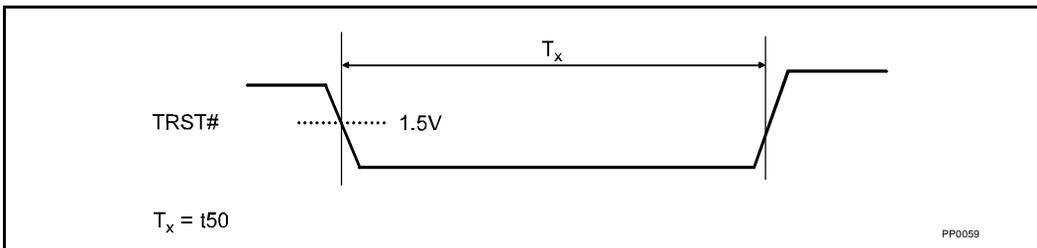

Figure 10. Test Reset Timings

ADVANCE INFORMATION
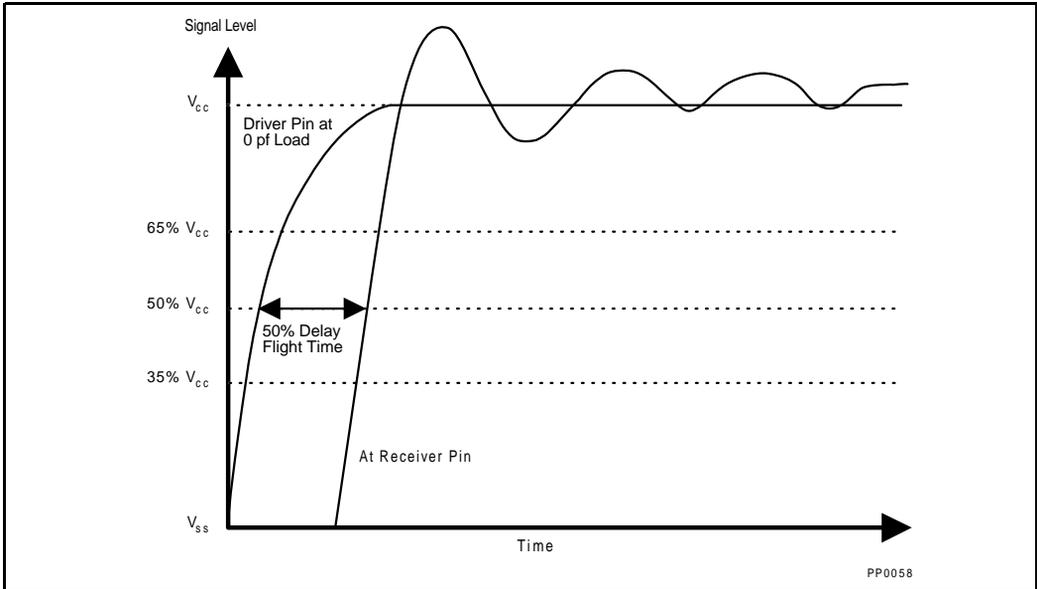
Figure 11. V$_{CC}$ Measurement of Flight Time

6.0 I/O Buffer Models

The first order I/O buffer model is a simplified representation of the Special Environment Pentium processor's complex input and output buffers. Figures 12 and 13 show the structure of the input buffer model. Figure 14 shows the output buffer model. Tables 18 and 19 show the parameters used to specify these models.

Although they are simplified, these buffer models will accurately model flight time and signal quality. For these parameters, there is very little added accuracy in a complete transistor model.

The following two models represent the input buffer models. The first model, Figure 12, represents all of the input buffers except for a special group of input buffers. The second model, Figure 13, represents these special buffers. The special group inputs are listed in Table 17.

Table 17. Special Group Inputs

AHOLD	INV
BOFF#	KEN#
CLK	NA#
EADS#	WB/WT#
EWBE#	

In addition to the input and output buffer parameters, input protection diode models are provided for added accuracy. These diodes have been optimized to provide ESD protection and provide some level of clamping. Although the diodes are not required for simulation, it may be more difficult to meet specifications without them.

Some signal quality specifications require that the diodes be removed from the input model. The series resistors (Rs) are a part of the diode model. Remove these when removing the diodes from the input model.

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Note: V_{CC} in this figure refers to the I/O buffer $V_{CC}3$.

PP0059
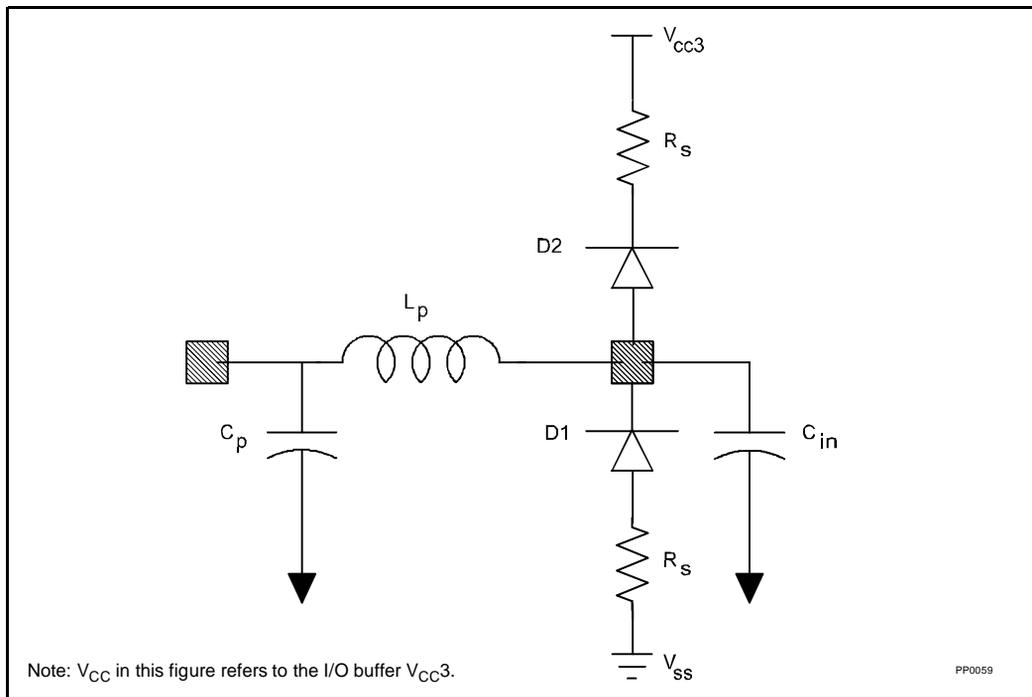
Figure 12. Input Buffer Model, Except Special Group

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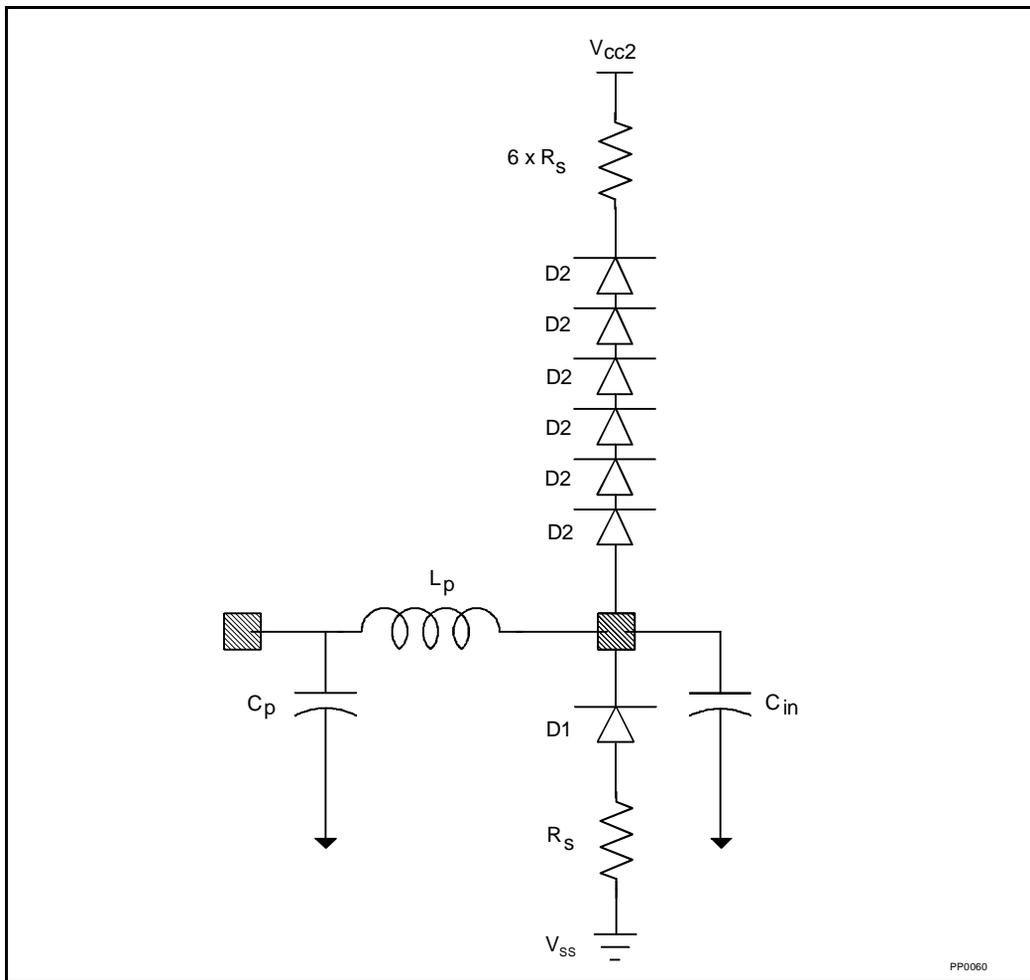
Figure 13. Input Buffer Model for Special Group

Table 18. Parameters Used in the Specification of the First Order Input Buffer Model

Parameter	Description
C_{IN}	Minimum and Maximum value of the capacitance of the input buffer model
L_P	Minimum and Maximum value of the package inductance
C_P	Minimum and Maximum value of the package capacitance
R_S	Diode Series Resistance
D1, D2	Ideal Diodes

Figure 14 shows the structure of the output buffer model. This model is used for all of the output buffers of the Pentium processor with voltage reduction technology.
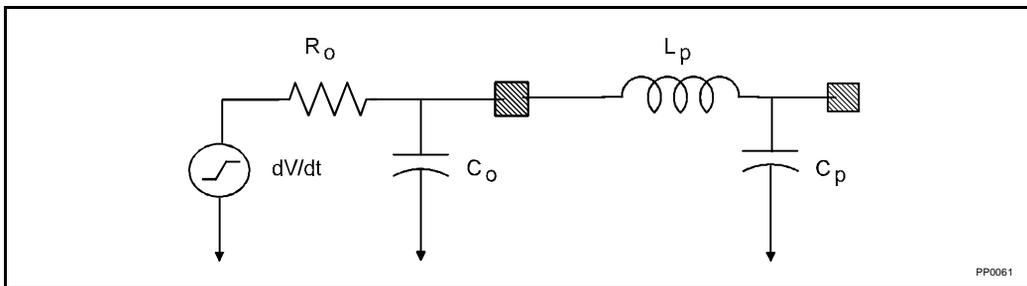

Figure 14. First Order Output Buffer Model

Table 19. Parameters Used in the Specification of the First Order Output Buffer Model

Parameter	Description
dV/dt	Minimum and maximum value of the rate of change of the open circuit voltage source used in the output buffer model
R_O	Minimum and maximum value of the output impedance of the output buffer model
C_O	Minimum and Maximum value of the capacitance of the output buffer model
L_P	Minimum and Maximum value of the package inductance
C_P	Minimum and Maximum value of the package capacitance

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6.1   Buffer Model Parameters

This section gives the parameters for the Special Environment Pentium processor's input, output and bidirectional signal, as well as the settings for the configurable buffers.

Some pins on the processor have selectable buffer sizes. These pins use the configurable output buffer EB2. Table 20 shows the BRDY# drive level required at the falling edge of RESET to select the buffer strength. The buffer sizes selected should be the appropriate size required; otherwise AC timings might not be met, or too much overshoot and ringback may occur. There are no other selection choices; all of the configurable buffers are set to the same size at the same time.

Table 20. Buffer Selection Chart

Environment	BRDY#	Buffer Selection
Typical Stand Alone Component	1	EB2
Loaded Component	0	EB2A

NOTE: For correct buffer selection, the BUSCHK# signal must be held inactive (high) at the falling edge of RESET.

The input, output and bidirectional buffer values are listed in Table 22. This table contains listings for all three buffer types, use care not to confuse them during simulation. When a bidirectional pin is operating as an input, use the Cin, Cp and Lp values; if it is operating as a driver, use all of the data parameters. Please refer to Table 21 for each signal's buffer type.

Table 21. Signal to Buffer Type

Signals	Type	Driver Buffer Type	Receiver Buffer Type
CLK	I		ER0
A20M#, AHOLD, BF, BOFF#, BRDY#, BUSCHK#, EADS#, EWBE#, FLUSH#, HOLD, IGNNE#, INIT, INTR, INV, KEN#, NA#, NMI, PEN#, R/S#, RESET, SMI#, STPCLK#, TCK, TDI, TMS, TRST#, WB/WT#	I		ER1
APCHK#, BE7-BE5#, BP3-BP2, BREQ, FERR#, IERR#, PCD, PCHK#, PM0/BP0, PM1/BP1, PRDY, PWT, SMIACT#, TDO, U/O#	O	ED1	
A31-A21, AP, BE4-BE0#, CACHE#, D/C#, D63-D0, DP8-DP0[8:0], HLDA, LOCK#, M/IO#, SCYC	I/O	EB1	EB1
A20-A3, ADS#, HITM#, W/R#	I/O	EB2/EB2A	EB2/EB2A
HIT#	I/O	EB3	EB3

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Table 22. Special Environment Pentium® Processor Input, Output and Bidirectional Buffer Model Parameters

Buffer Type	Transition	dV/dt (V/nsec)		R_O (Ohms)		C_P (pF)		L_P (nH)		C_O/C_{IN} (pF)	
		min	max	min	max	min	max	min	max	min	max
ER0 (input)	Rising					3.0	5.0	4.0	6.0	0.8	1.2
	Falling					3.0	5.0	4.0	6.0	0.8	1.2
ER1 (input)	Rising					1.1	5.3	7.7	15.3	0.8	1.2
	Falling					1.1	5.3	7.7	15.3	0.8	1.2
ED1 (output)	Rising	3/3.0	3.7/0.9	21.6	53.1	1.1	5.8	8.1	16.3	2.0	2.6
	Falling	3/2.8	3.7/0.8	17.5	50.7	1.1	5.8	8.1	16.3	2.0	2.6
EB1 (bidir)	Rising	3/3.0	3.7/0.9	21.6	53.1	1.3	7.0	8.2	18.4	2.0	2.6
	Falling	3/2.8	3.7/0.8	17.5	50.7	1.3	7.0	8.2	18.4	2.0	2.6

Table 22. Special Environment Pentium® Processor Input, Output and Bidirectional Buffer Model Parameters

Buffer Type	Transition	dV/dt (V/nsec)		R_O (Ohms)		C_P (pF)		L_P (nH)		C_O/C_{IN} (pF)	
		min	max	min	max	min	max	min	max	min	max
EB2 (bidir)	Rising	3/3.0	3.7/0.9	21.6	53.1	1.3	5.4	8.5	16.0	9.1	9.7
	Falling	3/2.8	3.7/0.8	17.5	50.7	1.3	5.4	8.5	16.0	9.1	9.7
EB2A (bidir)	Rising	3/2.4	3.7/0.9	10.1	22.4	1.3	5.4	8.5	16.0	9.1	9.7
	Falling	3/2.4	3.7/0.9	9.0	21.2	1.3	5.4	8.5	16.0	9.1	9.7
EB3 (bidir)	Rising	3/3.0	3.7/0.9	21.6	53.1	1.9	4.2	10.5	14.3	3.3	3.9
	Falling	3/2.8	3.7/0.8	17.5	50.7	1.9	4.2	10.5	14.3	3.3	3.9

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Table 23. Input Buffer Model Parameters: D (Diodes)

Symbol	Parameter	D1	D2
IS	Saturation Current	1.4×10^{-14} A	2.78×10^{-16} A
N	Emission Coefficient	1.19	1.00
RS	Series Resistance	6.5 Ohms	6.5 Ohms
TT	Transit Time	3 ns	6 ns
VJ	PN Potential	0.983 V	0.967 V
CJ0	Zero Bias PN Capacitance	0.281 pF	0.365 pF
M	PN Grading Coefficient	0.385	0.376

6.2   Signal Quality Specifications

To ensure proper data transfer and component reliability, signals driven by the system into the processor must meet signal quality specifications. There are two signal quality parameters: Ringback and Settling Time.

6.2.1   Ringback

Ringback is the absolute value of the maximum voltage at the receiving pin below $V_{CC}3$ (or above V_{SS}) relative to $V_{CC}3$ (or V_{SS}) after the signal has reached its maximum voltage level. Excessive ringback can cause false signal detection and degrade the processor's long-term reliability. Using the input buffer model (with or without the diodes), ringback can be simulated at the processor's input pins.

If simulated without the input diodes, follow the maximum overshoot/undershoot specification. Overshoot (undershoot) is the absolute value of the maximum voltage above $V_{CC}3$ (below V_{SS}). By meeting the overshoot/undershoot specification, the signal is guaranteed not to ringback excessively.

Maximum overshoot/undershoot = 1.4 V above $V_{CC}3$
(without diodes)

Maximum overshoot/undershoot = 1.6 V above $V_{CC}5$
(without diodes)

If simulated with the diodes present in the input model, follow the maximum ringback specification:

Maximum ringback on Inputs = 0.8 V (with diodes)
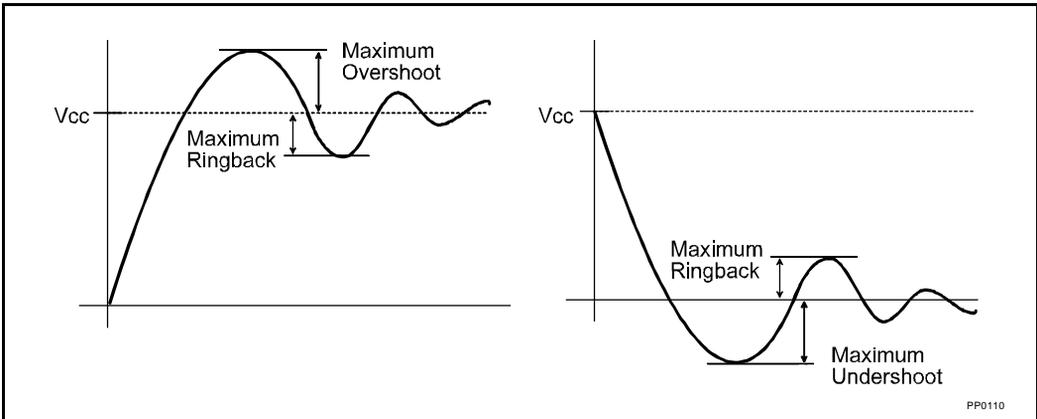
Figure 15. Overshoot/Undershoot and Ringback Guidelines

6.2.2 Settling Time

The settling time is defined as the time a signal requires at the receiver to settle within 10 percent of $V_{CC}3$ or V_{SS}. Maximum settling time is the maximum time allowed for a signal to reach within 10 percent of its final value.

Table 24. Maximum Settling Time

66 MHz	12.5 ns
60 MHz	14.2 ns
50 MHz	17.5 ns

Most available simulation tools are unable to accurately simulate settling time. On a physical board, second-order effects and other effects serve to dampen the signal at the receiver. In response to these concerns, settling time is a recommendation or a tool for layout tuning and not a specification. Although simulated settling time has not shown good correlation with physical, measured settling time, settling time simulations can still be used as a tool to tune layouts.

Use the following procedure to verify board simulation and tuning with concerns for settling time.

1. Simulate settling time at the slow corner for a particular signal.

2. If settling time violations occur, simulate signal trace with D.C. diodes in place at the receiver pin. The D.C. diode behaves almost identically to the actual (non-linear) diode on the part as long as excessive overshoot does not occur.
3. If settling time violations still occur, simulate flight times for five consecutive cycles for that particular signal.
4. If flight time values are consistent over the five simulations, settling time should not be a concern. If however, flight times are not consistent over the five simulations, layout tuning is required.
5. Note that, for signals that are allocated two cycles for flight time, the recommended settling time is doubled

To ensure that there is no impact on the signal flight times if the waveform has not settled, settling time is simulated at the slow corner. Settling time may be simulated with the diodes included or excluded from the input buffer model. If diodes are included, settling time recommendations will be easier to meet.

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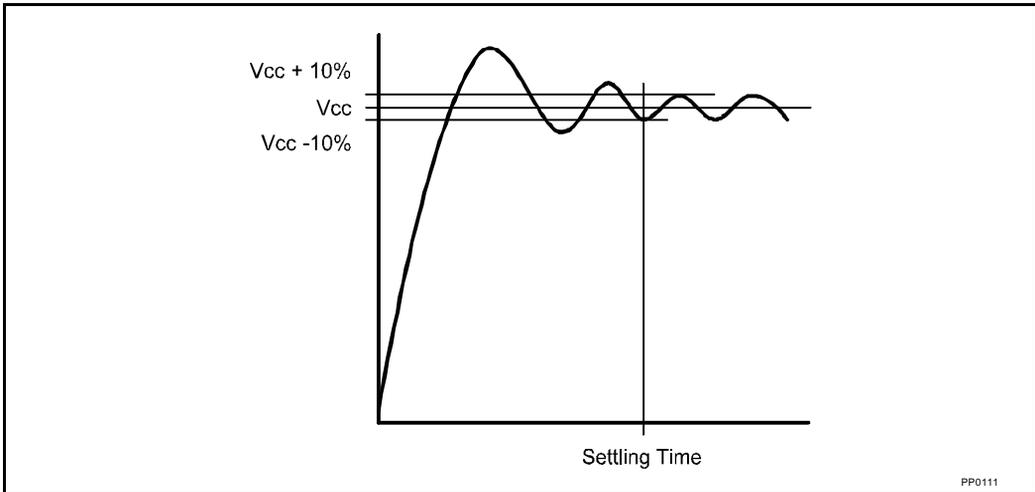
Figure 16. Settling Time

7.0 Mechanical Specifications

The Special Environment Pentium processor is packaged in a 296-pin Staggered Pin Grid Array (SPGA). The pins are arranged in a 37 x 37 matrix with a package dimension of 1.95" x 1.95". The mechanical specifications are provided in Table 25. Figure 17 graphically represents Table 21.

Table 25. 296-Pin Ceramic Pin Grid Array: Package Dimensions

Symbol	Millimeters			Inches		
	Min	**Max**	**Notes**	**Min**	**Max**	**Notes**
A1	0.66	0.86	Ceramic Lid	0.026	0.034	Ceramic Lid
A2	2.62	2.97		0.103	0.117	
B	0.43	0.51		0.017	0.020	
D	49.28	49.78		1.940	1.960	
D1	45.59	45.85		1.795	1.805	
D3	24.00	24.25	Includes Fillet	0.945	0.955	Includes Fillet
e1	2.29	2.79		0.090	0.110	
L	3.05	3.30		0.120	1.130	
N	296		Total Pins	296		Total Pins
S1	1.52	2.54		0.060	0.100	

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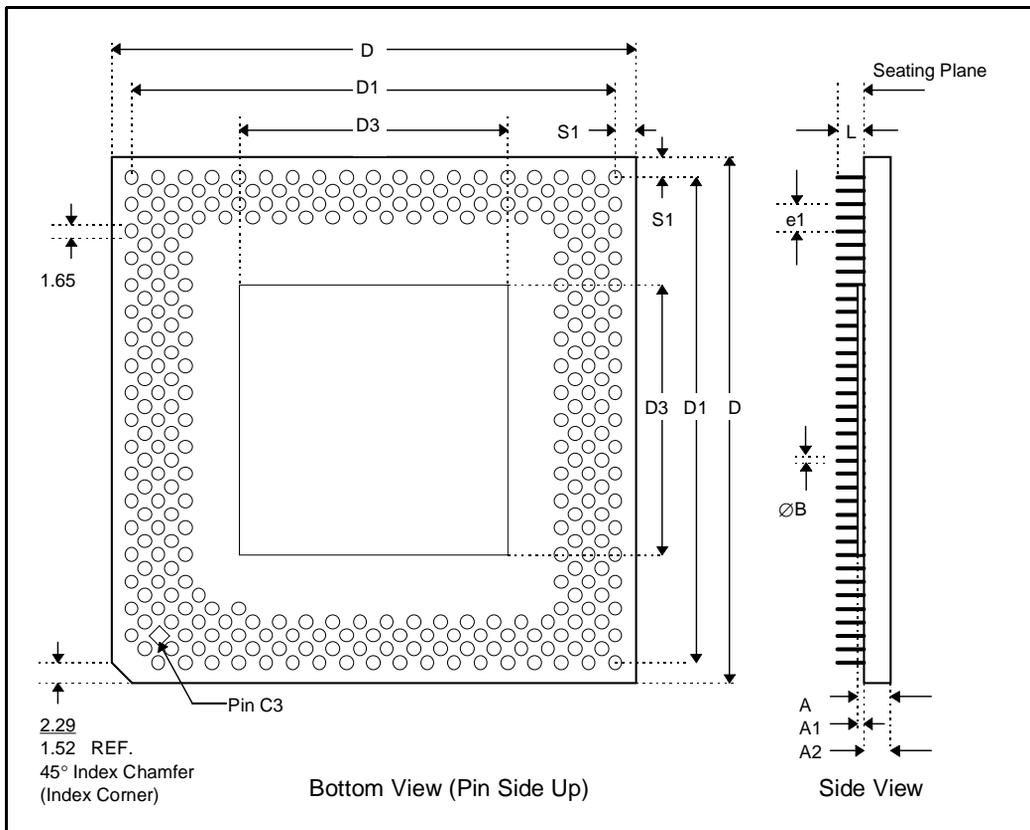
Figure 17. 296-Pin Ceramic Pin Grid Array Package

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8.0   Thermal Specifications

The Special Environment Pentium processors are available in three specific operating ranges: SE1, SE3, and SE5. Table 26 lists the operating ranges and the corresponding product markings.

Table 26. Specified Operating Temperatures

Specification	T_{CASE}	Product Marking
SE1	-55°C to +125°C	MG80502
SE3	-40°C to +110°C	TA80502
SE5	-40°C to +85°C	MG80502 SM637

8.1   Measuring Thermal Values

To verify that the proper T_C (case temperature) is maintained, it should be measured at the center of the package top surface (opposite of the pins). The measurement is made in the same way with or without a heat sink attached. When a heatsink is attached a hole (smaller than 0.150" diameter) should be drilled through the heat sink to allow probing the center of the package. See Figure 18 for an illustration of how to measure T_C.

To minimize any measurement errors, the following techniques are recommended:

• Use 36 gauge or finer diameter K, T, or J type thermocouples. Intel's laboratory testing is done using a thermocouple made by Omega (part number: 5TC-TTK-36-36).

• Attach the thermocouple bead or junction to the center of the package top surface using highly thermally conductive cements. Intel's laboratory testing was done using Omega Bond (part number: OB-100).

• The thermocouple should be attached at a 90° angle as shown in Figure 18.

• When drilling a hole through a heat sink, the holes diameter should not exceed a 0.150" diameter.
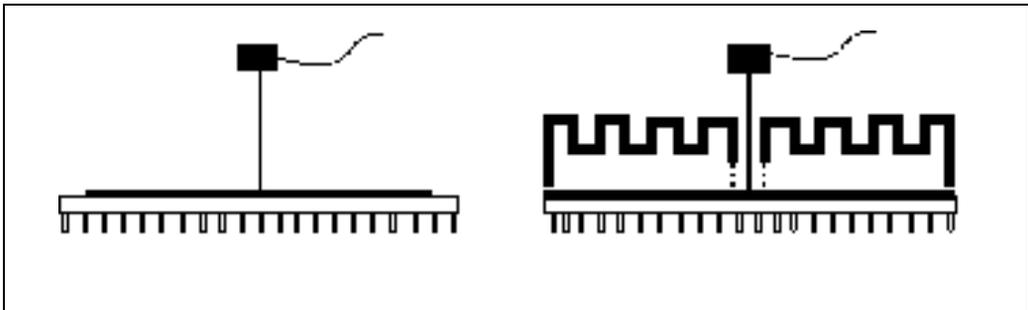
Figure 18. Technique for Measuring T_C

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8.2 Thermal Equations and Data

Ambient temperature (T_A) is not specified directly. The only requirement is that the case temperature (T_C) is met. The ambient temperature can be calculated from the following equations:

$$T_J = T_C + (P * \Theta_{JC})$$

$$T_A = T_J - (P * \Theta_{JA})$$

$$T_A = T_C - (P * \Theta_{CA})$$

$$T_C = T_A - [P * (\Theta_{JA} - \Theta_{JC})]$$

$$\Theta_{CA} = \Theta_{JA} - \Theta_{JC}$$

where, T_A and T_C are ambient and case temperatures (°C)

T_J is the junction temperature (°C)

Θ_{CA} = Case-to-Ambient thermal resistance (°C/W)

Θ_{JA} = Junction-to-Ambient thermal resistance (°C/W)

Θ_{JC} = Junction-to-Case thermal resistance (°C/W)

P = maximum power consumption (Watts)

Table 27 lists the Θ_{CA} values for the Special Environment Pentium processors. Figure 19 is a graphical representation of the data.

Table 27. Thermal Resistances for Packages without Spreader

Heat Sink in Inches	ΘJC (×C/Watt)	ΘCA (°C/Watt) vs. Laminar Airflow (linear ft./min)					
		0	100	200	400	600	800
0.25	0.8	9.1	8.0	6.6	4.4	3.6	3.0
0.35	0.8	8.8	7.5	6.0	4.0	3.3	2.8
0.45	0.8	8.4	7.0	5.3	3.6	2.9	2.5
0.55	0.8	8.1	6.5	4.7	3.2	2.6	2.3
0.65	0.8	7.7	6.0	4.3	3.0	2.4	2.1

NOTES:

1. Heat sinks are omni-directional pin aluminum alloy.
   Features were based on standard extrusion practices for a given height.
     Pin size ranged from 50 to 129 mils
     Pin spacing ranged from 93 to 175 mils
     Based thickness ranged from 79 to 200 mils
2. Heat sink attach was 0.005" of thermal grease.
    Attach thickness of 0.002" will improve performance approximately 0.3oC/Watt

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Table 27. Thermal Resistances for Packages without Spreader

0.80	0.8	7.0	5.3	3.9	2.8	2.2	2.0
1.00	0.8	6.3	4.6	3.6	2.6	2.1	1.8
1.20	0.8	5.9	4.3	3.3	2.4	2.0	1.8
1.40	0.8	5.4	3.9	3.0	2.2	1.9	1.7
Without Heat Sink	1.3	14.4	13.1	11.7	8.8	7.4	6.5

NOTES:

1. Heat sinks are omni-directional pin aluminum alloy.
    Features were based on standard extrusion practices for a given height.
        Pin size ranged from 50 to 129 mils
        Pin spacing ranged from 93 to 175 mils
        Based thickness ranged from 79 to 200 mils

2. Heat sink attach was 0.005" of thermal grease.
    Attach thickness of 0.002" will improve performance approximately 0.3oC/Watt
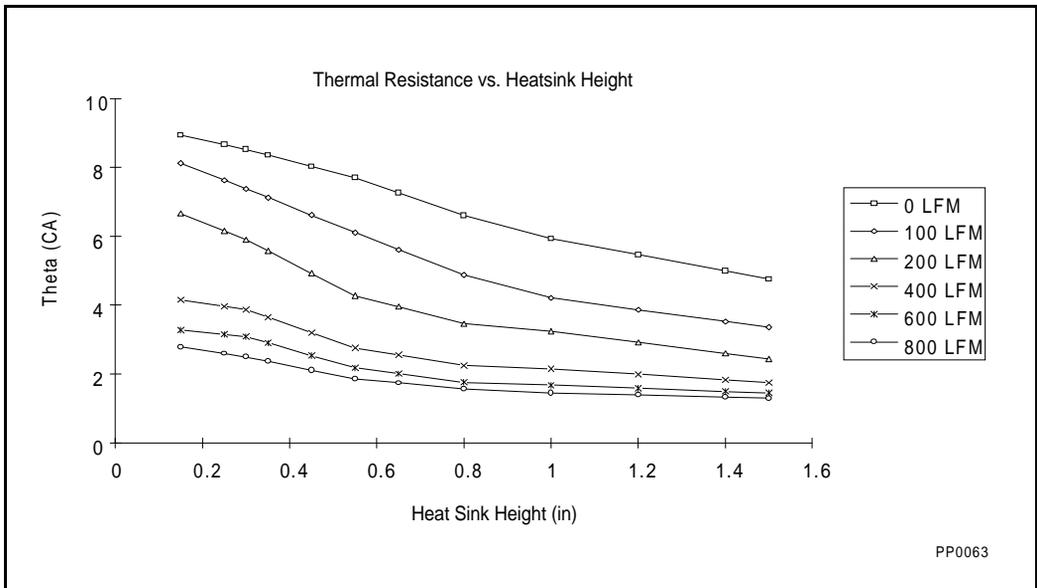

Figure 19. Thermal Resistance vs. Heat Sink Height

9.0   Errata

To ensure proper use of your components, please refer to the *Pentium® Processor Specification Update* (order #242480) from the Intel Literature Center. The update includes specification changes, errata, specification clarifications, and documentation changes for the Pentium processor in general.

The information for the 133 MHz, 120 MHz, and 100 MHz Pentium processors is located in Part Two of the update. The information is dependent on the processor's topside mark:

Topside Mark	Stepping Information	Component Type
xx80502xxxxx QDF490	cB1	preliminary samples
xx80502xxxxx QDF506	mcC0	samples
xx80502xxxxx 5962-945780xxXA	mcC0	production

In addition to the information in the Specification Update, the special environment components include the following errata:

Stepping	Errata
cB1	The JTAG unit is tested only at room temperature (25 °C) and is not guaranteed to operate over the components full temperature range.
mcC0	The core supply voltage is limited to 3.1 V ± 0.165 mV. This errata will be fixed in the next stepping. All power consumption specifications in this datasheet are computed with a 3.1 V supply voltage.

10.0   Revision History

Before finalizing a design or ordering devices, please verify that you have the latest data sheet version by contacting your local Intel sales office or Intel distributor representative.

This data sheet (-003) contains the following changes from the previous version (-002).

• The supply current specifications and power dissipation specifications have changed.
• A component errata section has been added.

This data sheet (-002) contains the following changes from the previous version (-001).

• The Special Environment Pentium processor has been streamlined for embedded applications. The following changes have been made to the product and the data sheet.

— Dual Processing, APIC, and Functional Redundancy support have been removed.

— The following signals have been removed: ADSC#, BRDYC#, CPUTYP, D/P#, FRCMC#, PBGNT#, PBREQ#, PHIT#, PHITM#, PIC-CLK, PICD0 [DPEN#], PICD1 [APICEN].

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