SGS-THOMSON MICROELECTRONICS

ST486DX4V

75, 100 & 120 MHz Clock Tripled 3.45 Volt 486 CPU

PRELIMINARY DATA

- **IMPROVED 486DX4 PERFORMANCE**
  - Clock tripled core speeds up to 120 MHz
  - Integrated FPU 10% faster than 80486DX4
  - Up to 50 MHz bus speeds for fast local bus systems, servers
- **INDUSTRY STANDARD 486 COMPATIBILITY**
  - 486DX socket and instruction set compatible
  - Runs DOS, Windows, OS/2, UNIX
  - Standard 168-pin Ceramic & Plastic PGA
  - 208-pin QFP
- **ON-CHIP 8-KBYTE WRITE-BACK CACHE**
  - Industry-wide write-back chipset support
  - Burst-mode write capability
  - Configurable as write-back or write-through
- **ADVANCED POWER MANAGEMENT**
  - Fast SMI interrupt with separate memory space
  - Fully static design permits dynamic clock control
  - Software or hardware initiated low power suspend
  - Automatic FPU power-down mode

The SGS-THOMSON ST486DX4 3.45 volt CPUs are advanced 486DX/DX2/DX4 compatible processors. These CPUs incorporate an on-chip 8KByte write-back cache and an integrated math coprocessor.

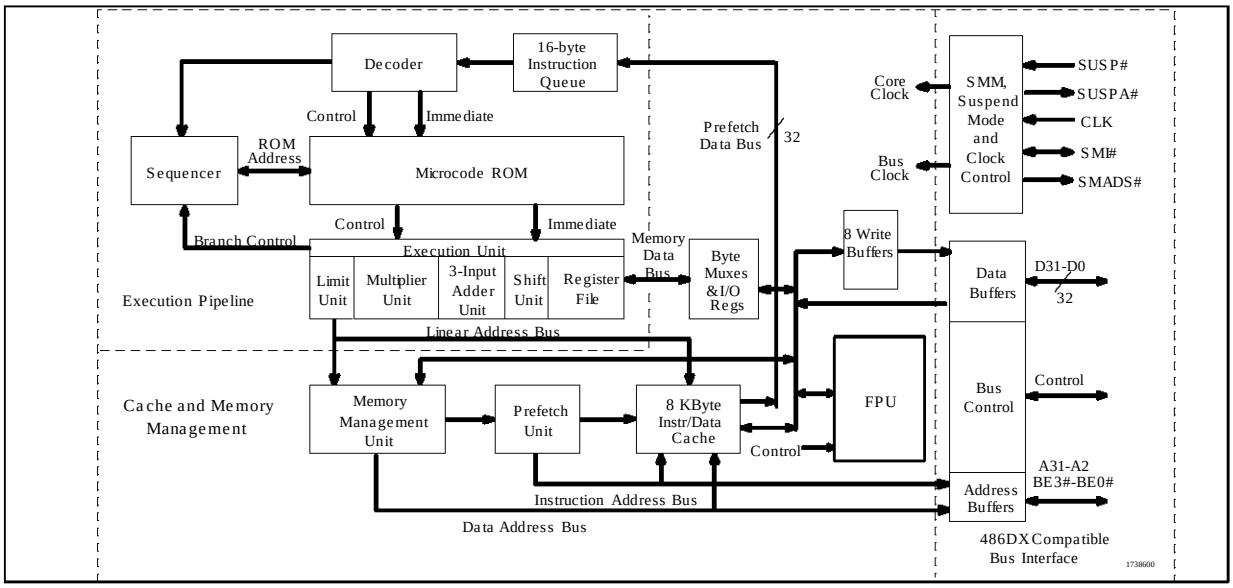
The on-chip write-back cache allows up to 15% higher performance by eliminating unnecessary external write cycles. On traditional write-through CPUs, these external write cycles can create bus bottlenecks affecting system wide performance.

The integrated floating point unit, improves performance up to 10% over the 80486DX4 at equal internal frequency as measured using Power Meter Whetstone test.

These processors are designed to meet the power management requirements in the newest generation of low-power desktops and notebooks. Power is saved by taking advantage of advanced power management features such as static circuitry, SMM, and automatic FPU power-down. Fast entry and exit of SMM allows frequent use of the SMM feature without noticeable performance degradation.

This CPU family maintains compatibility with the installed base of x86 software and provides essential socket compatibility with the 486DX/DX2/DX4

BLOCK DIAGRAM



1.0 PRODUCT OVERVIEW

The SGS THOMSON ST486DX™ 3.45 volt microprocessors are advanced 486DX4 microprocessors. The ST486DX4 CPU operates at two or three times the external bus speed.

The CPUs in the ST486DX4 family are high speed low voltage CPUs attaining clock-tripled core speeds of up to 120 MHz.

The ST486DX4 8-KByte cache can be configured to run in traditional write-through mode or in the higher performance write-back mode. Write-back mode eliminates unnecessary external memory write cycles offering up to 15% higher overall performance (100 MHz, PC Bench 9.0) than write-through mode.

The ST486DX4 supports 8, 16 and 32-bit data types and operates in real, virtual 8086 and protected modes. The CPU can access up to 4 GBytes of physical memory using a 32-bit burst mode bus. Floating point instructions are parallel processed using an on-chip math coprocessor.

The ST486DX4 CPUs are ideal design solutions for low-powered "Green PC" desktops as well as portable computers. These microprocessors typically draw only 450 µA, while the input clock is stopped in suspend mode, due to their static design. System Management Mode (SMM) allows the implementation of transparent system power management or the software emulation of I/O peripheral devices.

A list of ST486DX4 3.45 volt parts, including their operating frequency, and package types are listed on page 24 of this document.

1.1 Clock-Tripled CPU Core

The clock-tripled ST486DX4 CPU core operates at three times the frequency of the external clock input, while continuing to operate the bus interface at the external clock frequency. This configuration provides high frequency CPU performance without requiring a high speed interface to external memory.

The ST486DX4 provides up to 2.8 times the performance of a 486DX at the same external clock frequency. This level of performance is achieved by tripling the frequency of the input clock and using the resulting signal to drive the CPU core. To further enhance this architecture, the ST486DX4 reduces the performance penalty of slow external memory accesses through use of an on-chip write-back cache and eight write buffers.

The CPU core consists of a five-stage pipeline optimized for minimal instruction cycle times and includes all necessary hardware interlocks to permit successive instruction execution overlap. The execution stage of the pipeline executes simple but frequently used instructions in a single clock cycle and the hardware multiplier executes 16-bit integer multiplications in only three clocks.

1.2 On-Chip Write-Back Cache

The ST486DX4 on-chip cache can be configured to run in traditional write-through mode or in a higher performance write-back mode. The write-back cache mode was specifically designed to optimize performance of the CPU core by eliminating bus bottlenecks caused by unnecessary external write cycles. This write-back architecture is especially effective in improving performance of the clock-tripled ST486DX4 CPU.

Traditional write-through cache architectures require that all writes to the cache also update external memory simultaneously. These unnecessary write cycles create bottlenecks which result in CPU stalls and adversely impact performance. In contrast, a write-back architecture allows data to be written to the cache without updating external memory. With a write-back cache, external write cycles are only required when a cache miss occurs, a modified line is replaced in the cache, or when an external bus master requires access to data.

The ST486DX4 cache is an 8-KByte unified instruction and data cache implemented using a four-way set associative architecture and a least recently used (LRU) replacement algorithm. The cache is designed for optimum performance in write-back mode, however, the cache can be operated in write-through mode. The cache line size is 16 bytes and new lines are only allocated during memory read cycles. Valid status is maintained on a 16-byte cache line basis, but modified or "dirty" status for write-back mode is maintained on a 4-byte (double-word) basis. Therefore, only the double-words that have been modified are written back to external memory when a line is replaced in the cache. The CPU core can access the cache in a single internal clock cycle for both reads and writes.

1.3 FPU Operations

Since the FPU is resident within the CPU, the overhead associated with external math coprocessor cycles is eliminated. If the FPU is not in use, the FPU is automatically powered down. This feature reduces overall power consumption.

1.4 System Management Mode

System Management Mode (SMM) provides an additional interrupt and a separate address space that can be used for system power management or software transparent emulation of I/O peripherals. SMM is entered using the System Management Interrupt (SMI#) or SMINT instruction. While running in isolated SMM address space, the SMI interrupt routine can execute without interfering with the operating system or application programs.

After entering SMM, portions of the CPU state are automatically saved. Program execution begins at the base of SMM address space. The location and size of the SMM memory are pro- grammable within the ST486DX4. Eight SMM instructions have been

added to the 486 instruction set that permit software entry into SMM, as well as saving and restoring the total CPU state when in SMM mode.

1.5 Power Management

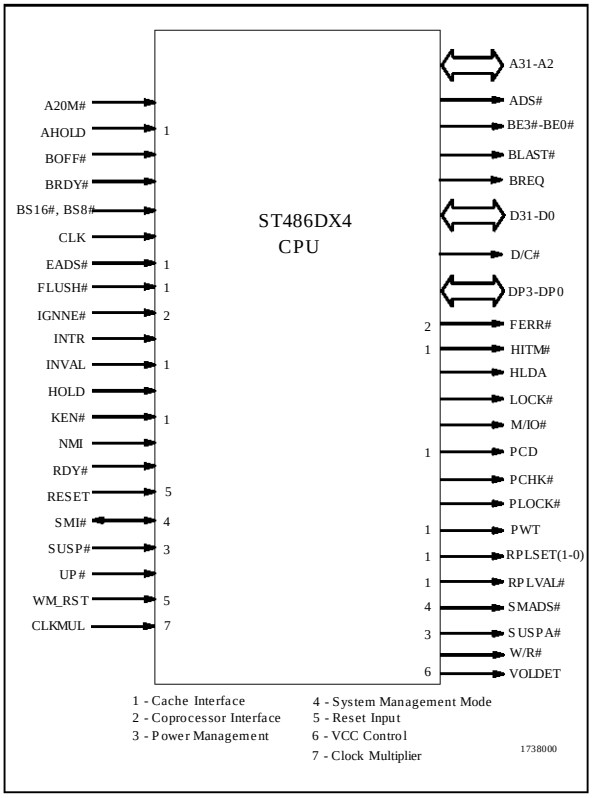
The ST486DX4 power management features allow for a dramatic improvement in battery life over systems designed with non-static 486 processors. During suspend mode the typical current consumption is less than 1 percent of the full operation current.

Suspend mode is entered by either a hardware or a software initiated action. Using the hardware method to initiate suspend mode involves a two-pin handshake between the SUSP# and SUSPA# signals. The software can initiate suspend mode through the execution of the HALT instruction. Once in suspend mode, the ST486DX4 power consumption is further reduced by stopping the external clock input. The resulting current draw is typically 450 µA. Since the ST486DX4 is static, no internal data is lost when the clock is stopped.

1.6 Signal Summary

The ST486DX4 signal set includes ten cache interface signals, two coprocessor interface signals, two power management signals, two system management mode signals, one power supply voltage control signal and one clock multiplier control signal.

Figure 1-1. ST486 DX4 Input & Output Signals.



1.7 VOLDET

The Voldet output signal is used by the system to detect that a low voltage part is in the CPU socket. It is permanently set to a logic 0 level for the low voltage part.

1.8 CLKMUL

The CLKMUL input signal is used to select the internal clock multiplication factor. The internal clock multiplication factor is 3X when CLKMUL is a logic 1 and 2X when CLKMUL is a logic 0.

CLKMUL has an internal pullup. If left unconnected, it will be driven to a logic 1.

1.9 Programable SMM Pin Interface

Following power-up or RESET, the ST486DX4 SMM interface pins are disabled. Once enabled, these two pins can either function as defined in the ST486DX/DX2 Databook(Order Code: DBST486DXST/1) (SMI# and SMADS#) or can be programmed to function with a protocol compatible with the 486 SL-enhanced CPUs (SMI#, SMIACT#).

1.10 SMM Mode Control Bit

Configuration register CCR3 bit 3 (SMM_Mode) controls the SMM interface mode. 0=ST mode, 1=SL-compatible mode, and the default state after reset is 0. If the SMI_Lock bit =0, the SMM_Mode may be modified. If the SMI_Lock bit is set, the SMM_Mode bit can no longer be modified. Once the SMI_lock bit is set, the CPU must be reset(RESET pin) in order to modify SMI_Lock and SMM_Mode.

1.11 SMM Pin Definitions

The two pins that change function in SL-compatible mode are SMI# and SMADS#. Table 1.1 lists the pin definitions for these two pins.

1.12 SMM Features Not Used with SL-Compatible Mode

The SMAC and SMAC functions controlled in Configuration Control Register 1 (CCR1) are disabled when in SL-compatible mode. If the SMI service routine accesses memory outside the defined SMM memory space, SMIACT# remains asserted. Also the SMINT instruction should not be used in SL-compatible mode.

Table 1.1. SMM Pin Definitions

ST MODE	SL-COMPATIBLE MODE
SMI#: Bidirectional System management Interrupt pin. Asserted by the system logic to request an SMI interrupt. Sampled by the CPU on each rising clock edge. Causes I/O trap to occur if sampled asserted at least two clocks prior to RDY# sampled asserted for an I/O cycle. Asserted by the CPU during execution of an SMI service routine or in response to SMINT if SMAC is set.	SMI#: System Management Interrupt input pin. Asserted by the system logic to request an SMI interrupt. Sampled by the CPU on each rising clock edge. SMI# is falling edge sensitive and causes an I/O trap to occur if sampled asserted at least three clocks prior to RDY#/BRDY# sampled for any I/O cycle.
SMADS#: SMI Address Strobe output used to indicate that the current bus cycle is an SMM memory access.	SMIACT#: SMI Active output asserted by the CPU during execution of an SMI service routine.

2.0 ELECTRICAL SPECIFICATIONS

Electrical specifications in this chapter are valid for the clock-doubled ST486DX2, and the clock-tripled ST486DX4. The ST486DX4 differs from the ST486DX2 in that the ST486DX4 internal CPU core operates at three times the frequency of the bus interface .

2.1 Electrical Connections

2.1.1 Power and Ground Connections and Decoupling

Due to the high frequency of operation of the ST486DX4, it is necessary to install and test this device using standard high frequency techniques. The high clock frequencies used in the ST486DX4 and its output buffer circuits can cause transient power surges when several output buffers switch output levels simultaneously. These effects can be minimized by filtering the DC power leads with low-inductance decoupling capacitors, using low impedance wiring, and by utilizing all of the VCC and GND pins.

2.1.2 Pull-Up/Pull-Down Resistors

Table 2-1 lists the input pins which are internally connected to pull-up and pull-down resistors. The pull-up resistors are connected to VCC and the pull-down resistors are connected to VSS. When unused, these inputs do not require connection to external pull-up or pull-down resistors. The SUSP# pin is unique in that it is connected to a pull-up resistor only when SUSP# is not asserted. It is recommended that the ADS#, LOCK# and SMI# output pins be connected to pull-up resistors, as indicated in Table 2-2. The external pull-ups guarantee that the signals remain negated during hold acknowledge states.

2.1.3 Unused Input Pins

All inputs not used by the system designer and not listed in Table 2-1 should be connected either to ground or to VCC. Connect active-high inputs to ground through a
20 kΩ (±10%) pull-down resistor and active-low inputs to VCC through a 20 kΩ (±10%) pull-up resistor to prevent possible spurious operation.

2.2 Absolute Maximum Ratings

The following table lists absolute maximum ratings for the ST486DX4 microprocessors. Stresses beyond those listed under Table 2-3 limits may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those listed under "Recommended Operating Conditions" Table 2-4 is possible. Exposure to conditions beyond Table 2-3 may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings (Table 2-3) may also result in reduced useful life and reliability.

Table 2-1. Pins Connected to Internal Pull-Up and Pull-Down Resistors

SIGNAL	RESISTOR
A20M#	20-kΩ pull-up
AHOLD	20-kΩ pull-down
BOFF#	20-kΩ pull-up
BS16#	20-kΩ pull-up
BS8#	20-kΩ pull-up
BRDY#	20-kΩ pull-up
EADS#	20-kΩ pull-up
FLUSH#	20-kΩ pull-up
IGNNE#	20-kΩ pull-up
INVAL	20-kΩ pull-up
KEN#	20-kΩ pull-up
RDY#	20-kΩ pull-up
UP#	20-kΩ pull-up
SUSP#	20-kΩ pull-up
WM_RST	20-kΩ pull-down
CLKMUL	20-kΩ pull-up

Table 2-2. Pins Requiring External Pull-Up Resistors

SIGNAL	EXTERNAL RESISTOR
ADS#	20-kΩ pull-up
LOCK#	20-kΩ pull-up

Table 2-3. Absolute Maximum Ratings

PARAMETER	ST486DX4V		UNITS	NOTES
	MIN	MAX		
Case Temperature	-65°	+110°	C	Power Applied
Storage Temperature	-65°	+150°	C	No Bias
Supply Voltage, VCC	-0.5	4.6	V	With Respect to V_{SS}
Voltage On Any Pin	-0.5	6.0	V	With Respect to V_{SS}
Input Clamp Current, I_{IK}		10	mA	Power Applied
Output Clamp Current, I_{OK}		25	mA	Power Applied

2.3 Recommended Operating Conditions

Table 2-4 presents the recommended operating conditions for the ST486DX4V device.

Table 2-4. Recommended Operating Conditions

PARAMETER	ST486DX4V		UNITS	NOTES
	MIN	MAX		
TC Case Temperature	0°	+85°	C	Power Applied
VCC Supply Voltage	3.3	3.6	V	With Respect to Vss
VIH High Level Input	2	5.5	V	
VIL Low Level Input	-0.3	0.8	V	
IOH Output Current (High)		-1	mA	VOH=VOH(MIN)
IOL Output Current (Low)		3	mA	VOL=VOL(MAX)

2.4 DC Characteristics

Table 2-5. DC Characteristics (at Recommended Operating Conditions)

PARAMETER	ST486DX4V		UNITS	NOTES
	MIN	MAX		
V_{OL} Output Low Voltage I_{OL} = 5 mA		0.35	V	
V_{OH} Output High Voltage I_{OH} = -1 mA	2.4		V	
I_{LI} Input Leakage Current For all pins except those listed in Table 2-1.		±15	µA	$0<V_{IN}<V_{CC}$
I_{IH} Input Leakage Current For all pins with internal pull-downs.		200	µA	V_{IH} = 2.4 V See Table 2-1.
I_{IL} Input Leakage Current For all pins with internal pull-ups		-400	µA	V_{IL} = 0.45 V See Table 2-1.
ICC Active ICC 66 MHz 75 MHz 80 MHz 100 MHz 120 MHz		 650 650 650 700 800	mA	Note 1
ICCSM Suspend Mode ICC 66 MHz 75 MHz 80 MHz 100 MHz 120 MHz	Typical: 14 16 16 18 18	 30 34 34 38 38	mA	Note 1, 3
I_{CCSS} Standby I_{CC} 0 MHz (Suspended/CLK Stopped)	Typical: 0.45	 1.1	mA	Note 4
C_{IN} Input Capacitance		20	pF	f_c = 1 MHz (Note 2)
C_{OUT} Output or I/O Capacitance		20	pF	f_c = 1 MHz (Note 2)
C_{CLK} CLK Capacitance		20	pF	f_c = 1 MHz (Note 2)

Notes: 1. MHz ratings refer to internal clock frequency.
2. Not 100% tested.
3. All inputs at 0.4 or V_{CC} - 0.4 (CMOS levels). All inputs held static except clock and all outputs unloaded (static I_{OUT} = 0 mA). Specification also valid for UP# = 0.
4. All inputs at 0.4 or V_{CC} - 0.4 (CMOS levels). All inputs held static and all outputs unloaded (static I_{OUT} = 0 mA).

2.5 AC Characteristics

Tables 2-6 through 2-9 list the AC characteristics including output delays, input setup requirements, input hold requirements and output float delays. These measurements are based on the measurement points identified in Figure 2-1 and Figure 2-2. The rising clock edge reference level V_{REF}, and other reference levels are shown in Table 2-6 below for the ST486DX4 Input or output signals must Figure 2-1 shows output delay (A and B) and input setup and hold times (C and D). Input setup and hold times (C and D) are specified minimums, defining the smallest acceptable sampling window a synchronous input signal must be stable for correct operation.

Table 2-6. Drive Level and Measurement Points for Switching Characteristics

SYMBOL	ST486DX4V	UNITS
V_{REF}	1.5	V
V_{IHD}	2.3	V
V_{ILD}	0	V
Note: Refer to Figure 2-1.		

Figure 2-1. Drive Level and Measurement Points for Switching Characteristics

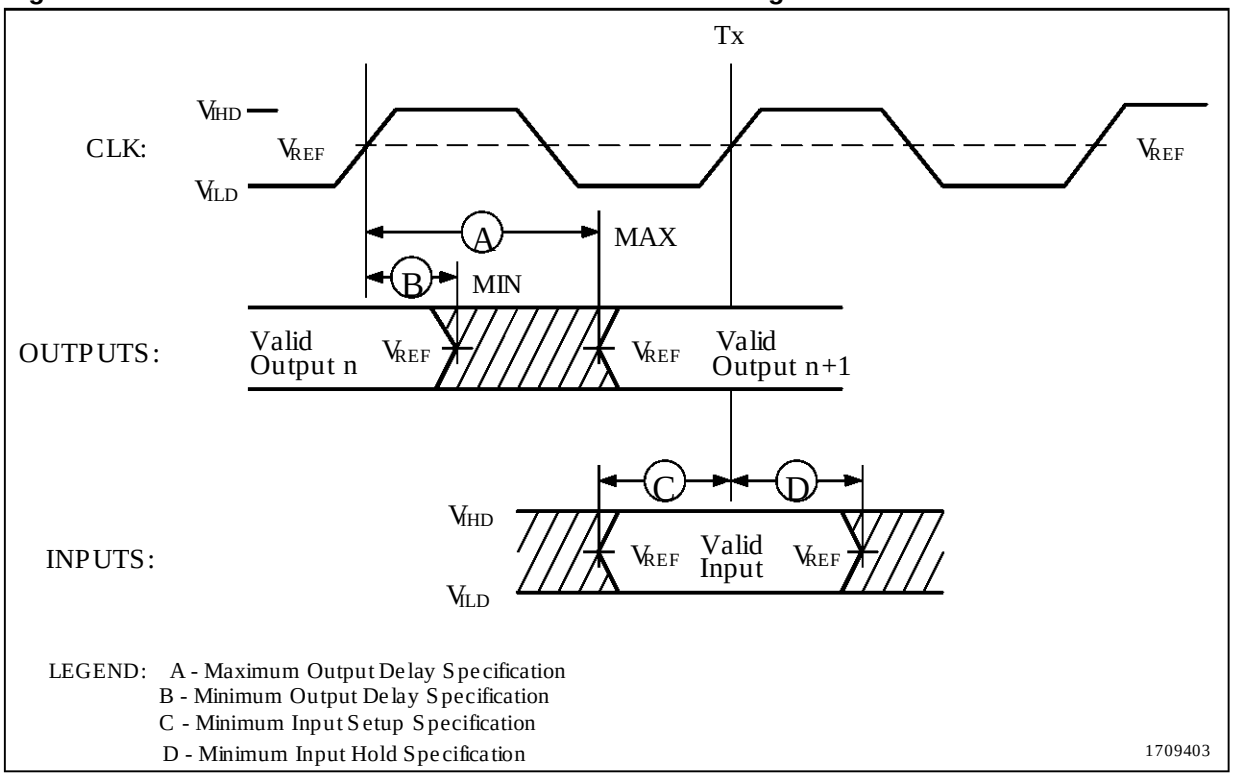


Figure 2-2. CLK Timing Measurement Points

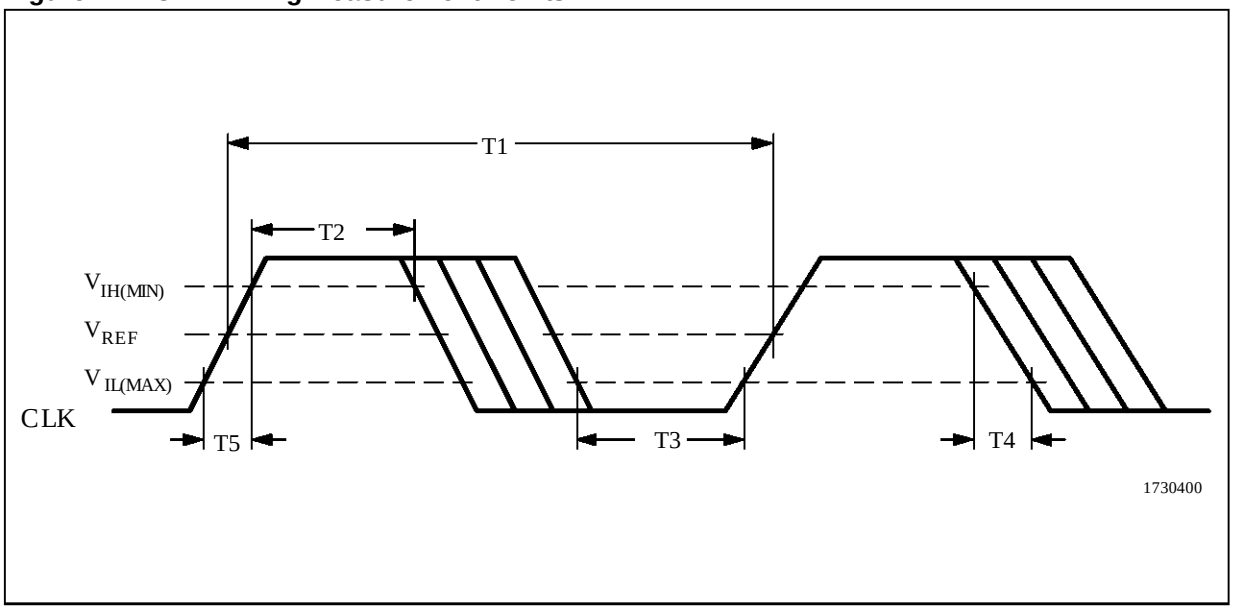


Table 2-7. AC Characteristics for ST486DX4V75
V_{cc} - 3.3 to 3.6V, T_{case}=0° to 85° C, C_L=50pF
External CLK = 25 MHz (Max.)

SYMBOL	PARAMETERS	MIN (ns)	MAX (ns)	FIGURE	NOTES
T1	CLK Period	40		2-2	
T2	CLK High Time	14		2-2	At 2 V
T3	CLK Low Time	14		2-2	$V_{IL(MAX)}$
T4	CLK Fall Time		4	2-2	2 V to $V_{IL(MAX)}$
T5	CLK Rise Time		4	2-2	$V_{IL(MAX)}$ to 2 V
T6	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, HLDA, FERR#, LOCK#, M/IO#, PCD, PWT, W/R# Valid Delay	3	19	2-6	
T6a	SMADS#, SMI# Valid Delay	3	19	2-6	
T7	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Float Delay		28	2-7	Note 1
T7a	SMADS#, SMI# Float Delay		28	2-7	Note 1
T8	PCHK# Valid Delay	3	24	2-5	
T8a	BLAST#, PLOCK# Valid Delay	3	24	2-6	
T8b	HITM#, RPLSET(1-0), RPLVAL#, SUSPA# Valid Delay	3	24	2-6	
T9	BLAST#, PLOCK# Float Delay		28	2-7	Note 1
T9a	RPLSET(1-0), RPLVAL# Float Delay		28	2-7	Note 1
T10	D31-D0, DP3-DP0 Write Data Valid Delay	3	20	2-6	
T11	D31-D0, DP3-DP0 Write Data Float Delay		28	2-7	Note 1
T12	EADS# Setup Time	8		2-3	
T12a	INVAL Setup Time	8		2-3	
T13	EADS# Hold Time	3		2-3	
T13a	INVAL Hold Time	3		2-3	
T14	BS16#, BS8#, KEN# Setup Time	8		2-3	
T15	BS16#, BS8#, KEN# Hold Time	3		2-3	
T16	BRDY#, RDY# Setup Time	8		2-4	
T17	BRDY#, RDY# Hold Time	3		2-4	
T18	AHOLD, HOLD Setup Time	10		2-3	
T18a	BOFF# Setup Time	10		2-3	
T19	AHOLD, BOFF#, HOLD Hold Time	3		2-3	
T20	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Setup Time	10		2-3	
T20a	SMI#, SUSP#, WM_RST Setup Time	10		2-3	
T21	A20M#, FLUSH#, INTR, IGNNE#, NMI, RESET Hold Time	3		2-3	
T21a	SMI#, SUSP#, WM_RST Hold Time	3		2-3	
T22	A31-A4, D31-D0, DP3-DP0 Read Setup Time	6		2-3, 2-4	
T23	A31-A4, D31-D0, DP3-DP0 Read Hold Time	3		2-3,2-4	
Note 1: Not 100% tested.					

Table 2-8 AC Characteristics for ST486DX4V10
V_{cc} - 3.3 to 3.6V, T_{case}=0° to 85° C, C_L=50pF
External CLK = 33 MHz (Max.)

SYMBOL	PARAMETERS	MIN (ns)	MAX (ns)	FIGURE	NOTES
T1	CLK Period	30		2-2	
T2	CLK High Time	11		2-2	At 2 V
T3	CLK Low Time	11		2-2	$V_{IL(MAX)}$
T4	CLK Fall Time		3	2-2	2 V to $V_{IL(MAX)}$
T5	CLK Rise Time		3	2-2	$V_{IL(MAX)}$ to 2 V
T6	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, FERR#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Valid Delay	3	14	2-6	
T6a	SMADS#, SMI# Valid Delay	3	14	2-6	
T7	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Float Delay		20	2-7	Note 1
T7a	SMADS#, SMI# Float Delay		20	2-7	Note 1
T8	PCHK# Valid Delay	3	14	2-5	
T8a	BLAST#, PLOCK# Valid Delay	3	20	2-6	
T8b	HITM#, RPLSET(1-0), RPLVAL#, SUSPA# Valid Delay	3	20	2-6	
T9	BLAST#, PLOCK# Float Delay		20	2-7	Note 1
T9a	RPLSET(1-0), RPLVAL# Float Delay		20	2-7	Note 1
T10	D31-D0, DP3-DP0 Write Data Valid Delay	3	14	2-6	
T11	D31-D0, DP3-DP0 Write Data Float Delay		20	2-7	Note 1
T12	EADS# Setup Time	5		2-3	
T12a	INVAL Setup Time	5		2-3	
T13	EADS# Hold Time	3		2-3	
T13a	INVAL Hold Time	3		2-3	
T14	BS16#, BS8#, KEN# Setup Time	6		2-3	
T15	BS16#, BS8#, KEN# Hold Time	3		2-3	
T16	BRDY#, RDY# Setup Time	5		2-4	
T17	BRDY#, RDY# Hold Time	3		2-4	
T18	AHOLD, HOLD Setup Time	6		2-3	
T18a	BOFF# Setup Time	7		2-3	
T19	AHOLD, BOFF#, HOLD Hold Time	3		2-3	
T20	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Setup Time	5		2-3	
T20a	SMI#, SUSP#, WM_RST Setup Time	5		2-3	
T21	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Hold Time	3		2-3	
T21a	SMI#, SUSP#, WM_RST Hold Time	3		2-3	
T22	A31-A4, D31-D0, DP3-DP0 Read Setup Time	5		2-3, 2-4	
T23	A31-A4, D31-D0, DP3-DP0 Read Hold Time	3		2-3, 2-4	
Note 1: Not 100% tested.					

Table 2-9. AC Characteristics for ST486DX4V12
V_{cc} - 3.3 to 3.6V, T_{case}=0° to 85° C, C_L=50pF
External CLK = 40 MHz (Max.)

SYMBOL	PARAMETERS	MIN (ns)	MAX (ns)	FIGURE	NOTES
T1	CLK Period	25		2-2	
T2	CLK High Time	9		2-2	At 2 V
T3	CLK Low Time	9		2-2	$V_{IL(MAX)}$
T4	CLK Fall Time		3	2-2	2 V to $V_{IL(MAX)}$
T5	CLK Rise Time		3	2-2	$V_{IL(MAX)}$ to 2 V
T6	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, FERR#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Valid Delay	3	14	2-6	
T6a	SMADS#, SMI# Valid Delay	3	14	2-6	
T7	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Float Delay		19	2-7	Note 1
T7a	SMADS#, SMI# Float Delay		19	2-7	Note 1
T8	PCHK# Valid Delay	3	14	2-5	
T8a	BLAST#, PLOCK# Valid Delay	3	16	2-6	
T8b	HITM#, RPLSET(1-0), RPLVAL#, SUSPA# Valid Delay	3	16	2-6	
T9	BLAST#, PLOCK# Float Delay		16	2-7	Note 1
T9a	RPLSET(1-0), RPLVAL# Float Delay		16	2-7	Note 1
T10	D31-D0, DP3-DP0 Write Data Valid Delay	3	14	2-6	
T11	D31-D0, DP3-DP0 Write Data Float Delay		19	2-7	Note 1
T12	EADS# Setup Time	5		2-3	
T12a	INVAL Setup Time	5		2-3	
T13	EADS# Hold Time	3		2-3	
T13a	INVAL Hold Time	3		2-3	
T14	BS16#, BS8#, KEN# Setup Time	6		2-3	
T15	BS16#, BS8#, KEN# Hold Time	3		2-3	
T16	BRDY#, RDY# Setup Time	5		2-4	
T17	BRDY#, RDY# Hold Time	3		2-4	
T18	AHOLD, HOLD Setup Time	6		2-3	
T18a	BOFF# Setup Time	7		2-3	
T19	AHOLD, BOFF#, HOLD Hold Time	3		2-3	
T20	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Setup Time	5		2-3	
T20a	SMI#, SUSP#, WM_RST Setup Time	5		2-3	
T21	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Hold Time	3		2-3	
T21a	SMI#, SUSP#, WM_RST Hold Time	3		2-3	
T22	A31-A4, D31-D0, DP3-DP0 Read Setup Time	5		2-3,2-4	
T23	A31-A4, D31-D0, DP3-DP0 Read Hold Time	3		2-3,2-4	

Note 1: Not 100% tested.

Figure 2-3 . Input Setup and Hold Timing

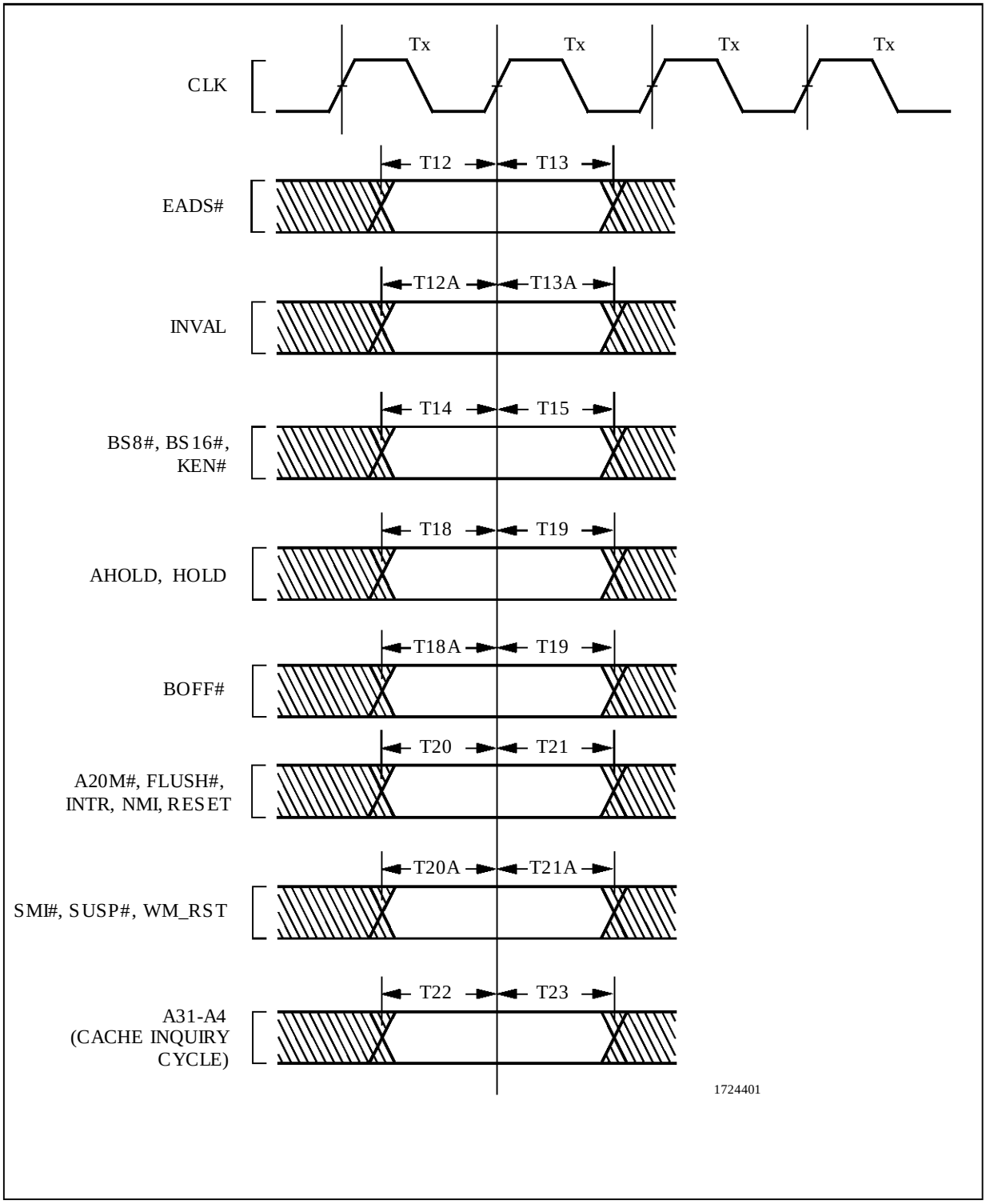


Figure 2-4 Input Setup and Hold Timing

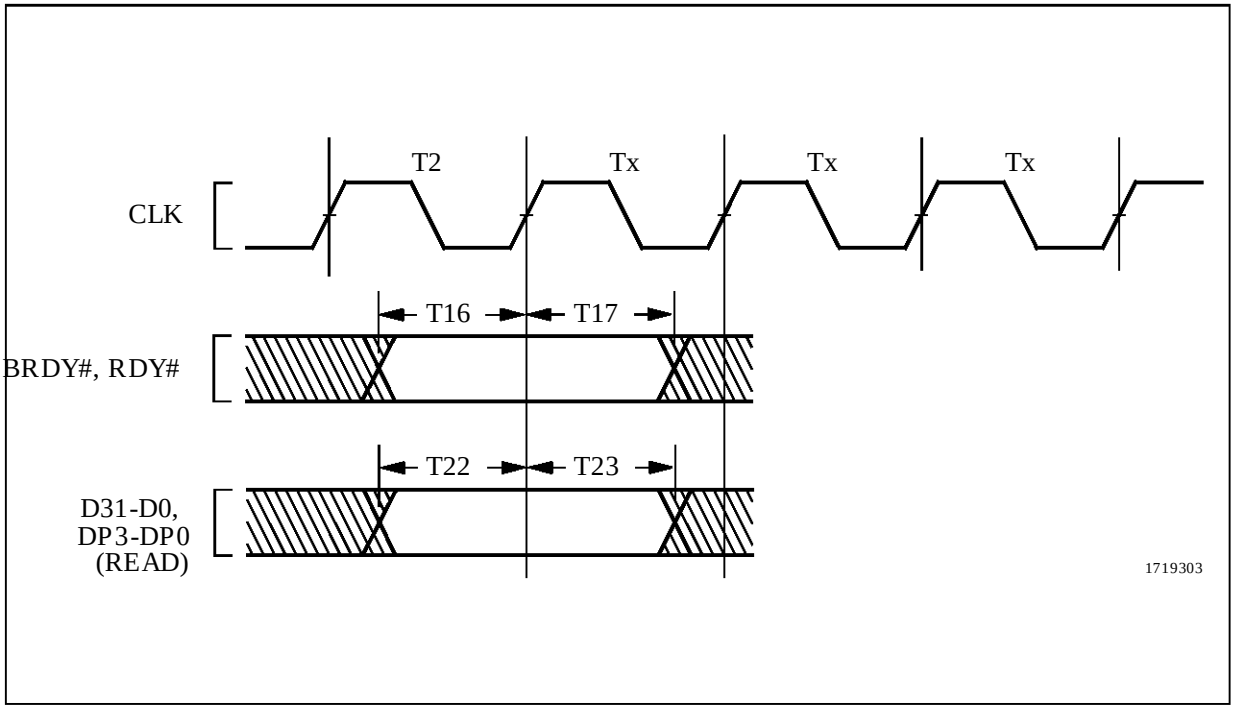


Figure 2-5. PCHK# Valid Delay Timing

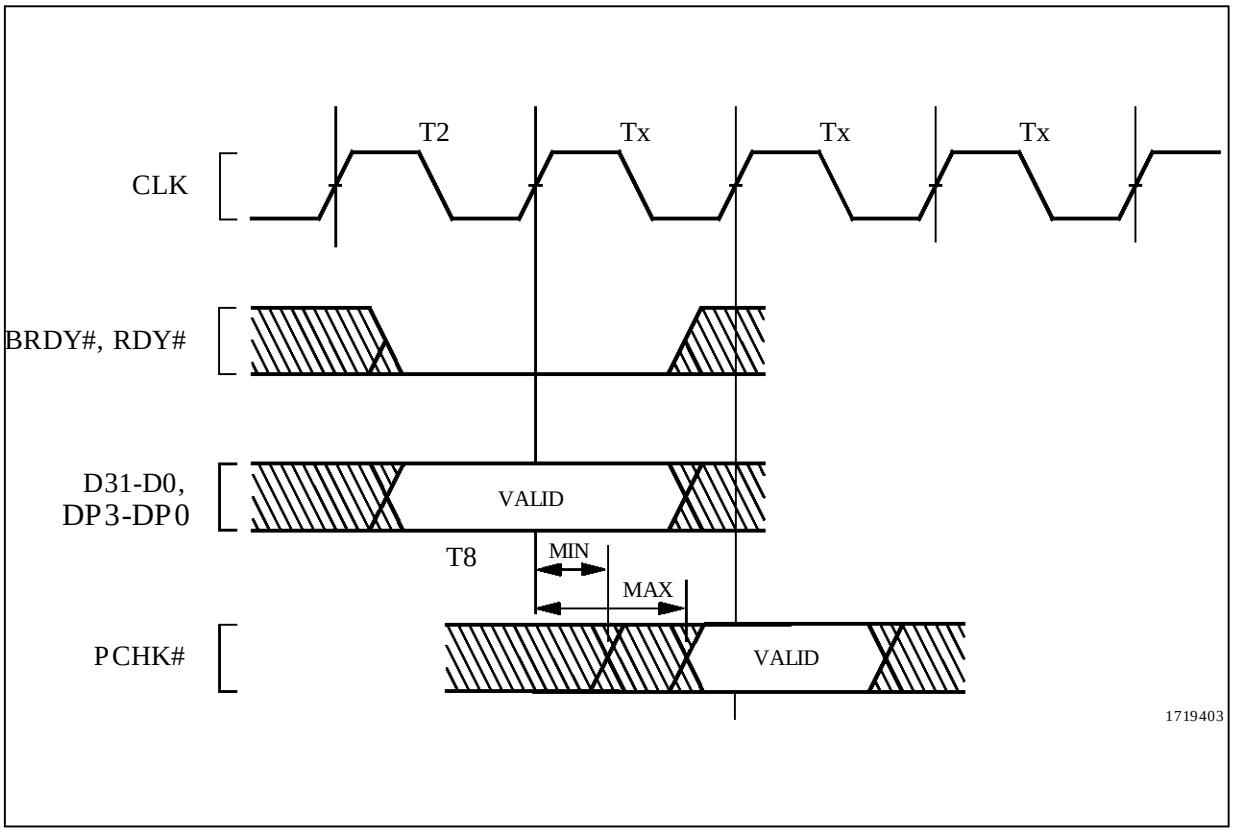


Figure 2-6 Output Valid Delay Timing.

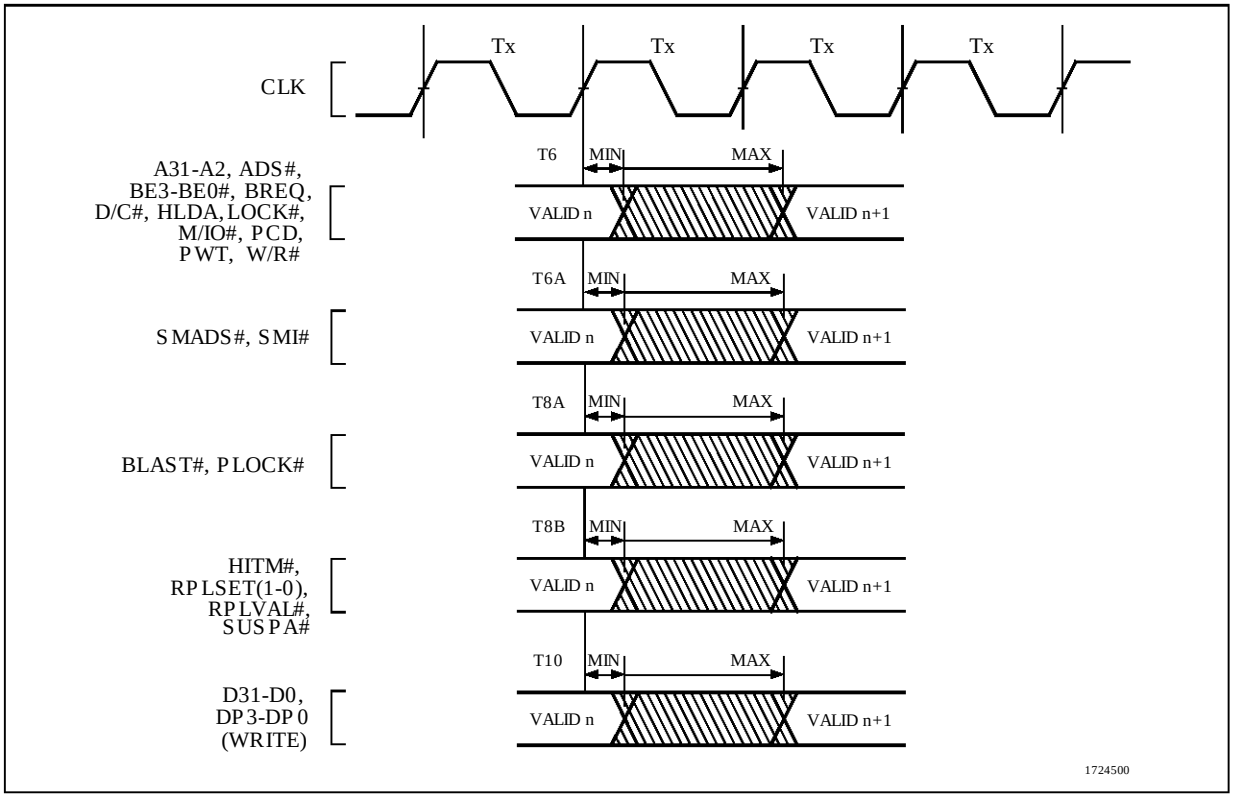
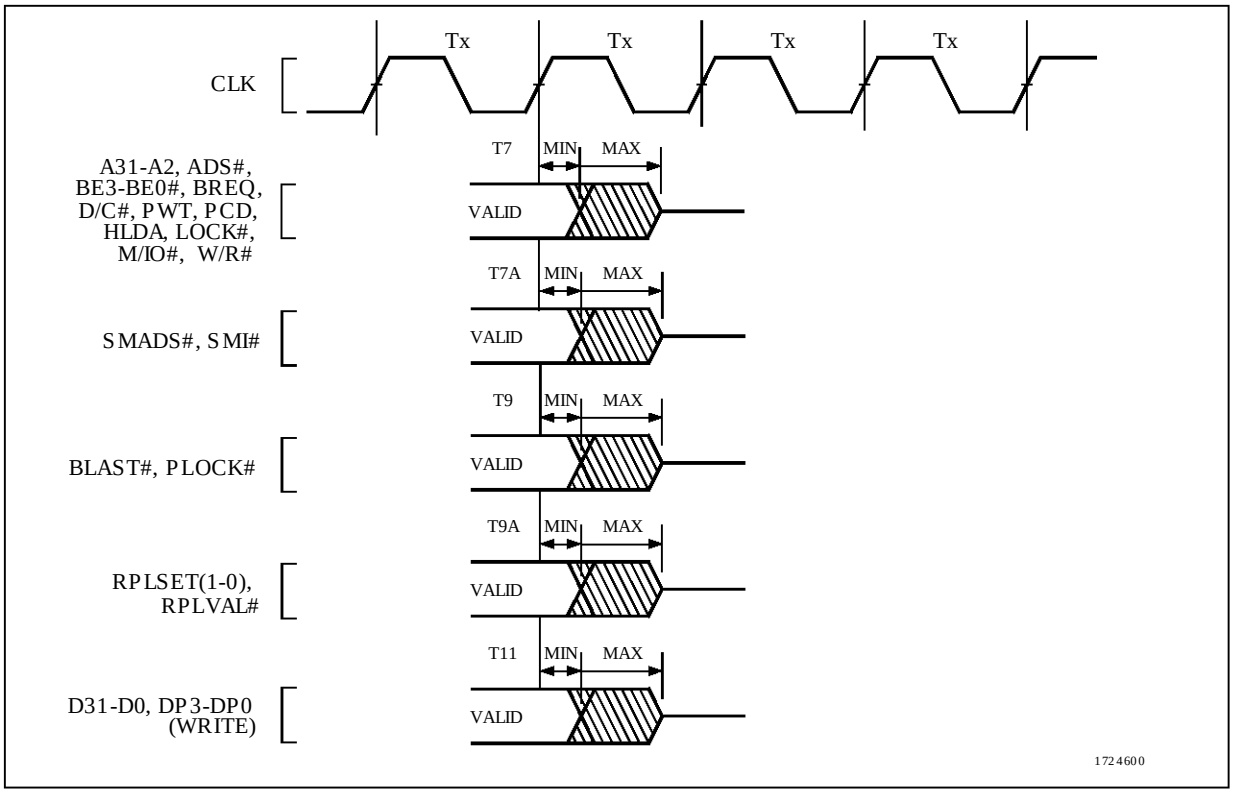


Figure 2-7. Output Valid Delay Timing



3.0 MECHANICAL SPECIFICATIONS

3.1 168-Pin Ceramic PGA & Plastic PGA Packages

The pin assignments for the ST486DX4V 168-pin PGA packages are shown in Figure 3-1. The pins are listed by signal name and pin number in Table 3-1.

Figure 3 - 1. 168-Pin Plastic & Ceramic PGA Packages Pin Assignments

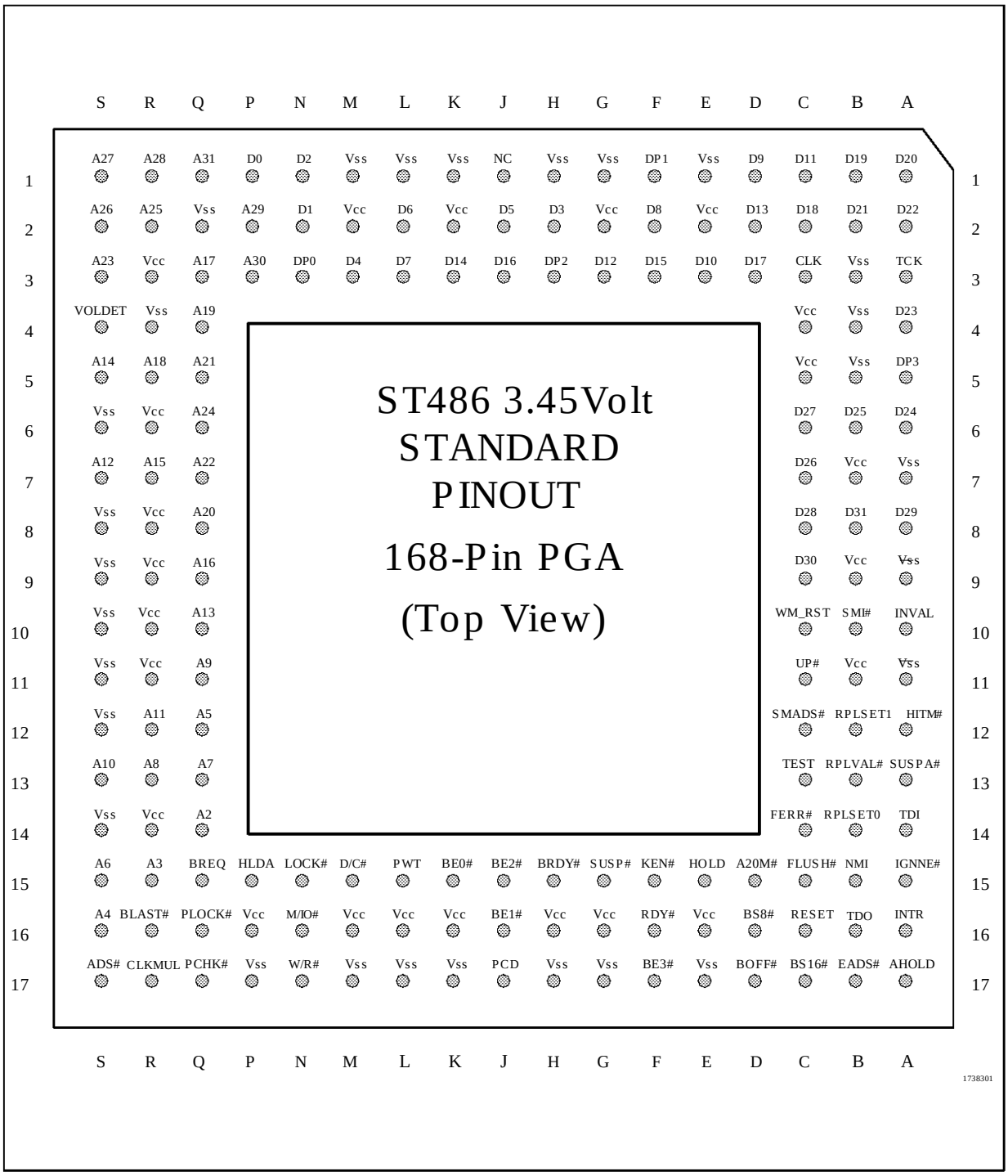


Table 3 - 1. ST486DX4 168-Pin PGA Packages Signal Names Sorted by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A1	D20	B12	RPLSET1	D17	BOFF#	J15	BE2#	P2	A29	R7	A15
A2	D22	B13	RPLVAL#	E1	VSS	J16	BE1#	P3	A30	R8	VCC
A3	TCK	B14	RPLSET0	E2	VCC	J17	PCD	P15	HLDA	R9	VCC
A4	D23	B15	NMI	E3	D10	K1	VSS	P16	VCC	R10	VCC
A5	DP3	B16	TD0	E15	HOLD	K2	VCC	P17	VSS	R11	VCC
A6	D24	B17	EADS#	E16	VCC	K3	D14	Q1	A31	R12	A11
A7	VSS	C1	D11	E17	VSS	K15	BE0#	Q2	VSS	R13	A8
A8	D29	C2	D18	F1	DP1	K16	VCC	Q3	A17	R14	VCC
A9	VSS	C3	CLK	F2	D8	K17	VSS	Q4	A19	R15	A3
A10	INVAL	C4	VCC	F3	D15	L1	VSS	Q5	A21	R16	BLAST#
A11	VSS	C5	VCC	F15	KEN#	L2	D6	Q6	A24	R17	CLKMUL
A12	HITM#	C6	D27	F16	RDY#	L3	D7	Q7	A22	S1	A27
A13	SUSPA#	C7	D26	F17	BE3#	L15	PWT	Q8	A20	S2	A26
A14	TDI	C8	D28	G1	VSS	L16	VCC	Q9	A16	S3	A23
A15	IGNNE#	C9	D30	G2	VCC	L17	VSS	Q10	A13	S4	VOLDET
A16	INTR	C10	WM_RST	G3	D12	M1	VSS	Q11	A9	S5	A14
A17	AHOLD	C11	UP#	G15	SUSP#	M2	VCC	Q12	A5	S6	VSS
B1	D19	C12	SMADS#	G16	VCC	M3	D4	Q13	A7	S7	A12
B2	D21	C13	TEST	G17	VSS	M15	D/C#	Q14	A2	S8	VSS
B3	VSS	C14	FERR#	H1	VSS	M16	VCC	Q15	BREQ	S9	VSS
B4	VSS	C15	FLUSH#	H2	D3	M17	VSS	Q16	PLOCK#	S10	VSS
B5	VSS	C16	RESET	H3	DP2	N1	D2	Q17	PCHK#	S11	VSS
B6	D25	C17	BS16#	H15	BRDY#	N2	D1	R1	A28	S12	VSS
B7	VCC	D1	D9	H16	VCC	N3	DP0	R2	A25	S13	A10
B8	D31	D2	D13	H17	VSS	N15	LOCK#	R3	VCC	S14	VSS
B9	VCC	D3	D17	J1	NC	N16	M/IO#	R4	VSS	S15	A6
B10	SMI#	D15	A20M#	J2	D5	N17	W/R#	R5	A18	S16	A4
B11	VCC	D16	BS8#	J3	D16	P1	D0	R6	VCC	S17	ADS#

Figure 3 -2. 168 pin Ceramic or Plastic PGA package

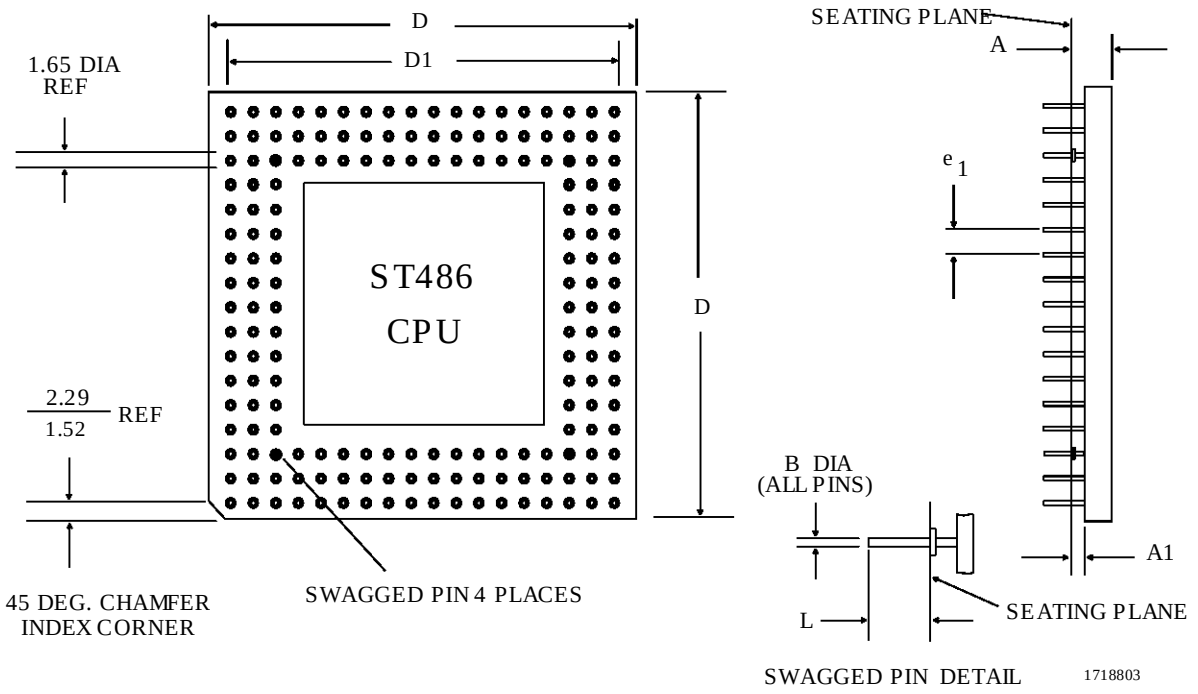


Table 3 - 2. 168 Pin PGA Packages Dimensions

SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.65	4.57	0.140	0.180
A1	1.14	1.40	0.045	0.055
B	0.43	0.51	0.017	0.020
D	44.07	44.83	1.735	1.765
D1	40.51	40.77	1.595	1.605
e1	2.29	2.79	0.090	0.110
L	2.54	3.30	0.110	0.120

3.2 208 Lead QFP(Quad Flat Package)

The pin assignments for the ST486DX4 208 lead QFP package are shown in Figure 3-2. The pins are listed by signal name and pin number in Table 3-2.

Figure 3 - 3. 208-Lead QFP Package Pin Assignments

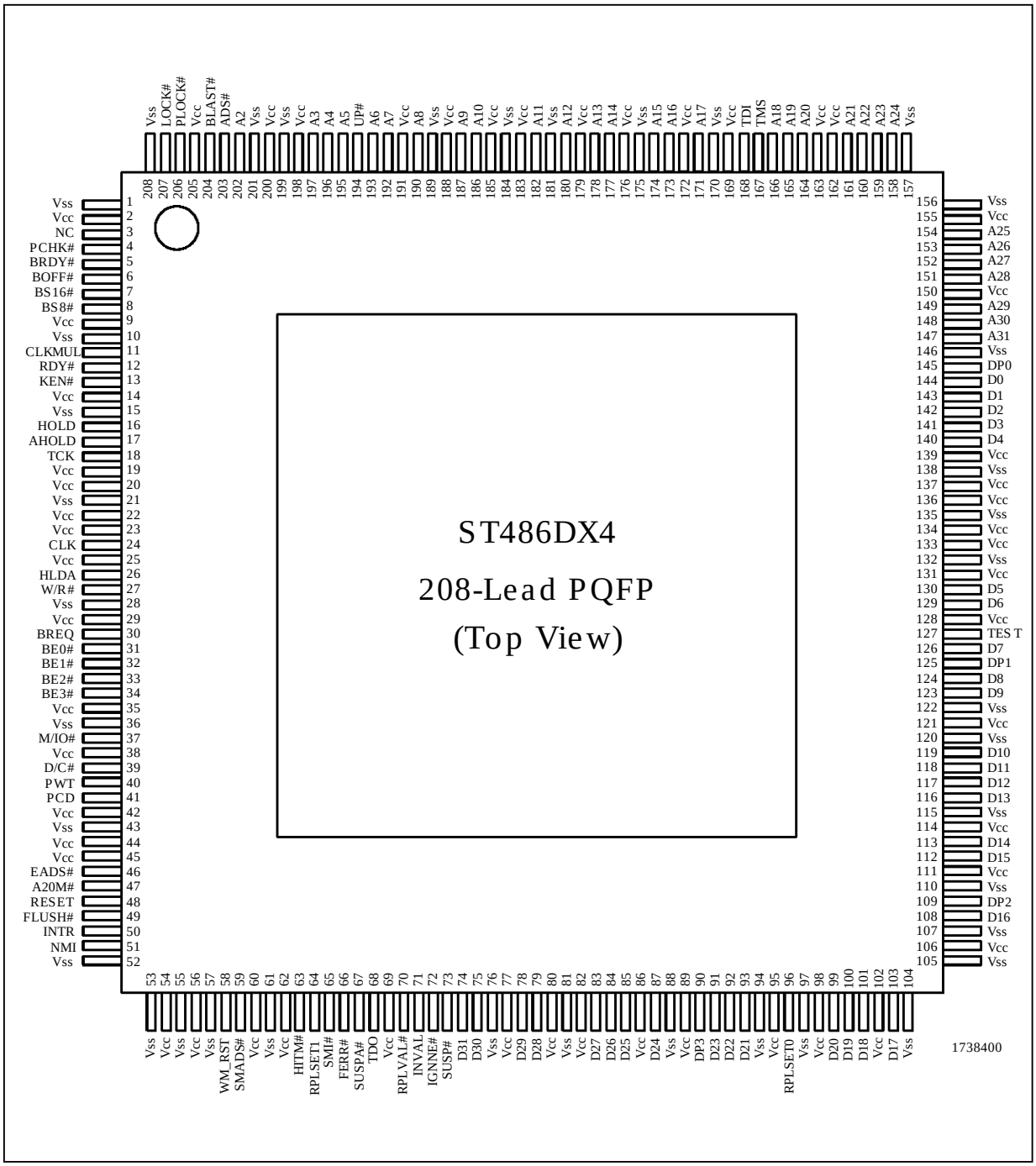


Table 3 - 3. ST486DX4 208 Lead QFP Package Signal Names Sorted by Pin Number

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	Vss	36	Vss	71	INVAL	106	Vcc	141	D3	176	Vcc
2	Vcc	37	M/IO#	72	IGNNE#	107	Vss	142	D2	177	A14
3	NC	38	Vcc	73	SUSP#	108	D16	143	D1	178	A13
4	PCHK#	39	D/C#	74	D31	109	DP2	144	D0	179	Vcc
5	BRDY#	40	PWT	75	D30	110	Vss	145	DP0	180	A12
6	BOFF#	41	PCD	76	Vss	111	Vcc	146	Vss	181	Vss
7	BS16#	42	Vcc	77	Vcc	112	D15	147	A31	182	A11
8	BS8#	43	Vss	78	D29	113	D14	148	A30	183	Vcc
9	Vcc	44	Vcc	79	D28	114	Vcc	149	A29	184	Vss
10	Vss	45	Vcc	80	Vcc	115	Vss	150	Vcc	185	Vcc
11	CLKMUL	46	EADS#	81	Vss	116	D13	151	A28	186	A10
12	RDY#	47	A20M#	82	Vcc	117	D12	152	A27	187	A9
13	KEN#	48	RESET	83	D27	118	D11	153	A26	188	Vcc
14	Vcc	49	FLUSH#	84	D26	119	D10	154	A25	189	Vss
15	Vss	50	INTR	85	D25	120	Vss	155	Vcc	190	A8
16	HOLD	51	NMI	86	Vcc	121	Vcc	156	Vss	191	Vcc
17	AHOLD	52	Vss	87	D24	122	Vss	157	Vss	192	A7
18	TCK	53	Vss	88	Vss	123	D9	158	A24	193	A6
19	Vcc	54	Vcc	89	Vcc	124	D8	159	A23	194	UP#
20	Vcc	55	Vss	90	DP3	125	DP1	160	A22	195	A5
21	Vss	56	Vcc	91	D23	126	D7	161	A21	196	A4
22	Vcc	57	Vss	92	D22	127	TEST	162	Vcc	197	A3
23	Vcc	58	WM_RST	93	D21	128	Vcc	163	Vcc	198	Vcc
24	CLK	59	SMADS#	94	Vss	129	D6	164	A20	199	Vss
25	Vcc	60	Vcc	95	Vcc	130	D5	165	A19	200	Vcc
26	HLDA	61	Vss	96	RPLSET0	131	Vcc	166	A18	201	Vss
27	W/R#	62	Vcc	97	Vss	132	Vss	167	TMS	202	A2
28	Vss	63	HITM#	98	Vcc	133	Vcc	168	TDI	203	ADS#
29	Vcc	64	RPLSET1	99	D20	134	Vcc	169	Vcc	204	BLAST#
30	BREQ	65	SMI#	100	D19	135	Vss	170	Vss	205	Vcc
31	BE0#	66	FERR#	101	D18	136	Vcc	171	A17	206	PLOCK#
32	BE1#	67	SUSPA#	102	Vcc	137	Vcc	172	Vcc	207	LOCK#
33	BE2#	68	TDO	103	D17	138	Vss	173	A16	208	Vss
34	BE3#	69	Vcc	104	Vss	139	Vcc	174	A15		
35	Vcc	70	RPLVAL#	105	Vss	140	D4	175	Vss		

Figure 3 - 4. 208 Lead Plastic QFP Package

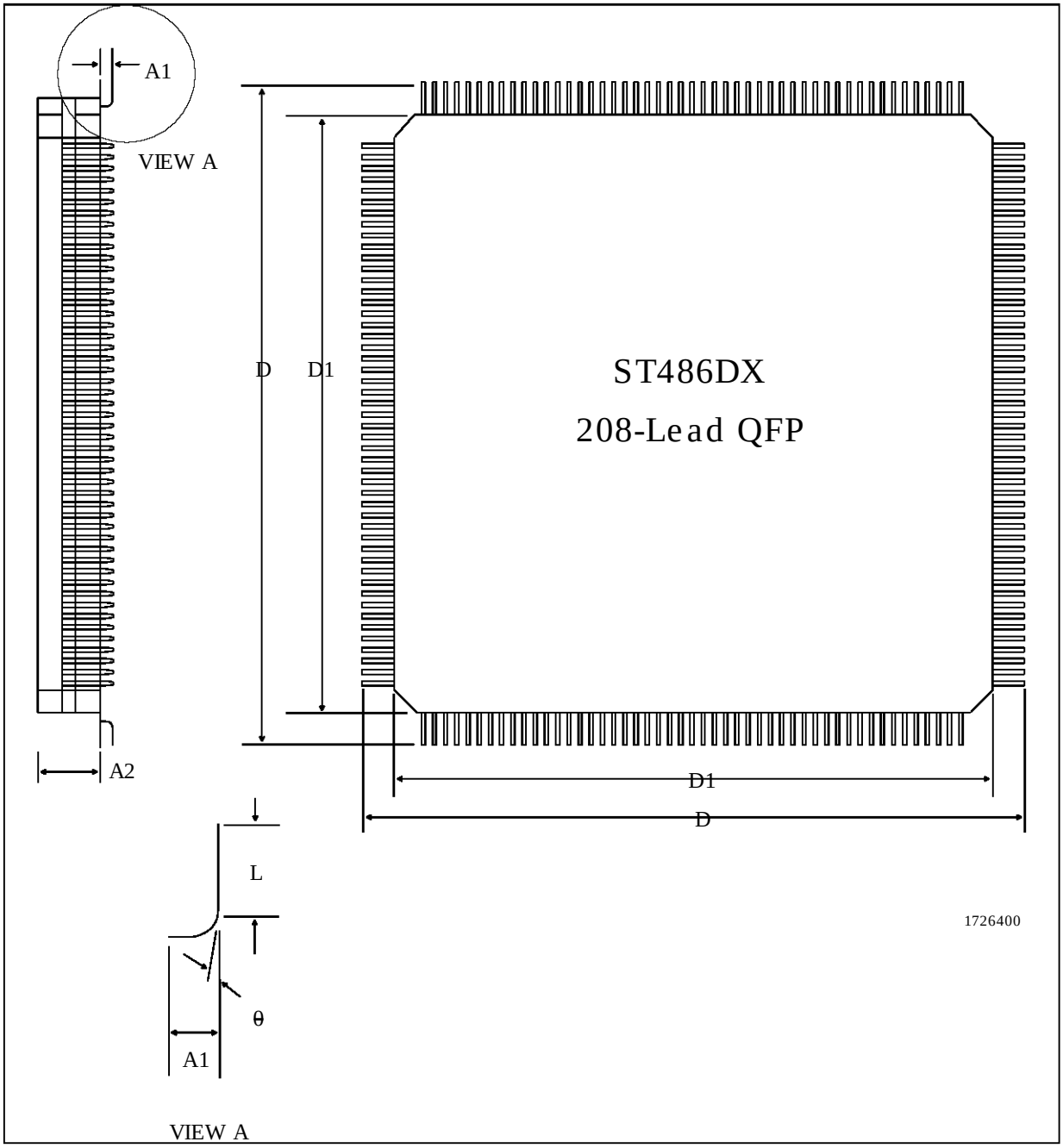


Table 3 - 4. 208 Lead Plastic QFP Package Dimensions

SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A1	0.13	0.33	0.005	0.013
A2	3.27	3.47	0.129	0.137
D	30.45	30.75	1.198	1.21
D1	27.9	28.1	1.098	1.106
L	0.4	0.6	0.015	0.023
θ	0°	7°	0°	7°

3.3 Thermal Characteristics

The ST486DX4V is designed to operate when case temperature is between 0° - 85°C. The case temperature is measured on the top center of the package. The maximum die temperature ($T_{J\ MAX}$) and the maximum ambient temperature (T_{aMAX}) can be calculated using the following equations.

$$T_{j\ MAX} = T_c + (P_{MAX} \times \theta_{jc})$$

$$T_{a\ MAX} = T_j - (P_{MAX} \times \theta_{ja})$$

where:

$T_{j\ MAX}$ = Maximum average junction temperature (°C)

T_c = Case temperature at top center of package (°C)

P_{MAX} = Maximum device power dissipation (W)

θ_{jc} = Junction-to-case thermal resistance (°C/W)

$T_{a\ MAX}$ = Maximum ambient temperature (°C)

T_j = Average junction temperature (°C)

θ_{ja} = Junction-to-ambient thermal resistance (°C/W)

3.4 PGA Packages

Table 3-5 lists the junction-to-ambient and junction-to-case thermal resistances for the PGA package. Table 3-6 lists the maximum ambient temperatures permitted for various clock frequencies and airflows for the PGA Package for Vcc equal to 3.6volts. Package dimensions for the heatsink used for the thermal analysis are shown in Figure 3-5 and Table 3-7.

Table 3 - 5. Ceramic & Plastic PGA Packages Thermal Resistance and Airflow

AIRFLOW (m/sec)	CERAMIC PGA THERMAL RESISTANCE (C/W)				PLASTIC PGA THERMAL RESISTANCE (C/W)			
	WITH HEATSINK		WITHOUT HEATSINK		WITH HEATSINK		WITHOUT HEATSINK	
	θja	θjc	θja	θjc	θja	θjc	θja	θjc
0	15	2.5	19	2.5	12	1.5	15	1.5
1	12	2.5	15	2.5	8	1.5	11.5	1.5
2	10	2.5	13	2.5	6.5	1.5	9.5	1.5
3	9.5	2.5	12	2.5	5.5	1.5	8.5	1.5
4	8.5	2.5	11	2.5	5	1.5	8	1.5

Table 3-6. Ceramic & Plastic PGA Packages Maximum Ambient Temperature (T_A) with V_{CC} = 3.6 V

PACKAGE	CPU INTERNAL CLOCK FREQUENCY	HEATSINK (Yes/No)	AIRFLOW (m/sec)				
			0	1	2	3	4
Ceramic Pin Grid Array	66 MHz	No	51 °C	60 °C	65° C	67 °C	69° C
	75 or 80 MHz	No	51 °C	60° C	65° C	67 °C	69° C
	100 MHz	No	47 °C	57° C	62 °C	65 °C	67 °C
	100 MHz	Yes	57 °C	65° C	70 °C	72° C	74 °C
	120 MHz	Yes	52 °C	60 °C	66 °C	68° C	71 °C
Plastic Pin Grid Array	66 MHz	No	60 °C	68 °C	73° C	75° C	76 °C
	75 or 80 MHz	No	60 °C	68 °C	73 °C	75 °C	76° C
	100 MHz	No	57 °C	66 °C	71 °C	74 °C	75 °C
	120 MHz	No	52 °C	62 °C	68 °C	71 °C	72 °C
	120 MHz	Yes	60 °C	72 °C	76 °C	79 °C	81 °C

Figure 3 - 5. Typical Heatsink for PGA Packages

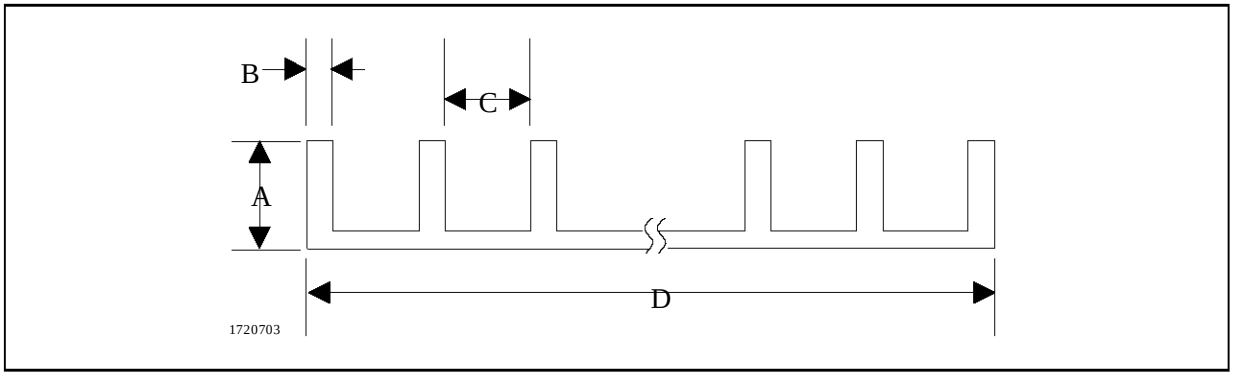


Table 3 - 7. Typical PGA Heatsink Dimensions

SYMBOL	MILLIMETERS	INCHES
A	6.1	0.24
B	1.3	0.05
C	4.8	0.19
D	39.1	1.54

QFP Package

Table 3-8 lists the junction-to-ambient and junction-to-case thermal resistances for the QFP package without a heat sink. Table 3-9 lists the maximum ambient temperatures permitted for various clock frequencies and airflows for the QFP Package for V_{CC} equal to 3.6 volts. These QFP package thermal characteristics assume that the package is soldered to a four-layer printed circuit board.

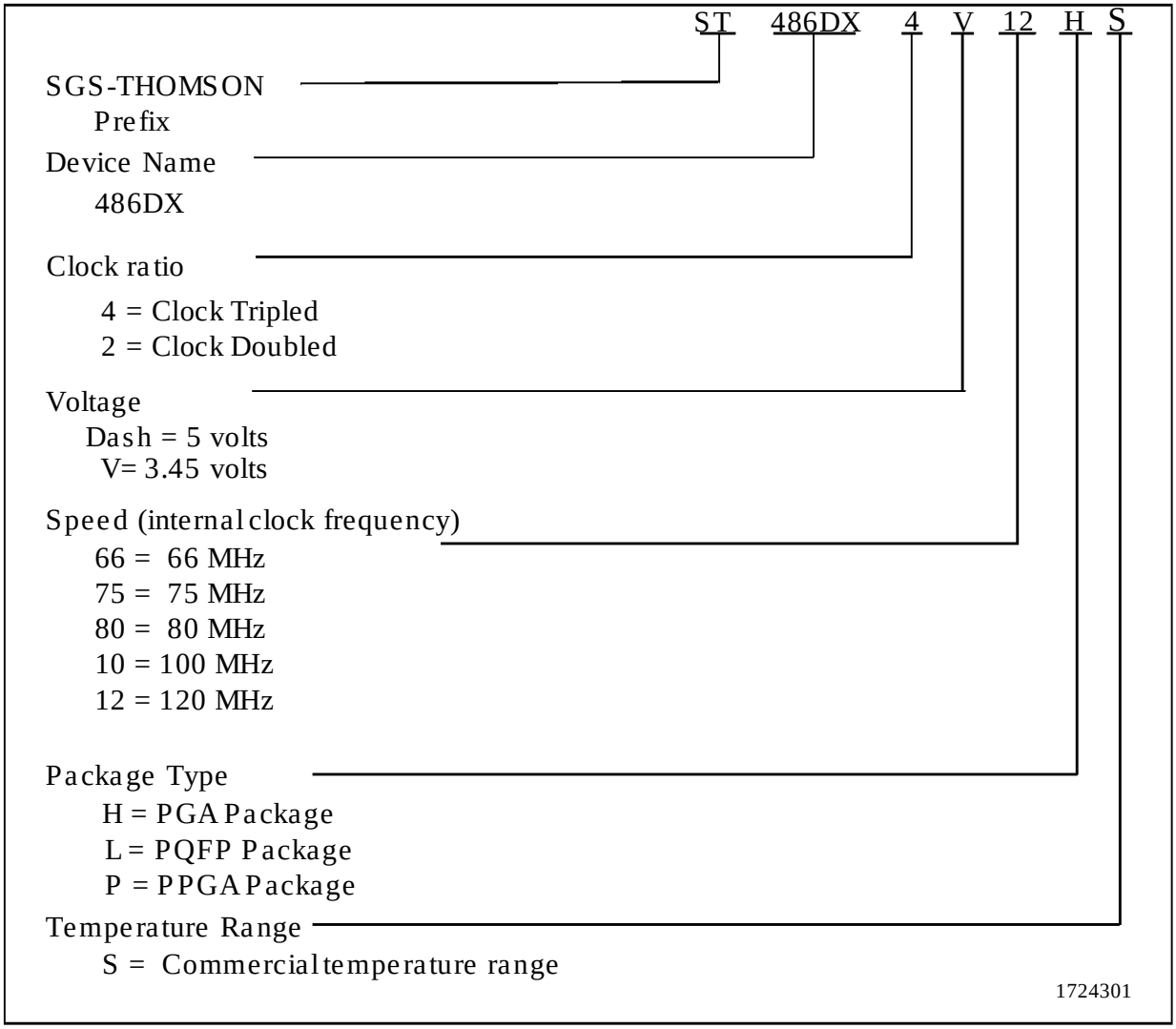
Table 3 - 8.

AIRFLOW	QFP THERMAL RESISTANCE (°C/W)	
	θ_{ja}	θ_{jc}
0 m/sec	21	3.5
1 m/sec	17	3.5

Table 3 - 9.

CPU INTERNAL CLOCK FREQUENCY	AIRFLOW	
	0 (m/sec)	1 (m/sec)
66 MHz	40° C	53 °C
75 MHz	34 °C	47 °C
100 MHz	30 °C	45 °C

Ordering Information*.



* Please contact your nearest SGS-THOMSON sales office to confirm availability of specific valid combinations and to check on newly released combinations.