

March 1992

Table 1 (continued): AMI LOW DENSITY FAMILY OF ROMS

Device Name	S63256	S63512	S631000/S631001	S632000	S634000
Process	CMOS	CMOS	CMOS	CMOS	CMOS
Capacity	256K/128K	512K	1 Meg	2 Meg	4 Meg
Organization	32K x 8	64K x 8	128K x 8	256K x 8	512K x 8
Compatible EPROM	27256	27512	27011/27010	27210	274001
Number of Pins	28	28	28/32	32	32
Plastic Dip Package Available	YES & 28 skinny	YES	YES	YES	YES
Ceramic Dip Package Available	YES	YES	YES	YES	YES
SOIC Plastic Package Available	YES	YES	YES	YES	NO
PLCC Package Available	YES 28& 32	YES	YES	YES	YES(44/68 Pin)
Temperature Range: C/I/M; 0 to 70°C/- 40 to 85°C/ - 55 to 125°C	C/I/M	C/I/M	C/I/M	C/I/M	C/I/M

Electrical Characteristics: $V_{CC} = +5V \pm 10\%$

Symbol	Parameter	Units	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{OL}	Output LOW Voltage ($I_{OL} = 3.2mA$)	V		0.4		0.4		0.4		0.4		0.4
V_{OH}	Output HIGH Voltage	V	2.4		2.4		2.4		2.4		2.4	
I_{OH}	Output HIGH Current			-1.0 mA		-1.0 mA		-1.0 mA		-1.0 mA		-1.0 mA
V_{IL}	Input LOW Voltage	V	-0.3	0.8	-0.3	0.8	-0.3	0.8	-0.3	0.8	-0.5	0.8
V_{IH}	Input HIGH Voltage	V	2.2	$V_{CC}+0.3$	2.2	$V_{CC}+0.3$	2.2	$V_{CC}+0.3$	2.2	$V_{CC}+0.3$	2.2	V_{CC}
I_{LI}	Input Leakage Current	μA	-1	1	-1	1	-1	1	-1	1	-1	1
I_{LO}	Output Leakage Current	μA	-10	10	-10	10	-10	10	-10	10	-10	10
I_{CC1}	Power Supply Current-TTL Active	mA	Note 1	20	Note 1	40	Note 1	40	Note 1	40	Note 1	40
I_{CC2}	Power Supply Current-CMOS Active	mA	Note 2	20	Note 2	35	Note 2	35	Note 2	35	Note 2	35
I_{SB1}	Power Supply Current TTL	mA	Note 3	1.0	Note 3	2	Note 3	2				
I_{SB2}	Power Supply Current CMOS	μA	Note 4	10/100	Note 4	10/100	Note 4	150	Note 4	150	Note 4	150
t_{AA}	Address Access Time Commercial Temp.	ns		90/120		100/120/150		100/120/150		150/200		150/200
	Industrial Temp.			120		120/150		120/150		200		200
	Mil Temp.			150		150		150		250		250
t_{ACE}	Chip Enable Access Time Commercial Temp.	ns		90/120		100/120/150		100/120/150		150/200		150/200
	Industrial Temp.			120		120/150		120/150		200		200
	Mil Temp.			150		150		150		250		250
t_{OE}	Output Enable Access Time Commercial Temp.	ns		30		50/80		50/80		70/80		70/80
	Industrial Temp.			40		85		85		85		90
	Mil Temp.			50		90		90		90		100
t_{CEO}	Disable Time From Chip Enable Commercial Temp.	ns	0	30	0	50	0	50	0	50	0	50
	Industrial Temp.		0	40	0	65	0	65	0	65	0	65
	Mil Temp.		0	50	0	70	0	70	0	70	0	70
t_{OEO}	Disable Time From Output Enable (Note 3) Commercial Temp.	ns	0	30	0	50	0	50	0	50	0	50
	Industrial Temp.		0	40	0	65	0	65	0	65	0	65
	Mil Temp.		0	50	0	70	0	70	0	70	0	70
t_{OH}	Output Hold Time Commercial Temp.	ns	0	0	0	0	0	0	0	0	0	0
	Industrial Temp.		0	0	0	0	0	0	0	0	0	0
	Mil Temp.		0	0	0	0	0	0	0	0	0	0
C_{in}	Input Capacitance (Note 5)	pf		7		7		5		5		5
C_{out}	Output Capacitance (Note 5)	pf		10		10		8		8		8

Notes:

1. TR = 150ns, duty = 100%, $V_I = 0.8V$ or 2.2V
2. TR = 150ns, duty = 100%, $V_I = Gnd$ or V_{CC}
3. Chip in Standby Mode, $V_I = V_{II}$ or V_{IH}
4. Chip in Standby Mode, $V_I = Gnd$ or V_{CC}
5. Capacitance is measured at $T_A = 25^\circ C$, $f = 1MHz$, $V_{in} = 0V$, $V_{out} = 0V$
6. In Notes 1 through 5 the Output Loads are Disconnected.