Bt454
Bt455

170 MHz Monolithic CMOS 16 Color Palette RAMDAC™

4

Distinguishing Features

- 170, 135, 110 MHz Operation
- 4:1 Multiplexed TTL Pixel Ports
- Triple 4-bit D/A Converters
- 16 Word Dual Port Color Palette
- 1 Dual Port Overlay Palette
- RS-343A-Compatible Outputs
- Standard MPU Interface
- +5 V CMOS Monolithic Construction
- 44-pin PLCC Package
- Typical Power Dissipation: 1 W

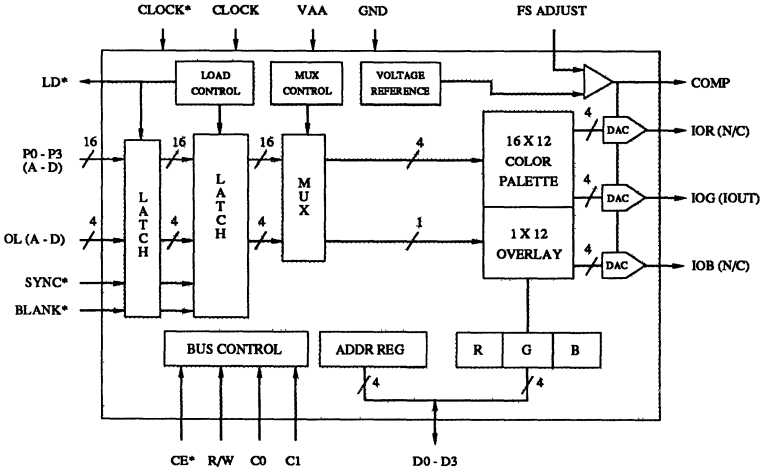
Applications

- High Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction
- Desktop Publishing

Related Products

- Bt451, Bt457, Bt458, Bt459 Bt460, Bt468

Functional Block Diagram



Product Description

The Bt454 and Bt455 are pin-compatible and software-compatible RAMDACs designed specifically for high-performance, high-resolution color graphics. The architecture enables the display of 1600 x 1200 bit-mapped color graphics (up to 4 bits per pixel plus 1 bit of overlay information), minimizing the use of costly ECL interfacing, as most of the high-speed (pixel clock) logic is contained on chip. The multiple pixel ports and internal multiplexing enables TTL-compatible interfacing (up to 42.5 MHz) to the frame buffer, while maintaining the 170-MHz video data rates required for sophisticated color graphics.

The Bt454 is a triple 4-bit video RAMDAC, and supports up to 17 simultaneous colors from a 4096 color palette. On-chip features include a temperature-compensated precision voltage reference, divide-by-four of the clock for load generation, color overlay capability, and a dual-port color palette RAM.

The Bt455 is a single-channel version of the Bt454, well-suited for high-performance monochrome or gray-scale applications.

The Bt454/455 generates RS-343A-compatible video signals, and is capable of driving doubly terminated 75 Ω coax directly, without requiring external buffering. Both the differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1/4 LSB over the full temperature range.

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Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt454/455 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color/overlay palettes. The dual-port color palette RAM and overlay register allow color updating without contention with the display refresh process.

As shown in Table 1, the C0 and C1 control inputs, in conjunction with the internal address register, specify which color palette RAM entry or overlay register will be accessed by the MPU. The address register is used to address the internal RAM, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

To write color data to the color palette RAM, the MPU loads the address register with the desired RAM location to be modified. The MPU performs three successive write cycles (4 bits each of red, green, and blue), using C0 and C1 to select the color palette RAM. Following the blue write cycle, the address register increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data.

To read color data from the color palette RAM, the MPU loads the address register with the desired RAM location to be read. The MPU performs three successive read cycles (4 bits each of red, green, and blue), using C0 and C1 to select the color palette RAM. Following the blue read cycle, the address register increments to the next location, which the MPU may read by simply reading another sequence of red, green, and blue data.

When accessing the color palette RAM, the address register resets to $0 following the blue read or write cycle to location $F.

To read from or write to the overlay register, the MPU, using C0 and C1 to select the overlay register, performs three successive read or write cycles (4 bits each of red, green, and blue). ADDR0–3 are not used.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 1. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 4 bits of the address register (ADDR0–3) are accessible to the MPU, and are used to address the color palette RAM locations.

Although the Bt455 uses only the green channel, it must still go through the count modulo 3 write sequence. The values loaded into the red and blue color palette should be $0.

When reading or writing the color values, the RAM or overlay register is accessed each time a 4-bit color value is read or written.

Although the color palette RAM and overlay register are dual-ported, if the pixel and overlay data is addressing the same palette entry being written to by the MPU, it is possible for one or more of the pixels on the display screen to be disturbed.

Figure 1 illustrates the MPU read/write timing when accessing the device.

Circuit Description (continued)

	Value	C1	C0	CE*	R/W	Addressed by MPU
ADDRa, b (counts modulo 3)	00		1			red value
	01		1			green value
	10		1			blue value
ADDR0–3 (counts binary)	$x	0	0	0	0	write to address register
	$0–$F	0	1	0	0	write to color palette RAM
	$x	1	0	0	0	D0–D3 ignored, 0 --> ADDRa, b
	$x	1	1	0	0	write to overlay register
	$x	0	0	0	1	read address register
	$0–$F	0	1	0	1	read color palette RAM
	$x	1	0	0	1	0 --> D0–D3, 0 --> ADDRa, b
	$x	1	1	0	1	read overlay register
	$x	x	x	1	x	3-state D0–D3

Table 1. Address Register (ADDR) Operation.

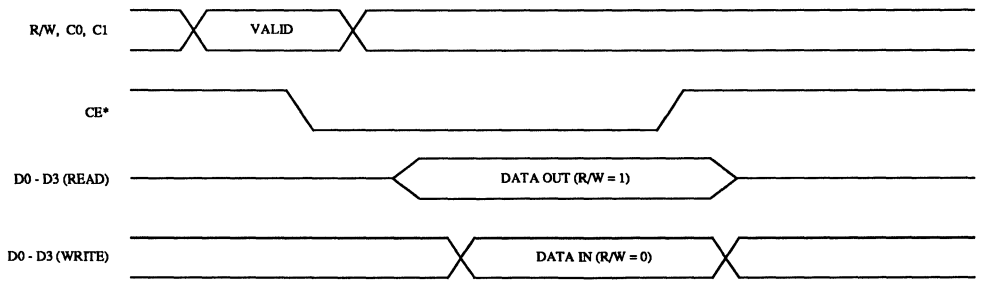


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at reasonable data rates (up to 42.5 MHz), the Bt454/455 incorporates internal latches and multiplexers. As illustrated in Figure 2, the SYNC*, BLANK*, P0–P3 {A–D}, and OL {A–D} inputs are latched on the rising edge of LDOUT. Note that with this configuration, the sync and blank timing will be recognized only with four pixel resolution. Typically, the LDOUT signal is used to clock external circuitry to generate the basic video timing and to clock the video DRAMs of the frame buffer.

The overlay inputs may have pixel timing, facilitating the use of an additional bit plane in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external character or cursor generation logic.

The Bt454/455 generates the LDOUT signal internally by dividing the clock by four. LDOUT is the setup-and-hold time reference for the pixel, overlay, sync, and blank inputs. It is recommended that LDOUT be buffered to clock the shift registers of the video DRAMs.

Once the pixel and overlay data are latched by LDOUT, they are internally multiplexed at the pixel clock rate. On each clock cycle, the Bt454/455 outputs color information based on the {A} inputs, followed by the {B} inputs, etc., until all four pixels have been output, at which point the cycle repeats.

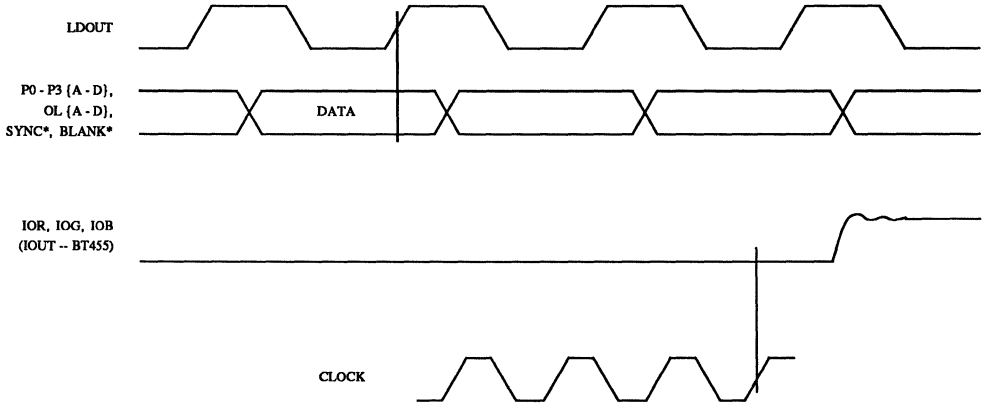


Figure 2. Video Input/Output Timing.

Circuit Description (continued)

Video Generation

Each clock cycle, 4bits of color information (P0–P3) and 1 bit of overlay information (OL) for each pixel are used to determine whether a color palette entry in the RAM or whether the overlay register is to provide color information. Note that P0 is the LSB when addressing the color palette RAM. Table 2 illustrates the truth table used for color selection.

Every clock cycle, the selected information is presented to the three 4-bit D/A converters.

The SYNC* and BLANK* inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 3.

The varying output current from each of the D/A converters produces a corresponding voltage level, which is used to drive the color CRT monitor. Note that only the green output (IOG) on the Bt454 contains sync information. Table 3 details how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt454/455 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current-steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

CRT Monitor Interface

The analog outputs are capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable, when soldered directly to a PC board. When the device is socketed, it is recommended that only a singly terminated 75 Ω load be used (unless air flow or heat sinking are available). Note that when driving a singly terminated 75 Ω load, the RSET value must be adjusted.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

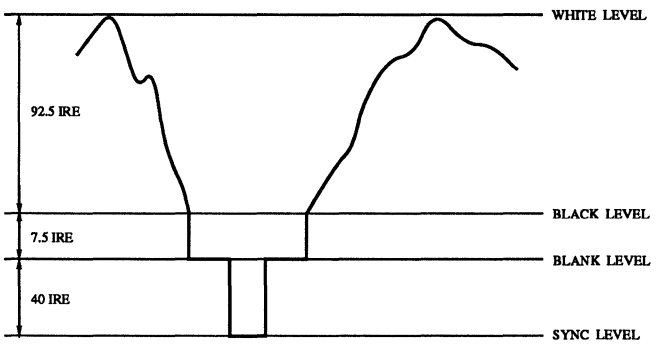
Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

OL	P0–P3	Addressed by frame buffer
0	$0	color palette entry $0
0	$1	color palette entry $1
:	:	:
0	$F	color palette entry $F
1	$x	overlay color

Table 2. Palette and Overlay Select Truth Table.

Circuit Description (continued)

IOR, IOB		IOG, IOUT	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly terminated load, RSET = 523 Ω. RS-343A levels and tolerances assumed on all levels.

Figure 3. Composite Video Output Waveforms.

Description	IOG, IOUT (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$F
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$0
BLACK - SYNC	1.44	1.44	0	1	$0
BLANK	7.62	0	1	0	$x
SYNC	0	0	0	0	$x

Note: Typical with full-scale IOG = 26.67 mA. RSET = 523 Ω.

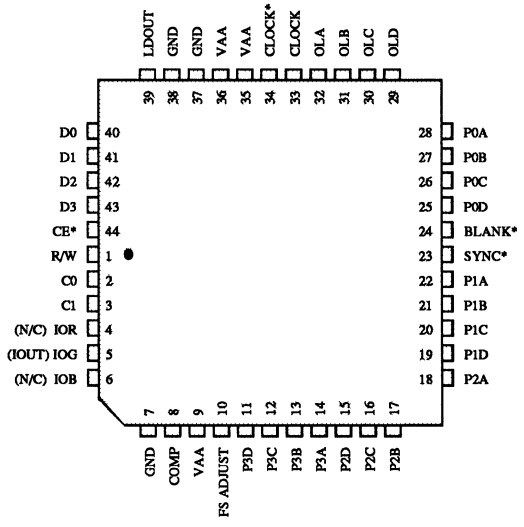
Table 3. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Table 3. It is latched on the rising edge of LDOUT. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the IOG output (see Figure 3). SYNC* does not override any other control or data input, as shown in Table 3; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of LDOUT. If sync information is not to be generated on the IOG output, this pin should be connected to GND.
LDOUT	Load control output (TTL compatible). The P0–P3 {A–D}, OL {A–D}, BLANK*, and SYNC* inputs are latched on the rising edge of LDOUT. LDOUT is internally generated by dividing the clock by four. LDOUT should have absolute minimal loading (one TTL load) to avoid display artifacts.
P0–P3 {A–D}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which one of the 16 entries in the color palette RAM is to be used to provide color information. Four consecutive pixels (up to 4 bits per pixel) are input through this port. They are latched on the rising edge of LDOUT. P0 is the LSB. Unused inputs should be connected to GND. Note that the {A} pixel is output first, followed by the {B} pixel, etc., until all four pixels have been output, at which point the cycle repeats.
OL {A–D}	Overlay select inputs (TTL compatible). These control inputs are latched on the rising edge of LDOUT, and specify which palette is to be used for color information. A logical zero indicates the color palette RAM is to provide color information, while a logical one indicates the overlay register is to provide color information. When accessing the overlay palette, the P0–P3 {A–D} inputs are ignored. Unused inputs should be connected to GND.
IOR, IOG, IOB, IOUT	Red, green, and blue video current outputs. These high-impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable (Figure 4). All outputs, whether used or not, should have the same output load. The Bt455 outputs IOUT rather than IOR, IOG, and IOB.
GND	Analog ground. All GND pins must be connected.
VAA	Analog power. All VAA pins must be connected.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full scale video signal (Figure 4). Note that the IRE relationships in Figure 3 are maintained, regardless of the full scale output current. The relationship between RSET and the full scale output current on IOG is: RSET (Ω) = 13,948 / IOG (mA) The full-scale output current on IOR and IOB for a given RSET is: IOR, IOB (mA) = 9,963 / RSET (Ω)

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and the adjacent VAA pin (Figure 4). Connecting the capacitor to VAA rather than to GND provides the highest possible low-frequency power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. *Refer to PC Board Layout Considerations for critical layout criteria.*
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE* (Figure 1). Care should be taken to avoid glitches on this edge-triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*. See Figure 1.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as illustrated in Table 1. They are latched on the falling edge of CE*.
D0 - D3	Data bus (TTL compatible). Data is transferred into and out of the device over this 4 bit bidirectional data bus. D0 is the least significant bit.



Note: Bt455 pin names are in parentheses.

PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS RAMDAC layout example found in Bt451/7/8 Evaluation Module Operation and Measurements, application note (AN-16). This application note can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt454/455 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A minimum of a 6-layer PC board is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer 2 the ground plane (preferably analog ground plane), layer 3 the analog power plane, using the remaining layers for digital traces and digital power supplies.

The optimum layout enables the Bt454/455 to be located as close to the power supply connector and as close to the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8 inch gap) and connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector to preserve digital noise margins during MPU read cycles. Thus, the ground tub isolation technique is constrained by the noise margin degradation during digital readback of the Bt454/455.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk.

The analog ground plane should include all Bt454/455 ground pins, reference circuitry (RSET resistors, etc.), power supply bypass circuitry for the Bt454/455, analog output traces, and the video output connector. The Bt455 no-connect (N/C) pins should be tied directly to ground.

Power Planes

Separate digital and analog power planes are necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt454/455 power pins, any reference circuitry, and COMP and reference decoupling. There should be at least a 1/8 inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 4. This bead should be located within 3 inches of the Bt454/455 and provides resistance to switching currents, acting as a resistance at high frequencies. A low resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged so that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor decoupling each of the two groups of VAA pins to GND. The capacitors should be placed as close as possible to the device.

The 10 µF capacitor is for low frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection.

PC Board Layout Considerations (continued)

A linear regulator to filter the analog power supply is recommended if the power supply noise is ≥ 200 mV. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10% of power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. Lead lengths should be minimized for best performance.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may help to fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt454/455 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission line mismatch will exist if the line length reflection time is greater than 1/4 the signal edge time, resulting in ringing, overshoot, and undershoot that can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (10 to 50 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10 to 50 Ω) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt454/455 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog outputs should have a source load resistor equal to the destination termination (via a clean isolated ground return path). The load resistor connection between the current output and GND should be as close as possible to the Bt454/455 to minimize reflections. Unused analog outputs should be connected to GND.

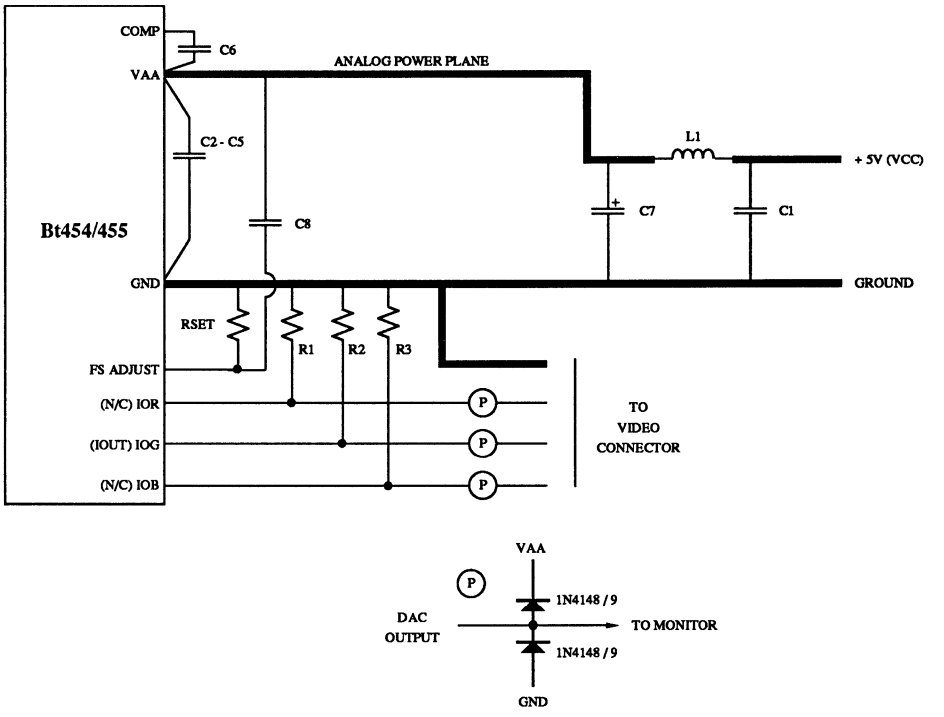
Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise.

Analog Output Protection

The Bt454/455 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 4 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1, C7	10 µF tantalum capacitor	Mallory CSR13G106KM
C2, C3, C6, C8	0.1 µF ceramic capacitor	Erie RPE110Z5U104M50V
C4, C5	0.01 µF ceramic chip capacitor	Johanson Dielectrics X7R500S41W103KP
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
RSET	523 Ω 1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt454/455.

Figure 4. Typical Connection Diagram and Parts List.

Application Information

LDOUT Termination

To reduce reflections on the LDOUT signal, it should be terminated at the point furthest from the Bt454/455. A 330 Ω resistor to VCC and a 470 Ω resistor to GND should work in most cases.

LDOUT should have absolute minimal loading (one TTL load) to avoid display artifacts.

Using Multiple Bt455s

When using multiple Bt455s, each Bt455 should have its own power plane ferrite bead.

Each Bt455 must still have its own individual RSET resistor, analog output termination resistors, power supply bypass capacitors, and COMP capacitor.

TTL Clock Interfacing

Figure 5 illustrates interfacing the Bt454/455 to a TTL clock. The MC10H116 is operated from a single +5 V supply. The resistor network attenuates the TTL levels to MECL input levels. Although not shown, both the CLOCK and CLOCK* lines require termination resistors (220 Ω resistor to VCC and 330 Ω resistor to GND), located as close as possible to the Bt454/455.

ECL Clock Generation

Due to the high clock rates at which the Bt454/455 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are designed to be generated by ECL logic operating at +5 V. Note that the CLOCK and CLOCK* inputs require termination resistors (typically a 220 Ω resistor to VCC and a 330 Ω resistor to GND), located as close as possible to the Bt454/455.

170 MHz applications require robust ECL clock signals with strong pull-down (~20 mA at VOH) and double termination for clock trace lengths greater than 2 inches.

The CLOCK and CLOCK* inputs must be differential signals due to the noise margins of the CMOS process. The Bt454/455 will not function using a single-ended CLOCK with CLOCK* connected to ground.

A 10K or 10KH ECL crystal oscillator that generates differential outputs, operating between +5 V and ground, may be interfaced directly to the B454/455, as shown in Figure 6. If the crystal oscillator generates only a single-ended output, a MC10H116 may be used to generate the differential clock signals, as illustrated in Figure 7. If the MC10H116 is not readily available, a MC10H101, MC10H105, or MC10H107 may be used.

Although ECL works well using a single +5 V supply, care must be taken to isolate the TTL power supply lines from the ECL power supply. Further information on ECL design may be obtained in the MECL Device Data Catalog and the MECL System Design Handbook, by Motorola.

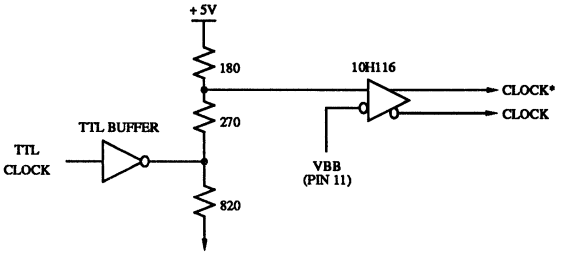


Figure 5. Interfacing the Bt454/455 to a TTL Clock.

Application Information (continued)

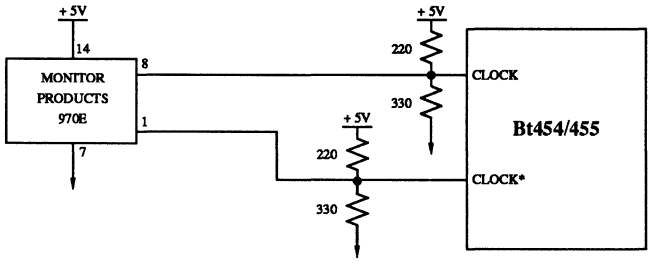


Figure 6. Interfacing to a Differential ECL Oscillator.

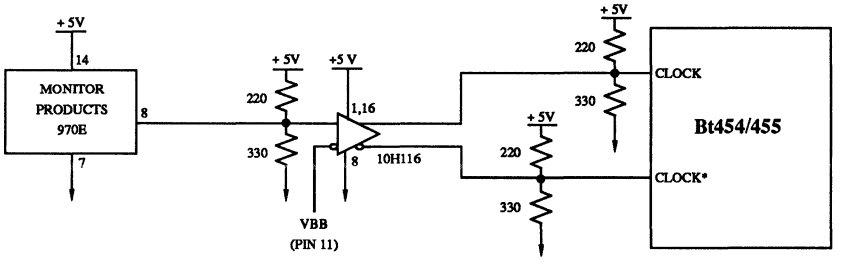


Figure 7. Interfacing to a Single-Ended ECL Oscillator.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ohms
FS ADJUST Resistor	RSET		523		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on Any Signal Pin*		GND–0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		4	4	4	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1/4	LSB
Differential Linearity Error	DL			±1/4	LSB
Gray Scale Error				±10	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		10		pF
Clock Inputs (CLOCK, CLOCK*)					
Differential Input Voltage	ΔVIN	.6		6	Volts
Input High Current (Vin = 4.2 V)	IKIH			1	µA
Input Low Current (Vin = 3.2 V)	IKIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 4.2 V)	CKIN		10		pF
Digital Outputs					
Output High Voltage	VOH				
D0–D3 (IOH = –400 µA)		2.4			Volts
LDOUT (IOH = -12 mA)		2.4			Volts
Output Low Voltage	VOL				
D0–D3 (IOL = 3.2 mA)				0.4	Volts
LDOUT (IOL = 24 mA)				0.5	Volts
3-state Current (D0–D3)	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		16.81	19.05	21.30	mA
White Level Relative to Black		15.86	17.62	19.40	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG or IOUT		6.29	7.62	8.96	mA
Sync Level on IOG or IOUT		0	5	50	µA
LSB Size			1.175		mA
DAC-to-DAC Matching				5	%
Output Compliance	VOC	-1.0		+1.4	Volts
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		20		pF
Internal Reference Voltage	VREF	1.18	1.22	1.26	Volts
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR		0.5		%/%ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	170 MHz Devices			135 MHz Devices			110 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock Rate	Fmax			170			135			110	MHz
R/W, C0, C1 Setup Time	1	0			0			0			ns
R/W, C0, C1 Hold Time	2	15			15			15			ns
CE* Low Time	3	50			50			50			ns
CE* High Time	4	25			25			25			ns
CE* Asserted to Data Bus	5	10			10			10			ns
CE* Asserted to Data Valid	6			75			75			75	ns
CE* Negated to Data Bus 3-Stated	7			15			15			15	ns
Write Data Setup Time	8	35			35			35			ns
Write Data Hold Time	9	10			10			10			ns
LDOUT Pulse Width High	10	9			11.5			13			ns
LDOUT Pulse Width Low	11	9			11.5			13			ns
Clock to LDOUT	12	4	7.5	14.3	4	7.5	14.3	4	7.5	14.3	ns
Pixel and Control Setup Time	13	0			0			0			ns
Pixel and Control Hold Time	14	3			5			5			ns
Clock Cycle Time	15	5.88			7.4			9			ns
Clock Pulse Width High	16	2			3			3.6			ns
Clock Pulse Width Low	17	2			3			3.6			ns
Analog Output Delay	18		20			20			20		ns
Analog Output Rise/Fall Time	19		2			2			2		ns
Analog Output Settling Time*	20			6			9			9	ns
Clock and Data Feedthrough*			70			70			70		pV - sec
Glitch Impulse*			50			50			50		pV - sec
Analog Output Skew			0	2		0	2		0	2	ns
Pipeline Delay		6	6	6	6	6	6	6	6	6	Clocks
VAA Supply Current**	IAA		200	tbd		150	tbd		120	200	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. ECL input values are 3.2–4.2 volts, with input rise/fall times ≤ 2 ns, measured between 20% and 80% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D3 output load ≤ 75 pF. See timing notes in Figure 9. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (typ) at VAA = 5.0 V, TA = 20° C. IAA (max) at VAA = 5.25 V, TA = 0° C.

Timing Waveforms

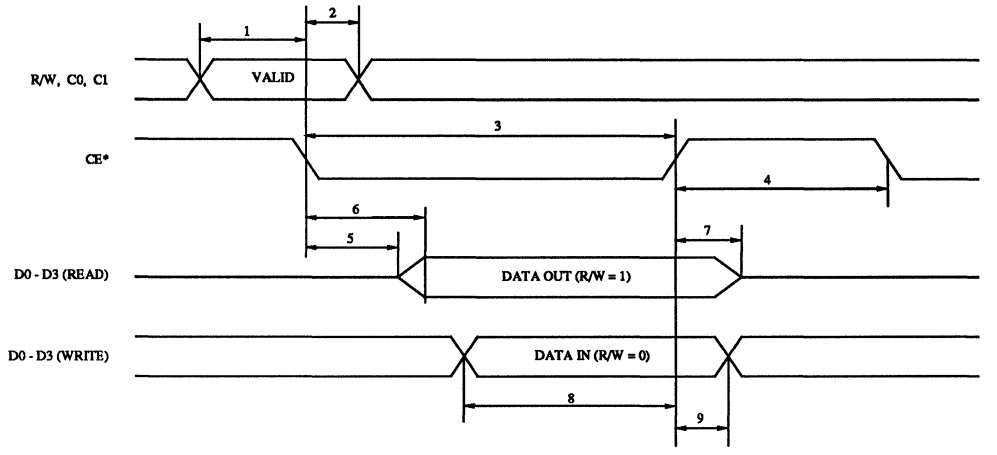
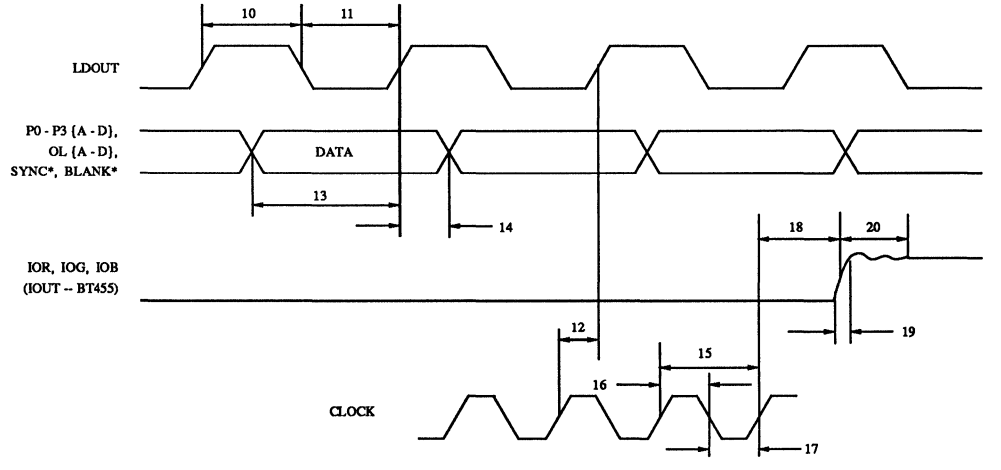


Figure 8. MPU Read/Write Timing Dimensions..



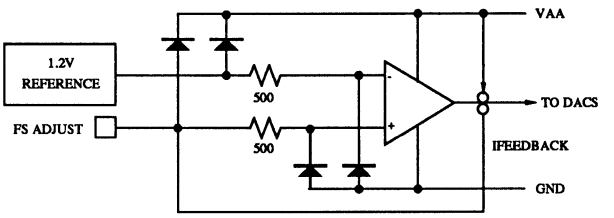
Note 1: Output delay time measured from 50% point of the rising clock edge to 50% point of full scale transition.

Note 2: Output settling time measured from 50% point of full-scale transition to output settling within ±1/4LSB.

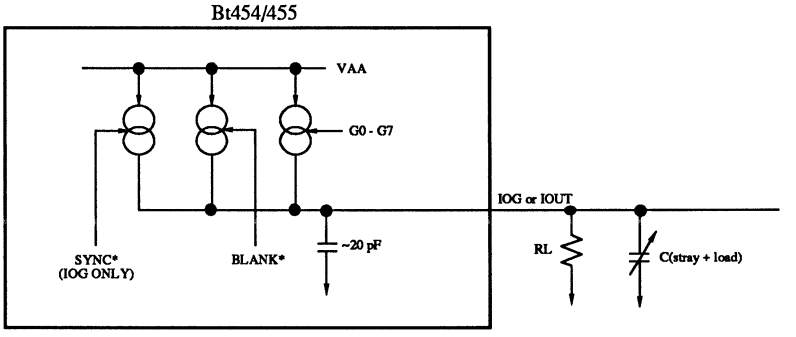
Note 3: Output rise/fall time measured between 10% and 90% points of full-scale transition.

Figure 9. Video Input/Output Timing.

Device Circuit Data



Equivalent Circuit of the Reference Amplifier.



Equivalent Circuit of the Current Output (IOG or IOUT).

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt454KPJ	110 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt454KPJ135	135 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt454KPJ170	170 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt455KPJ110	110 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt455KPJ135	135 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt455KPJ170	170 MHz	44-pin Plastic J-Lead	0° to +70° C

Revision History

Datasheet Revision	*Change from Previous Revision*
F	Note added to pin description and applications section that LDOUT should have absolute minimal loading (one TTL load) to avoid display artifacts.
G	Expanded PCB layout section.
H	Added Bt455 part and description.
I	Expanded ESD and PCB Layout sections.