Advance Information

This document contains information on a product under development. The parametric information contains target parameters and is subject to change.

Bt485

135 MHz Monolithic CMOS True-Color RAMDAC™

4

Distinguishing Features

- 135, 110, 85, 75 MHz Pipelined Operation
- 8:1, 4:1, 2:1, 1:1 Multiplexed Pixel Ports
- Separate 8-bit VGA Port
- 2-Times-Clock Multiplier
- 64 x 64 x 2 Programmable Cursor
- Triple 8-bit D/A Converters
- Three 256 x 8 Color Palette RAMs
- Three 3 x 8 Cursor Color Palettes
- Optional Sync on All Three Channels
- 0 or 7.5 IRE Blanking Pedestal
- Voltage Reference
- Analog Output Comparators
- Antisparkle Circuitry
- Power-Down Mode
- VRAM Shift Clock
- VGA Support in a True-Color Window
- 84-pin PLCC Package

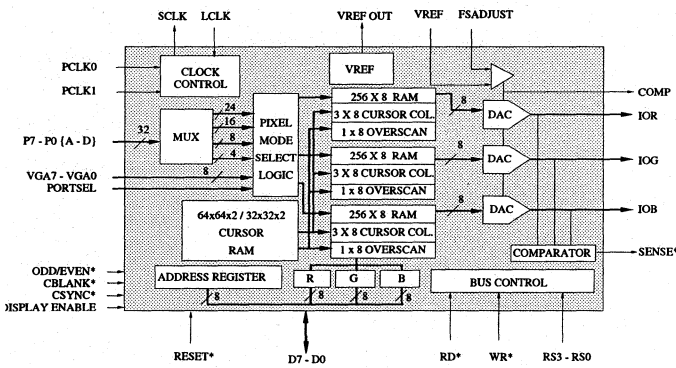
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing

Related Products

- Bt484

Functional Block Diagram



Product Description

The Bt485 RAMDAC is designed specifically for high-performance color graphics. The Bt485 is pin-compatible and functionally backwards- compatible to the Bt484.

Included are four byte-wide pixel input ports (multiplexed 4:1), three 256 x 8 color lookup tables with triple 8-bit video D/A converters (configurable for either 6-bit or 8-bit D/A converter operation), and a programmable 64 x 64 x 2 cursor with its own color palette.

The Bt485 may alternately be configured for a lower performance VGA mode, where 8 bits of VGA pixel data (from a VGA controller) are input through a separate VGA pixel port.

Several operational modes are supported by the 32 pins allocated for the P7:P0 port including 8-bit pseudo color, 16- and 24-bit true color, and various packed and sparse pixel formats. The color palette may be bypassed in any of the true-color modes.

The Bt485 generates RS-343A-compatible video signals into a doubly-terminated 75 Ω load.

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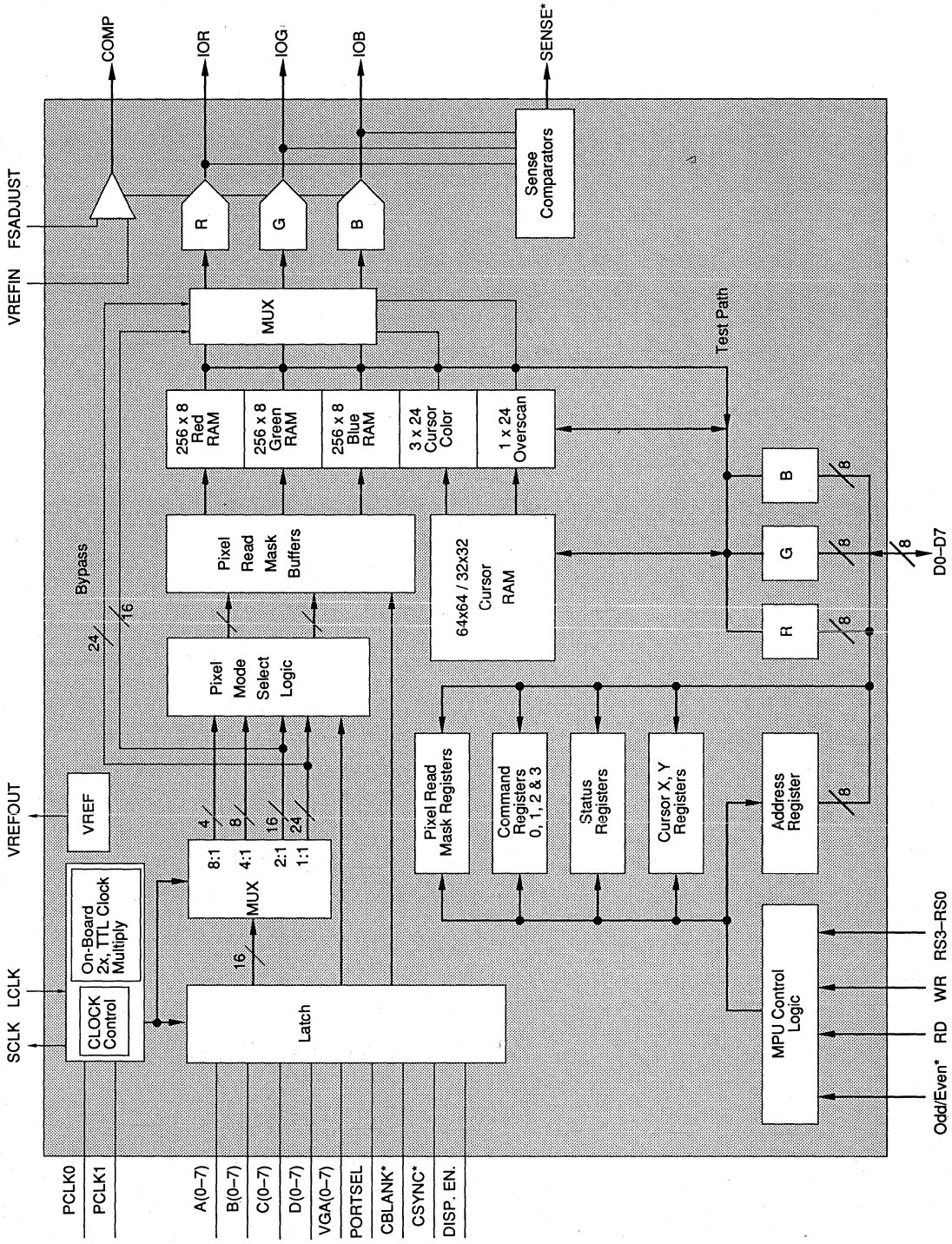


Bt485 Detailed Block Diagram.

Circuit Description

MPU Interface

As illustrated in the functional block diagram, a standard MPU bus interface is supported, giving the MPU direct access to the color palette RAM. MPU data is transferred into and out of the RAMDAC with the D0–D7 data pins. The read/write timing is controlled by the RD* and WR* inputs.

The RS0–RS3 select inputs specify which control register the MPU is accessing, as shown in Tables 1 and 2. The 8-bit address register is used to address the color palette RAM, eliminating the requirement for external address multiplexers. D0 corresponds to ADDR0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU writes the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS3 to select the color palette RAM. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous RGB write cycles until the entire block has been written. The Timing Waveforms section contains further information.

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers, and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS3 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers, and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Writing Cursor and Overscan Color Data

To write cursor color data, the MPU writes the address register (cursor color write mode) with the address of the cursor color location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS3 to select the cursor color registers. After the blue write cycle, the 3 bytes of red, green, and blue color information are concatenated into a 24-bit word and written to the cursor color location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous RGB write cycles until the entire block has been written.

RS3–RS0	Access	Addressed by MPU
0000	R/W	address register; palette/cursor RAM write
0001	R/W	6/8-bit color palette data
0010	R/W	pixel mask register
0011	R/W	address register; palette/cursor RAM read
0100	R/W	address register; cursor/overscan color write
0101	R/W	cursor overscan and color data
0110	R/W	command register 0
0111	R/W	address register; cursor/overscan color read
1000	R/W	command register 1
1001	R/W	command register 2
1010	read only	status register
1011	R/W	cursor RAM array data
1100	R/W	cursor x-low register
1101	R/W	cursor x-high register
1110	R/W	cursor y-low register
1111	R/W	cursor y-high register

Table 1. Control Input Truth Table (RS3 = MSB and RS0 = LSB).

Circuit Description *(continued)*

CR31 (A9)	ADDR 0–7 (counts binary)	ADDRa,b (counts modulo 3)	RS3	RS2	RS1	RS0	Addressed by MPU
N/A	$00–$FF	00	0	0	0	1	color palette RAM (red component)
		01	0	0	0	1	color palette RAM (green component)
		10	0	0	0	1	color palette RAM (blue component)
N/A	xxxx xx00	00	0	1	0	1	overscan color (red component)
		01	0	1	0	1	overscan color (green component)
		10	0	1	0	1	overscan color (blue component)
N/A	xxxx xx01	00	0	1	0	1	cursor color 1 red component
		01	0	1	0	1	cursor color 1 green component
		10	0	1	0	1	cursor color 1 blue component
N/A	xxxx xx10	00	0	1	0	1	cursor color 2 red component
		01	0	1	0	1	cursor color 2 green component
		10	0	1	0	1	cursor color 2 blue component
N/A	xxxx xx11	00	0	1	0	1	cursor color 3 red component
		01	0	1	0	1	cursor color 3 green component
		10	0	1	0	1	cursor color 3 blue component
N/A	$00–$7F	N/A	1	0	1	1	cursor RAM array, plane 0 (32 x 32 x 2 cursor only)
N/A	$80–$FF	N/A	1	0	1	1	cursor RAM array, plane 1 (32 x 32 x 2 cursor only)
0	$000–$1FF	N/A					cursor RAM array, plane 0 (64 x 64 x 2 cursor only)
1	$200–$3FF	N/A					cursor RAM array, plane 1 (64 x 64 x 2 cursor only)

When the cursor color register or overscan register is addressed, the 6 MSBs of the address register are don't-care conditions. Therefore, when the address register is read and the previous access was to the cursor color registers or overscan register, address register bits [7–2] are returned as either ones or zeros.

Table 2. Address Register Operation and Auto-Incrementing.

Reading Cursor Color Data

To read cursor color data, the MPU loads the address register (cursor color read mode) with the address of the cursor color location to be read. The contents of the cursor color register at the specified address are copied into the RGB registers, and the address register is incremented to the next cursor color location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS3 to select the cursor color registers. Following the blue read cycle, the contents of the cursor color location at the address specified by the address register are copied into the RGB registers, and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous RGB read cycles until the entire block has been read.

Additional Information

When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF.

The MPU interface operates asynchronously to the pixel clock. Data transfers that occur between the color palette RAM and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and take place in the period between MPU accesses. To reduce noticeable sparkling on the CRT screen during MPU access to the color palette RAMs, internal logic maintains the previous output color data on the analog outputs while the transfer between RGB registers and lookup table RAMs occurs.

To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits(ADDRa and ADDRb) that count modulo three. They are reset to

zero when the MPU writes to the address register and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Accessing the Cursor RAM Array

The 32 x 32 x 2 cursor RAM is accessed in a planar format. In the planar format only 7 address bits are used. The eighth bit determines which plane (0 or 1) data of the cursor RAM array is accessed. A single address presented to the cursor RAM accesses eight bit locations in plane 0 or 1, depending on the state of address bit 7.

After each access in the planar format, the address increments. The MPU uses ADDR, a binary address counter, to access the cursor RAM array (see Table 2). ADDR is the same binary counter used for RGB auto-incrementing. Any write to ADDR after cursor auto-incrementing has been initiated resets the cursor auto-incrementing logic until cursor RAM array has again been accessed. Cursor auto-incrementing will then begin from the address written. A read from the ADDR does not reset the cursor, auto-incrementing logic. The color palette RAM and the cursor RAM share the same external address register, and MPU addressing for this and all other registers is determined by the external register select lines RS3–RS0 (see Table 1).

The 64 x 64 x 2 cursor RAM is accessed in a planar format. The larger cursor RAM can be accessed after bit CR32 in Command Register 3 has been set to a logical one. Bits CR30 and CR31 in Command Register 3 become the load inputs to the 2 MSBs of a 10-bit address counter; therefore, these bits must be written in Command Register 3 before the lower 8 bits are written to the address counter through the MPU port. In the planar format, only 9 address bits are used. The tenth bit is to determine which plane (0 or 1) data of the cursor RAM array is accessed. A single address presented to the cursor RAM accesses eight bit locations in plane 0 or 1, depending on the state of address bit 9.

After each access in the planar format, the address increments. The MPU uses ADDR, a 10-bit binary address counter, to access the cursor RAM array. The address counter is the same 8-bit binary counter used for RGB auto-incrementing with CR30 and CR31 as its extended MSBs. Any write to the address counter after cursor auto-incrementing has been initiated resets the cursor auto-incrementing logic until cursor RAM array has again been accessed. Cursor auto-incrementing will then begin from the address written. A read from the address counter does not reset the cursor, auto-incrementing logic. The color palette RAM and the cursor RAM share the same external address register, and MPU addressing for this and all other registers is determined by the external register select lines RS3–RS0 (see Table 1).

6-Bit / 8-Bit Operation

The command bit CR01 is used to specify whether the MPU is reading and writing 8 bits or 6 bits of color information each cycle.

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation, color data is contained on the lower 6 bits of the data bus, with D0 the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 are logical zeros.

Accessing the cursor RAM array does not depend on the resolution of the DACs.

In the 6-bit mode, the Bt485's full-scale output current will be about 1.5-percent lower than when in the 8-bit mode. This is because the 2 LSBs of each 8-bit DAC are logical zeros in the 6-bit mode.

Power-Down Mode

The Bt485 incorporates a power-down capability, controlled by command bit CR00. While command bit CR00 is a logical zero, the Bt485 functions normally.

While command bit CR00 is a logical one, the DACs and power to the RAM are turned off. The RAM still retains the data. Also, the MPU may read or write to the RAM while the pixel clock is running. The RAM automatically powers up during MPU read/write cycles and shuts down when the MPU access is completed. The DACs output no current, and the three command registers may still be written to or read by the MPU. The output DACs require about 1 second to turn off (sleep mode) or turn on (normal), depending on the compensation capacitor used (see Video Generation for further information).

When an external voltage reference is used, external circuitry should turn off the voltage reference (VREF = 0 V) to further reduce power consumption caused by biasing of portions of the internal voltage reference.

Frame Buffer Clocking

The video DRAM shift clock (SCLK) is generated by the Bt485. SCLK is one eigth, one fourth, or one half the pixel clock rate, depending on whether multiplexing is 8:1, 4:1, or 2:1, respectively. In the 1:1/VGA mode, SCLK = LCLK.

P0–P7 (A–D) are pixel data, 8 bits per pixel (4:1 MUX) and 4 bits per pixel (8:1 MUX) for 4 and 8 horizontally consecutive output pixels. P0–P7 (A–D) are always latched on the rising edge of LCLK.

The pixel clock is specified to be either PCLK 0 or PCLK 1 by command bit CR24.

Onboard 2x TTL Clock Multiplier

The Bt485 provides an onboard 2x TTL clock multiplier for high-speed operations. The clock multiplier can be

enabled or disabled by programming bit CR33 in Command Register 3 (see Accessing Command Register 3 in the Internal Registers section). Upon applying a RESET signal, the clock multiplier is disabled until bit CR33 is written to a logical one. Either PCLOCK0 or PCLOCK1 can be doubled internally. For operations above 90 MHz, the clock doubler is recommended.

The clock multiplier can lower system costs by eliminating expensive ECL crystals and clock synthesizers. It can also improve system design by eliminating conversion logic.

Frame Buffer Pixel Port Interface

There are four 8-bit pixel ports, (A–D), used to interface to the frame buffer memory.

Video input data ports A through D are designated in this manner to represent the order of pixel data presentation: Port A always corresponds to the first pixel of the first line of the display. This is the first pixel fed to the analog outputs, followed by B, then C, and finally D, repeating the pattern ABCD, ABCD, until the first scan line is completely displayed.

For the cursor display, the output sequence depends on the CR23 command bit and the ODD/EVEN* input. For example, when either interlaced or noninterlaced operation is selected, the current field is displayed.

Scan line 1 is always displayed first in the interlaced mode and is considered the first line of the EVEN field. In the noninterlaced mode, scan line 2 immediately follows scan line 1. In the interlaced mode, scan line 2 is considered to be the first line of the ODD field and is displayed only after the entire EVEN field has been displayed and the ODD/EVEN pin has been toggled.

Only the ODD lines or only the EVEN lines will be displayed, if the ODD/EVEN does not change.

Figure 1 shows the interlaced and noninterlaced display scan. Noninterlaced display scan is equal to one frame. Interlaced display scan is equal to one frame with odd and even fields.

Pixel Read Mask Register

Each pixel clock cycle, P0–P7 pixel data is bit-wise logically ANDed with the contents of the pixel read mask register. The result is used to address the color palette RAM. The addressed location provides 24 bits of color information to the three D/A converters. Pixel masking is enabled for all modes of operation, except when the true color bypass is enabled. The pixel mask register is not initialized at the power-up/reset and should be initialized by the user to logical ones for proper operation.

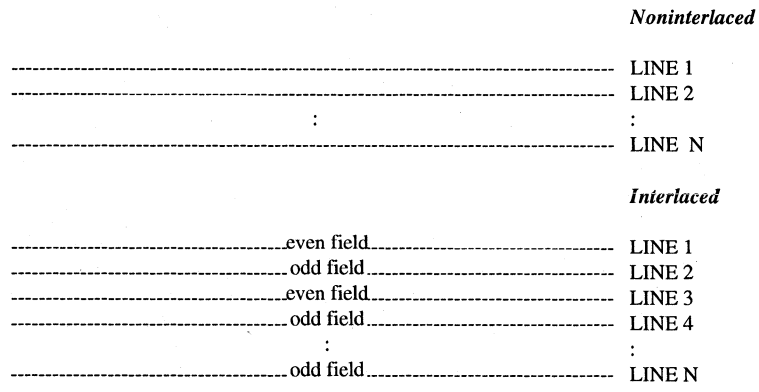


Figure 1. Interlaced/Noninterlaced Display Operation.

Circuit Description *(continued)*

Modes of Operation

4-Bits/Pixel Operation (8:1 MUX)

The 32 input bits are multiplexed 8:1 and are configured for 4 bits/pixel. There are eight independent 4-bit pixel ports, P7:4 (A–D) and P3:0 (A–D). The pixel bits are latched on the rising edge of LCLK. One rising edge of LCLK should occur every eight PCLK cycles. SCLK will equal the PCLK selected, divided by 8. The 4 bits from each port will select 1 of 16 locations (RAM address 0–15) in the palette in the order presented in Table 3.

8-Bits/Pixel Operation (4:1 MUX)

The 32 input bits are multiplexed 4:1 and are configured for 8 bits/pixel. There are four independent 8-bit pixel ports, (A–D). The pixel bits are latched on the rising edge of LCLK. One rising edge of LCLK should occur every four PCLK cycles. SCLK will be equal to the PCLK selected, divided by 4. The 8 bits from each port will select 1 of 256 locations in the palette as presented in Table 3.

16-Bits/Pixel Operation (2:1 MUX)

The 32 input bits are multiplexed 2:1 and are configured for 16 bits/pixel. Multiplexing of 2:1 is selected through bit CR12 in Command Register 1. There are two independent 16-bit pixel ports, (B–A) and (D–C). The bits are latched on the rising edge of LCLK. One rising edge of LCLK should occur every two PCLK cycles. SCLK will be equal to the PCLK selected, divided by 2. The pixel bits multiplexed in this mode are from the same ports of RGB color formats of 5:5:5 or 5:6:5. P7D and P7B are ignored internally when the 5:5:5 color format is selected (see Table 3).

Bit CR14 can be programmed in Command Register 1, which enables or disables true-color palette bypass. When the bypass mode is selected, the pixel data bypasses the palette as well as the pixel mask and is transferred to the proper MSBs of the respective DACs. When the bypass mode is not selected, the pixel data indexes the proper locations in the palette, and the correct color information is passed on to the respective DACs.

Bit CR22 in Command Register 2 determines whether palette addressing is sparse or contiguous. For sparse palette addressing, each color component of pixel data is mapped to the most significant bits of the respective palette address; the least significant bits are set to zero. For contiguous palette addressing, each color component of the pixel data is mapped to the least significant bits of the respective palette address; the most significant bits are set to zero. The color palette values indexed, for either sparse or contiguous addressing, are transferred to the DACs.

When 5:5:5 or 5:6:5 color format is selected, the display can contain 32 K or 64 K simultaneous colors. The DACs can be configured for 6 or 8 bits of resolution in this mode.

16-Bits/Pixel Operation (1:1 MUX)

The 1:1 multiplexing mode is selected through CR12 in Command Register 1. When this mode is selected, two independent 16-bit pixel ports, (B–A) and (D–C), are latched on the rising edge of LCLK and are multiplexed 1:1. Selection between the two ports is made by bit CR10 in Command Register 1. One rising edge of LCLK should occur every PCLK cycle. SCLK is equal to the PCLK selected.

Bit P7D switches between the two ports on a pixel-by-pixel basis when 5:5:5 RGB color format (bit CR13 in Command Register 1) and real-time pixel port switching is enabled (bit CR11 in Command Register 1). If PORTSEL is a logical zero, the VGA port is multiplexed regardless of the state of P7D. Bit P7B is ignored internally when in 5:5:5 mode. Real-time pixel port switching is not supported for 5:6:5 RGB color format.

Bits P7B and P7D are ignored internally if 5:5:5 RGB color format is selected and real-time pixel port switching is disabled. Programming bit CR10 in Command Register 1 determines switching for both 5:5:5 and 5:6:5 RGB color formats.

Bit CR14 can be programmed in Command Register 1, which enables or disables true-color palette bypass. When the bypass mode is selected, the pixel data bypasses the palette as well as the pixel mask and is transferred to the proper MSBs of the respective DACs. When the bypass mode is not selected, the pixel data indexes the proper locations in the palette, and the correct color information is passed on to the respective DACs.

Bit CR22 in Command Register 2 determines whether palette addressing is sparse or contiguous. For sparse palette addressing, each color component of pixel data is mapped to the most significant bits of the respective palette address; the least significant bits are set to zero. For contiguous palette addressing, each color component of the pixel data is mapped to the least significant bits of the respective palette address; the most significant bits are set to zero. The color palette values indexed, for either sparse or contiguous addressing, are transferred to the DACs.

When 5:5:5 or 5:6:5 color format is selected, the display can contain 32 K or 64 K simultaneous colors. The DACs can be configured for 6 or 8 bits of resolution in this mode.

24-Bits/Pixel Operation (1:1 MUX)

When 24 bits/pixel is selected, there is one 24-bit pixel port. The pixel bits, P7:0 (C–A), are latched on the rising edge of LCLK and are multiplexed 1:1. One rising edge of LCLK should occur every PCLK cycle. SCLK is equal to the PCLK selected. The RGB color format in this mode is 8:8:8.

Bit CR14 can be programmed in Command Register 1, which enables or disables true-color palette bypass. When the bypass mode is selected, the pixel data bypasses the palette as

Circuit Description *(continued)*

PORTSEL	CR11	CR10	P7D	CR12	CR13	CR16	CR15	Ports MUXed	MUX Rate	Operating Modes
0	x	x	x	x	x	x	x	VGA(7:0)	1:1	VGA
1	x	x	Data	x	x	1	1	P7:4(A) P3:0(A) P7:4(B) P3:0(B) P7:4(C) P3:0(C) P7:4(D) P3:0(D)	8:1	4 Bits/Pixel
1	x	x	Data	x	x	1	0	P7:0(A) P7:0(B) P7:0(C) P7:0(D)	4:1	8 Bits/Pixel
1	x	x	x	0	0	0	1	P7:0(B-A) P7:0(D-C)	2:1	16 Bits/Pixel (5:5:5) (see Table 4)
1	x	x	Data	0	1	0	1	P7:0(B-A) P7:0(D-C)	2:1	16 Bits/Pixel (5:6:5) (see Table 5)
1	0	0	x	1	0	0	1	P7:0(B-A)	1:1	16 Bits/Pixel (5:5:5)
1	0	1	x	1	0	0	1	P7:0(D-C)	1:1	16 Bits/Pixel (5:5:5)
1	1	x	0	1	0	0	1	P7:0(B-A)	1:1	16 Bits/Pixel (5:5:5) (see Table 4)
1	1	x	1	1	0	0	1	P7:0(D-C)	1:1	16 Bits/Pixel (5:5:5) (see Table 4)
1	x	0	x	1	1	0	1	P7:0(B-A)	1:1	16 Bits/Pixel (5:6:5) (see Table 5)
1	x	1	Data	1	1	0	1	P7:0(D-C)	1:1	16 Bits/Pixel (5:6:5) (see Table 5)
1	x	x	x	x	x	0	0	P7:0(C-A)	1:1	24 Bits/Pixel (see Table 6)

Table 3. Modes of Operation (Pixel Port Configuration).

Circuit Description *(continued)*

Bit	MSB															LSB
Format	S	R	R	R	R	R	G	G	G	G	G	B	B	B	B	B
Port 1	S	P6B	P5B	P4B	P3B	P2B	P1B	P0B	P7A	P6A	P5A	P4A	P3A	P2A	P1A	P0A
Port 2	S	P6D	P5D	P4D	P3D	P2D	P1D	P0D	P7C	P6C	P5C	P4C	P3C	P2C	P1C	P0C

If bit CR11 in Command Register 1 is a logical zero, then S=CR10 bit, 16-bit/pixel port switch control (1:1 multiplexing, CR12 = 1). If bit CR11 in Command Register 1 is a logical one, then S=P7D bit, real-time pixel port switch (1:1 multiplexing, CR12 = 1).

Table 4. 5:5:5 RGB Color Format for Both 2:1 and 1:1 Multiplexing Modes.

Bit	MSB															LSB
Format	R	R	R	R	R	G	G	G	G	G	G	B	B	B	B	B
Port 1	P7B	P6B	P5B	P4B	P3B	P2B	P1B	P0B	P7A	P6A	P5A	P4A	P3A	P2A	P1A	P0A
Port 2	P7D	P6D	P5D	P4D	P3D	P2D	P1D	P0D	P7C	P6C	P5C	P4C	P3C	P2C	P1C	P0C

Table 5. 5:6:5 RGB Color Format for Both 2:1 and 1:1 Multiplexing Modes.

Bit	MSB																						LSB
Format	R	R	R	R	R	R	R	R	G	G	G	G	G	G	G	G	B	B	B	B	B	B	B	B
Port	P7C	P6C	P5C	P4C	P3C	P2C	P1C	P0C	P7B	P6B	P5B	P4B	P3B	P2B	P1B	P0B	P7A	P6A	P5A	P4A	P3A	P2A	P1A	P0A

Note: P7:0(D) are ignored.

Table 6. 24-Bits/Pixel RGB Color Format.

well as the pixel mask and is transferred to the proper MSBs of the respective DACs. When the bypass mode is not selected, the pixel data indexes the proper locations in the palette, and the independent RGB color values are passed on to the respective DACs. When 8:8:8 color format is selected, the display can contain 16.8 million simultaneous colors. The DACs should be configured for 8 bits of resolution in this mode (CR14=1 and CR01=1).

VGA Port

An 8-bit pixel port is provided to support VGA pixel data. The data is latched on the rising edge of LCLK. One rising edge of LCLK should occur every PCLK cycle. SCLK will equal the PCLK selected. A logical zero on the PORTSEL pin ensures that the VGA port is selected. A logical one on the PORTSEL pin selects the pixel port. To use the VGA PORTSEL feature the RAMDAC *must* be configured in the 1:1 multiplexing mode through the RAM (CR14 = 0) or pallette bypass (CR14 = 1). After the RAMDAC has been properly configured, the VGA PORTSEL can then be used to select between the pixel port and the VGA port on a pixel-by-pixel basis. The PORTSEL pin can also be used to switch between VGA and the pixel ports in 2:1, 4:1, or 8:1 MUX modes on a frame-by-frame basis. The VGA pixels address the color palette when selected. Only PCLK0 should be used when switching between the VGA and pixel ports on a pixel-by-pixel basis. PCKL1 should be used when switching between the VGA and pixel ports on a frame-by-frame basis. The 8-bit VGA data forms a common index into the palette, selecting 1 of 256 colors. Valid data begins at address zero.

Pixel Read Mask Register

The pixel data has can be masked with the 8-bit pixel read mask register before being transferred to the color palette. The pixel data is bit-wise logically ANDed with the

	MSB							LSB	
Pixel Mask Register	7	6	5	4	3	2	1	0	Register Bits
VGA Data	7	6	5	4	3	2	1	0	Palette Index
4 Bits/Pixel	x	x	x	x	3	2	1	0	Palette Index
8 Bits/Pixel	7	6	5	4	3	2	1	0	Palette Index
16 Bits/Pixel	7	6	5	4	3	x	x	x	Red Palette Index
5:5:5 Format	7	6	5	4	3	x	x	x	Green Palette Index
SPARSE	7	6	5	4	3	x	x	x	Blue Palette Index
16 Bits/Pixel	x	x	x	4	3	2	1	0	Red Palette Index
5:5:5 Format	x	x	x	4	3	2	1	0	Green Palette Index
CONTIGUOUS	x	x	x	4	3	2	1	0	Blue Palette Index
16 Bits/Pixel	7	6	5	4	3	x	x	x	Red Palette Index
5:6:5 Format	7	6	5	4	3	2	x	x	Green Palette Index
SPARSE	7	6	5	4	3	x	x	x	Blue Palette Index
16 Bits/Pixel	x	x	x	4	3	2	1	0	Red Palette Index
5:6:5 Format	x	x	5	4	3	2	1	0	Green Palette Index
CONTIGUOUS	x	x	x	4	3	2	1	0	Blue Palette Index
24 Bits/Pixel	7	6	5	4	3	2	1	0	Red Palette Index
8:8:8 Format	7	6	5	4	3	2	1	0	Green Palette Index
	7	6	5	4	3	2	1	0	Blue Palette Index

Table 7. Pixel Index Masking.

contents of the pixel read mask register. The result is used to address the color palette RAM. The addressed location provides 24 bits of color information to the three D/A converters. Pixel masking is enabled for all modes of operation, except when the true-color bypass is enabled. The pixel read mask register is not initialized at the power-up/reset and must be initialized by the user to logical ones for proper operation (see Table 7).

Cursor Operation

The Bt485 has an on-chip, three-color, 64 x 64 x 2 pixel user-definable cursor. A 32 x 32 x 2 pixel user-defineable cursor can also be selected by writing bit CR32 in Command Register 3. This cursor can be used with both interlaced and noninterlaced systems.

The pattern for the cursor is provided by the cursor RAM, which may be accessed by the MPU at any time. The cursor is positioned through the cursor position register (Xp,Yp) (see Figure 2). A (0,0) written to the cursor position registers will place the cursor off the screen. A (1,1) written to the cursor position registers will place the lower right pixel of the cursor on the upper left corner of the screen. Only one cursor pattern per frame is displayed at the location specified for both interlaced and noninterlaced display formats, regardless of the number of updates to (Xp,Yp). The cursor's vertical or horizontal location is not affected during any frame displayed. There are no restrictions on updating (Xp, Yp) other than both cursor position registers must be written when the cursor location is updated. Internal x-and y-position registers are loaded after the upper byte of Yp has been written to ensure one cursor pattern per frame at the correct location. The cursor pattern is displayed at the last cursor location written.

Cursor positioning is relative to CDE. The cursor position is not dependent upon CBLANK* (see Figure 2). The reference point of the cursor (row 0, column 0) is in the lower right corner. The cursor Xp position is relative to the first rising edge of LCLK when CDE is sampled at logical one. The cursor Yp position is relative to the first rising edge of LCLK when CDE is sampled at logical one after the CDE vertical blanking interval has been determined (see Figure 2). If a CDE transition from logical zero to logical one (as determined by LCLK) does not occur within 2048 PCLKs (2048 LCLKs when in 1:1 MUX mode), CDE is in vertical blanking. In 8:1, 4:1, or 2:1 MUX modes, cursor timing is based on the PCLK selected. When the MUX rate is 1:1, cursor timing is based on LCLK.

The 64 x 64 x 2 cursor pattern can be displayed in an interlaced system if bit CR23 in Command Register 2 is a logical one. If Yp is greater than 64 ($0040), and less than or equal to 4095 ($0FFF), the first cursor line displayed depends on the state of the ODD/EVEN* pin and the value of Yp. If Yp is an even number, the data in row 0 of the cursor RAM array will be displayed during the even field,

Circuit Description *(continued)*

and the data in row 63 of the cursor RAM will be displayed during the odd field, starting at the position specified by (Xp,Yp). Each subsequent scan line displayed in the even field will correspond to every alternate active cursor line after row 0 in the cursor RAM array. During the odd fields, row 1 of the cursor RAM array is displayed on the first odd scan line at the position specified by (Xp, Yp). Each subsequent scan line displayed in the odd field will correspond to every alternate active cursor line after row 1 in the cursor RAM array.

If Yp is an odd number, then the data in row 0 of the cursor RAM array will be displayed during the odd field, and the data in row 63 of the cursor RAM will be displayed during the even field, starting at the position specified by (Xp,Yp). Each subsequent scan line displayed in the odd field will correspond to every alternate active cursor line after row 0 in the cursor RAM array. During even fields, row 1 of the cursor RAM array is displayed on the first even scan line at the position specified by (Xp, Yp). Each subsequent scan line displayed in the even field will correspond to every alternate active cursor line after row 1 in the cursor RAM array.

If Yp is less than 64 ($0040), cursor display does not depend on whether Yp is odd or even. If the ODD/EVEN* pin is a logical zero, the first line of the cursor is displayed on scan line 1. Every alternate active cursor line in the cursor RAM array relative to the first active cursor line in the even field will correspond to subsequent scan lines in the even field. If the ODD/EVEN* pin is a logical one, the second active cursor line in the cursor RAM array is displayed on scan line 2. Each subsequent scan line displayed in the odd field corresponds to alternate cursor lines in the cursor RAM array relative to the first active cursor line in the odd field.

The cursor pattern can be displayed in an interlaced system if bit CR23 in Command Register 2 is a logical one. If Yp is greater than 32 ($0020), and less than or equal to 4095 ($0FFF), the first cursor line displayed depends on the state of the ODD/EVEN* pin and the value of Yp. If Yp is an even number, the data in row 0 of the cursor RAM array will be displayed during the even field, and the data in row 31 of the cursor RAM array will be displayed during the odd field, starting at the position specified by (Xp,Yp). Each subsequent scan line displayed in the even field will correspond to every alternate active cursor line after row 0 in the cursor RAM array. During the odd fields, row 1 of the cursor RAM array is displayed on the first odd scan line at the position specified by (Xp, Yp). Each subsequent scan line displayed in the odd field will correspond to every alternate active cursor line after row 1 in the cursor RAM array.

If Yp is an odd number, then the data in row 0 of the cursor RAM array will be displayed during the odd field, and the data in row 31 of the cursor RAM array will be displayed during the even field, starting at the position specified by (Xp,Yp). Each subsequent scan line displayed in the odd field will correspond to every alternate active cursor line after row 0 in the cursor RAM array. During even fields, row 1 of the cursor RAM array is displayed on the first even scan line at the position specified by (Xp, Yp). Each subsequent scan line displayed in the even field will correspond to every alternate active cursor line after row 1 in the cursor RAM array.

If Yp is less than 32 ($0020), cursor display does not depend on whether Yp is odd or even. If the ODD/EVEN* pin is a logical zero, the first line of the cursor is displayed on scan line 1. Every alternate active cursor line in the cursor RAM array relative to the first active cursor line in the even field will correspond to subsequent scan lines in the even field. If the ODD/EVEN* pin is a logical one, the second active cursor line in the cursor RAM array is displayed on scan line 2. Each subsequent scan line displayed in the odd field corresponds to alternate cursor lines in the cursor RAM array relative to the first active cursor line in the odd field.

If bit CR23 is a logical zero, the cursor must be

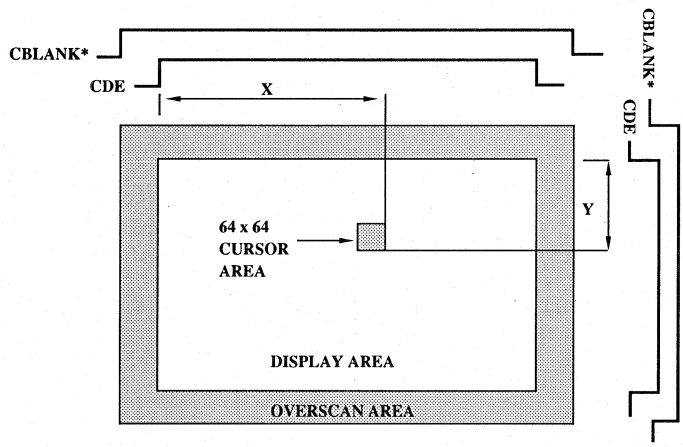


Figure 2. Cursor Positioning.

displayed in a noninterlaced system. Scan lines displayed in a frame correspond to sequential cursor lines in the cursor RAM relative to the first active cursor line in the frame.

Figure 3 is a visual explanation of planar pixel format and cursor RAM array pixel mapping.

Cursor Color Support

The cursor has three modes for color selection. Bits CR21 and CR20 in Command Register 2 determine which cursor mode is to be used. Mode 1 is a three-color cursor, mode 2 is referred to as a PM/Window cursor, and mode 3 is referred to as an X-Windows cursor (see Table 8).

Highlight Logic

The highlight logic is enabled in cursor mode 2 when both plane data (plane 1 and plane 0) are logical ones (see Table 8). When the highlight logic is enabled, it ensures that the pixel highlighted has a unique color. This is because the highlight logic bit-wise complements the 24- or 18-bit palette or bypass data supplied to the DACs.

Video Generation

The CSYNC* and CBLANK* inputs are latched on the rising edge of LCLK to maintain synchronization with the color data. They add appropriately weighted currents to the analog outputs and produce the specific output levels required for video applications, as illustrated in Figures 4 and 5. Tables 9 and 10 detail how the CSYNC* and BLANK* inputs modify the output levels.

The CR05 command bit is used to specify whether a 0 or 7.5 IRE blanking pedestal is to be used. Command bits CR02, CR03, and CR04 specify whether the RGB outputs contain sync information.

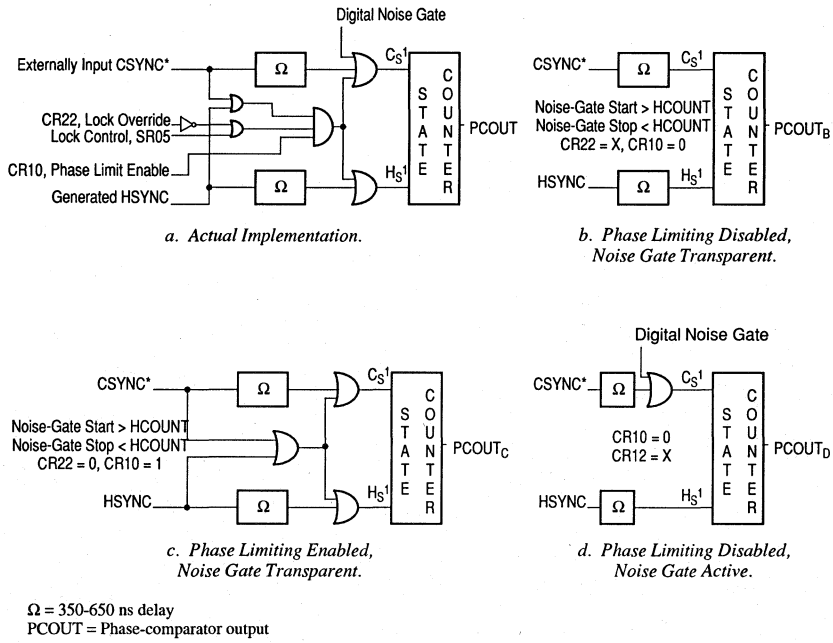
SENSE* Output

SENSE* is a logical zero if one or more of the IOR, IOG, or IOB outputs have exceeded the internal voltage reference level of the SENSE* comparator circuit. This output is used to determine the presence of a CRT monitor, and, with diagnostic code, the difference between a loaded or an unloaded RGB line can be discerned. The reference is generated by a voltage divider from the external 1.235 V voltage reference on the VREF pin. For the proper operation of the SENSE circuit, the following levels should be applied to the comparator by the IOR, IOG, and IOG outputs:

DAC Low Voltage ≤ 260 mV (Note 1)
DAC High Voltage ≥ 410 mV (Note 1)

Note 1: SENSE values are subject to change upon completion of characterization.

There is an additional ±10-percent tolerance on the above levels when the internal voltage reference is used. If SYNC* is logical zero, SENSE* is stable. The SENSE* output can drive only one CMOS load.



a. Actual Implementation.

b. Phase Limiting Disabled, Noise Gate Transparent.

c. Phase Limiting Enabled, Noise Gate Transparent.

d. Phase Limiting Disabled, Noise Gate Active.

Ω = 350-650 ns delay
PCOUT = Phase-comparator output

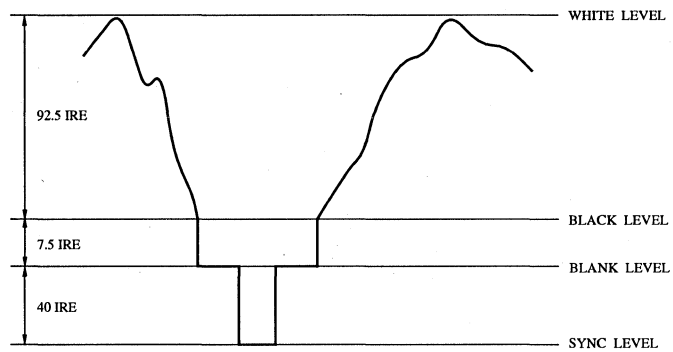
Figure 3. Planar Pixel Format and Cursor RAM Array Pixel Mapping for Both 32 x 32 and 64 x 64 Cursors.

Plane 1	Plane 0	MODE 1	MODE 2	MODE 3
0	0	Palette Data	Cursor Color 1	Palette Data
0	1	Cursor Color 1	Cursor Color 2	Palette Data
1	0	Cursor Color 2	Palette Data	Cursor Color 1
1	1	Cursor Color 3	Palette Data Complement	Cursor Color 2

Table 8. Overlay Color Modes.

Circuit Description *(continued)*

NO SYNC		SYNC	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load, VREF = 1.235 V, and RESET ~ 147 Ω. RS-343A levels and tolerances are assumed on all levels.

Figure 4. Composite Video Output Waveforms (SETUP = 7.5 IRE).

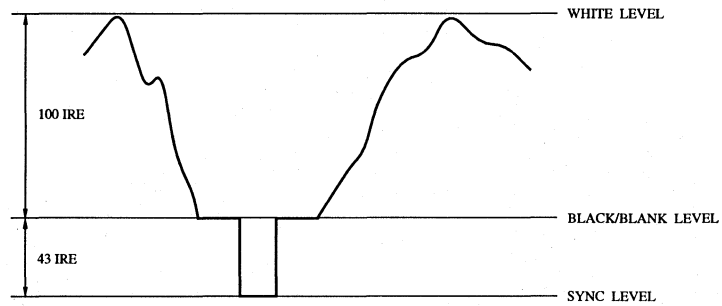
Description	Sync Disabled	Sync Enabled	CSYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	19.05	26.67	1	1	$FF
DATA	data + 1.44	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	1.44	9.05	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly-terminated load, VREF = 1.235 V, and RESET ~ 147 Ω.

Table 9. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description *(continued)*

NO SYNC		SYNC	
MA	V	MA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000



Note: 75 Ω doubly-terminated load, VREF = 1.235 V, and RESET ~ 147 Ω. RS-343A levels and tolerances are assumed on all levels.

Figure 5. Composite Video Output Waveforms (SETUP = 0 IRE).

Description	Sync Disabled	Sync Enabled	CSYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	17.62	25.24	1	1	$FF
DATA	data	data + 7.62	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	7.62	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly-terminated load, VREF = 1.235 V, and RESET~ 147 Ω.

Table 10. Video Output Truth Table (SETUP = 0 IRE).

Command Register 0 (RS value = 0110)

This register may be written to or read by the MPU at any time and is not initialized at power-up. CR00 corresponds to data bus bit D0, the least significant data bit. All command register bits are set to logical zeros when a low signal is asserted on the RESET* pin.

CR07	(0) Command Register 3 Cannot be Addressed (1) Command Register 3 Can be Addressed	A logical one written to this bit allows the user to indirectly access Command Register 3.
CR06	Clock Disable ANDed with CR00 (0) Normal Operation (1) Disable Internal Clocking	When this bit *and* CR00 are a logical one, the internal clock and SCLK are disabled to further conserve power when in power-down mode. The RAM still retains the data, and MPU reads and writes can occur without loss of data. When this bit is a logical zero, internal clocking is enabled and SCLK will be generated.
CR05	Setup Enable (0) Disable SETUP (0 IRE) (1) Enable SETUP (7.5 IRE)	This bit determines the video blanking pedestal. A logical zero sets a 0 IRE blanking pedestal, and a logical one sets 7.5 IRE.
CR04 CR03 CR02	Blue Sync Enable Green Sync Enable Red Sync Enable (0) Disable Sync (1) Enable Sync	These bits specify whether the respective IOB, IOG, or IOR outputs are to contain sync information.
CR01	DAC 6/8-Bit Resolution (0) 6-bit Operation (1) 8-bit Operation	This bit specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle.
CR00	Power-Down Enable (0) Normal Operation (1) Power-Down Operation	While this bit is a logical zero, the device operates normally. If this bit is a logical one, the DACs and power to the RAM are turned off. The RAM still retains the data, and CPU reads and writes can occur with no loss of data. The DACs will be turned off during sleep mode only if a voltage reference (internal or external) is used.

Internal Registers *(continued)*

Command Register 1 (RS value = 1000)

This register may be written to or read by the MPU at any time and is not initialized at power-up. CR10 corresponds to data bus bit D0, the least significant data bit (see Table 7). All command register bits are set to logical zero when a low signal is asserted on the RESET* pin.

CR17	Reserved (logical zero)	This bit is reserved for future expansion. A logical zero must be written to ensure proper operation.
CR16, 15	Bit/Pixel Select (00) One 24-Bit Pixel (01) One or Two 16-Bit Pixels (10) Four 8-Bit Pixels (11) Eight 4-Bit Pixels	These bits select the pixel size depth and determine the multiplexing rates for 4-, 8-, and 24-bit/pixel operation. The 16-bit/pixel multiplexing rate is set by the state of CR12.
CR14	True-Color Bypass Enable (0) Pixel Addresses Palette (1) Pixel Bypasses Palette	When this bit is a logical zero, the pixel palette is addressed by the pixel data. When this bit is a logical one, the RGB pixel data bypasses the color palette and drive the DACs directly. True-color bypassing is available only for pixel sizes of 16 and 24 bits.
CR13	16-Bit RGB Color Format (0) 5:5:5 R:G:B Color Format (1) 5:6:5 R:G:B Color Format	This bit selects the RGB color format for 16-bit/pixel operation.
CR12	16-Bit Multiplexing Rate (0) 2:1 Multiplexing (1) 1:1 Multiplexing	When this bit is a logical zero and CR16 and 15 are set to 01, two 16-bit values are latched in during every LCLK cycle. When this bit is a logical one and CR16 and 15 are set to 01, one 16-bit value is output during every LCLK cycle. This bit is ignored if CR16/CR15 specify 4-, 8-, or 24-bit/pixel operation.
CR11	16-Bit Real-Time Switch Enable (0) CR10 Controls Selection (1) P7D Controls Selection	This bit is only valid when CR13 = 0 (5:5:5 format) and CR12 = 1 (1:1 multiplexing) are specified. When this bit is a logical zero, CR10 switches the ports multiplexed. When this bit is a logical one, pixel port bit P7D switches the ports multiplexed. This bit is ignored when 5:6:5 RGB color format is selected (when bit CR13 is a logical one).
CR10	16-Bit/Pixel Port Switch Control (0) Multiplex Port [B–A] (1) Multiplex Port [D–C]	This bit specifies which 16-bit word is selected for either 5:5:5 (CR13 = 0) or 5:6:5 (CR13 = 1) modes. In order for this bit to control which 16-bit port is selected, CR12 must be a logical one (16-bit 1:1 multiplexing). This bit is ignored when real-time port switching is enabled (CR11 = 1).

Internal Registers *(continued)*

Command Register 2 (RS value = 1001)

This register may be written to or read by the MPU at any time and is not initialized at power-up. CR20 corresponds to data bus bit D0, the least significant data bit. All command register bits are set to logical zero when a low signal is asserted on the RESET* pin.

CR27	SCLK Disabled (0) SCLK Enabled (1) SCLK Disabled	A logical zero must be written to this bit to enable SCLK to be output. A logical one written to this bit three-states the SCLK output.
CR26	Test Path Enable (0) Normal Operation (1) Test Path Enabled	When this bit is set to a logical zero, the device operates normally. A logical one enables certain test paths to be internally set up. This involves any input mode and any inputs that affect access to the color palette RAM. When this bit is set to a logical one, the pixel data is accessible on the MPU data bus. While this test mode is enabled, the device will not operate at speed.
CR25	PORTSEL Mask (0) Masked (1) Nonmasked	This bit determines the selection of the input port. It is logically ANDed with the PORTSEL pin. A logical zero selects the VGA port. When this bit is a logical one, the PORTSEL pin selects either the VGA or pixel port.
CR24	CLKSEL Enable (0) PCLK0 Selected (1) PCLK1 Selected	When this bit is a logical zero, PCLK0 is selected. When this bit is a logical one, PCLK1 is selected. To eliminate glitches on the SCLK output, switching between PCLKs should occur only when the multiplexing rate is 8:1 or 4:1. To ensure the integrity of the palette, the device should be put in sleep mode before switching clocks.
CR23	Display Mode Select (0) Noninterlaced (1) Interlaced	When this bit is a logical zero, the display format is noninterlaced. When the bit is a logical one, the display format is interlaced. The mode must be set properly to ensure proper operation of the internal cursor.
CR22	16-Bit/Pixel Palette Index Select (0) Sparse Indexing (1) Contiguous Indexing	When this bit is a logical zero, palette addressing is sparse. The RGB color component pixel data is mapped to the most significant bits of the RGB palette address. The least significant of the palette address bits are set to zero. When this bit is a logical one, palette addressing is contiguous. The RGB color component pixel data is mapped to the least significant bits of the palette address. The most significant bits of the address are set to zero.
CR21, 20	Cursor Mode Select (00) Cursor Disabled (01) Three-Color Cursor (10) Two-Color/Highlight Cursor (11) Two-Color/X-Windows Cursor	These bits determine the functionality of the onboard 64 x 64 x 2 or the 32 x 32 x 2 hardware cursor.

Command Register 3 (RS value = 1010, when bit CR07 in Command Register 0 is set to logical one.)

This register may be written to or read by the MPU at any time and is not initialized at power-up. CR30 corresponds to data bus bit D0, the least significant data bit. All command register bits are set to logical zero when a low signal is asserted on the RESET* pin.

CR37	Reserved (Logical Zero)	This bit is reserved for future expansion. A logical zero must be written to ensure proper operation.
CR36	Reserved (Logical Zero)	This bit is reserved for future expansion. A logical zero must be written to ensure proper operation.
CR35	Reserved (Logical Zero)	This bit is reserved for future expansion. A logical zero must be written to ensure proper operation.
CR34	Reserved (Logical Zero)	This bit is reserved for future expansion. A logical zero must be written to ensure proper operation.
CR33	2x Clock Multiplier (0) 2x Clock Multiplier Disabled (1) 2x Clock Multiplier Enabled.	This bit enables or disables the 2x multiplier. A logical one written to this bit enables the 2x on-chip TTL clock multiplier for high-speed operation. A logical zero written to CR33 will disable the clock multiplier and will allow the external clock source to directly drive the logic.
CR32	Cursor Select (0) 32x32x2 Cursor (1) 64x64x2 Cursor	This bit selects either a 64 x 64 or a 32 x 32 hardware cursor. A logical zero written to this bit will select the 32 x 32 cursor size, and a logical one will select the 64 x 64 cursor size.
CR31, 30	MSBs for 10-bit Address Counter CR31 = A9 CR30 = A8	These bits are the load inputs to the 2 MSBs of the 10-bit address counter. The 10-bit address counter can be set to access any particular location in the 64 x 64 x 2 cursor RAM array.

Internal Registers *(continued)*

Pixel Read Mask Register (RS value = 0010)

The 8-bit pixel read mask register may be written to or read by the MPU at any time, and *is not* initialized at power-up. D0 is the least significant bit. The contents of this register are bit-wise ANDed with the pixel data prior to addressing the color palette RAM. The pixel read mask register must be initialized by the user to logical ones for proper operation.

Status Register (RS value = 1010)

The 8-bit status register monitors certain device states and identifies devices. It may be read by the MPU at any time; MPU write cycles to this register are ignored. D0 is the least significant bit corresponding to SR0. This register is not reset during power-up/reset.

SR7–SR6: These bits are identification values. SR7=0 and SR6=1.
SR5–SR4: These bits are revision values.

SR3: This is the SENSE* bit. If it is a logical zero, one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level (335 mV). This bit is used to determine the presence of a CRT monitor, and, with diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The SENSE reference has an additional ±10-percent tolerance when an internal voltage reference is used.

SR2: (0) Write Cycle
(1) Read Cycle

Read/write access status. This bit provides RD/WR status when the register select bits equal $0, $3, $4, or $7. When address register $0 or $4 has been written, the device is in the write mode and this bit is a logical zero. When address register $3 or $7 has been written, the device is in the read mode and this bit is a logical one.

SR1–SR0: When read, these bits reflect the color component address for the next RD/WR cycle when the palette, cursor color registers, or overscan register are accessed: Address [a,b] state (00) Red Color Component
(01) Green Color Component
(10) Blue Color Component

Accessing Command Register 3

A fourth Command Register, CR3, was added to address the extended functionality of the Bt485 and to remain backwards compatible to the Bt484. Since there are only 4 register select lines (and all 16 combinations have already been used), CR3 must be accessed indirectly.

Command Register 3 is accessed with the following sequence of operations:

1. Set RS3–RS0 = 0110, Command Register 0.
2. Write a logical one to CR07.
3. Set RS3–RS0 = 0000, address register.
4. Write address register to 0000 0001.
5. Set RS3–RS0 = 1010.
6. Read or write Command Register 3.

With this indirect addressing, the status register can be accessed by writing 0000 0000 to the address register, as in step 4. The status register cannot be written to; it can only be read.

When a 64 x 64 x 2 cursor is selected (CR32 = 1), CR31 and CR30 must be written to use a 10-bit counter to address the larger RAM array. CR31 and CR30 become the load inputs to the 2 MSBs of the 10-bit address counter. Therefore, to set this counter to access a particular location in the 64 x 64 x 2 cursor RAM array, these 2 bits must be written to Command Register 3 before the lower 8 bits are written to the address counter through the MPU port. As the 10-bit address counter auto-increments, the new values of this counter can be read back through CR31 and CR30. The contents of this register will be reset with the assertion of the external RESET* pin.

Internal Registers *(continued)*

Cursor (x,y) Registers (RS values: CXLR = 1100, CXHR = 1101, CYLR = 1110, and CYHR = 1111)

These registers are used to specify the (x, y) coordinate of the 64 x 64 x 2 hardware cursor. The cursor (x) register contains the cursor (x) low register (CXLR) and the cursor (x) high register (CXHR); the cursor (y) register contains the cursor (y) low register (CYLR) and the cursor (y) high register (CYHR). The last value written by the MPU to these registers is the value returned on a read. These registers may be written to or read by the MPU at any time.

CXLR and CXHR are cascaded to form a 12-bit cursor (x) register. Similarly, CYLR and CYHR are cascaded to form a 12-bit cursor (y) register. Bits D4–D7 of CXHR and CYHR are ignored.

	Cursor (x) High (CXHR)				Cursor (x) Low (CXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Cursor (y) High (CYHR)				Cursor (y) Low (CYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The cursor (x) value to be written is calculated as follows:

Xp = desired display screen (x) position + 64 (or $0040)

where

the (x) reference point for the display screen, x = 0, is the upper left corner of the screen. The Xp position equation places the upper left corner of the cursor RAM array to the desired screen location. This allows the cursor position to be defined in the same coordinate space as the screen.

Values from 0 (or $0000) to 4095 (or $0FFF) may be written into the cursor (x) register. If Xp is equal to 0, the cursor will be offscreen (see Cursor Operation in the Circuit Description section).

The cursor (y) value to be written is calculated as follows:

Yp = desired display screen (y) position + 64 (or $0040)

where

the (y) reference point for the display screen, y = 0, is the upper left corner of the screen. The Yp position equation places the upper left corner of the cursor RAM array to the desired screen location. This allows the cursor position to be defined in the same coordinate space as the screen.

Values from 0 (or $0000) to 4095 (or $0FFF) may be written into the cursor (y) register. If Yp is equal to 0, the cursor will be entirely offscreen (see Cursor Operation).

Cursor (x, y) Registers (RS values: CXLR = 1100, CXHR = 1101, CYLR = 1110, and CYHR = 1111)

These registers are used to specify the (x, y) coordinate of the 32 x 32 x 2 hardware cursor. The cursor (x) register contains the cursor (x) low register (CXLR) and the cursor (x) high register (CXHR); the cursor (y) register contains the cursor (y) low register (CYLR) and the cursor (y) high register (CYHR). The last value written by the MPU to these registers is the value returned on a read. These registers may be written to or read by the MPU at any time.

CXLR and CXHR are cascaded to form a 12-bit cursor (x) register. Similarly, CYLR and CYHR are cascaded to form a 12-bit cursor (y) register. Bits D4–D7 of CXHR and CYHR are always logical zeros.

	Cursor (x) High (CXHR)				Cursor (x) Low (CXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Cursor (y) High (CYHR)				Cursor (y) Low (CYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The cursor (x) value to be written is calculated as follows:

Xp = desired display screen (x) position + 32 (or $0020)

where

the (x) reference point for the display screen, x = 0, is the upper left corner of the screen. The Xp position equation places the upper left corner of the cursor RAM array to the desired screen location. This allows the cursor position to be defined in the same coordinate space as the screen.

Values from 0 (or $0000) to 4095 (or $0FFF) may be written into the cursor (x) register. If Xp is equal to 0, the cursor will be offscreen (see Cursor Operation).

The cursor (y) value to be written is calculated as follows:

Yp = desired display screen (y) position + 32 (or $0020)

where

the (y) reference point for the display screen, y = 0, is the upper left corner of the screen. The Yp position equation places the upper left corner of the cursor RAM array to the desired screen location. This allows the cursor position to be defined in the same coordinate space as the screen.

Values from 0 (or $0000) to 4095 (or $0FFF) may be written into the cursor (y) register. If Yp is equal to 0, the cursor will be entirely offscreen (see Cursor Operation).

Pin Descriptions

Pin Name	Pin #	Description
RESET*	47	Reset input (TTL compatible). When this signal is low, all the command register bits are set to zero, and the device is in VGA mode. The pixel read mask register is not initialized on reset and must be initialized by the user to logical ones for proper operation (see Pixel Read Mask Register in the Circuit Description section).
CBLANK*	65	Composite blank control input (TTL compatible). A logical zero drives the analog outputs to the blanking level, as specified in Tables 9 and 10. CBLANK* is latched on the rising edge of LCLK. When BLANK* is a logical zero, the pixel inputs are ignored. The falling edge of this signal determines the polarity of the CSYNC* input pin. The onboard cursor positioning counters are referenced to this signal.
CSYNC*	64	Composite sync control input (TTL compatible). The polarity of this pin is determined on the last rising LCLK edge before the falling edge of CBLANK*. CSYNC* does not override any other control or data input, as shown in Tables 9 and 10; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of LCLK. Bits CR04–CR02 in Command Register 0 can permanently disable sync on the IOR, IOG, or IOB output.
CDE	63	Composite display enable control input (TTL compatible). The state of this signal and CBLANK* determines whether the analog outputs are blanked or contain cursor color, pixel , or overscan data. This signal is latched on the rising edge of LCLK. If overscanning is not used, this pin should be tied to CBLANK*. The following is a list of combinations of CDE and CBLANK*: PORTSEL CDE CLBANK* x x 0 Video Blanking 0 0 1 VGA Pixel Data 0 1 1 Cursor Color or VGA Data 1 0 1 Overscan Data 1 1 1 Cursor Color or Pixel Data
ODD / EVEN*	62	Odd/even field input (TTL compatible). This signal should be changed only during vertical blank. This input is used to ensure proper operation of the onboard cursor when interlaced operation (command bit CR23=1) is selected. When this signal is a logical zero, an even field is specified. When this signal is a logical one, an odd field is specified. This input is ignored if noninterlaced operation (command bit CR23=0) is selected.
PCLK0	78	Pixel Clock 0 input (TTL compatible). This clock is selected when CR24 in Command Register 2 is a logical zero. The signal on this pin should be the VGA pixel clock. This clock should be specified when switching between the pixel and VGA ports on a pixel-by-pixel basis (in 1:1 mode, only). It is recommended that all clock inputs be driven by a dedicated buffer to avoid reflection-induced jitter.
PCLK1	76	Pixel Clock 1 input (TTL compatible). This clock is selected when CR24 in Command Register 2 is a logical one. The signal on this pin is typically the high-speed pixel clock used during multiplexed operation of the pixel port.
SCLK	83	VRAM shift clock output (TTL compatible). The signal on this pin is equal to the selected pixel clock divided by 8, 4, 2, or 1, depending on the operating mode selected. If 2x clock multiplier is selected (CR33 = 1), then the SCLK output is equal to pixel clock divided by 4, 2, or 1, or pixel clock multiplied by 2, in 8:1, 4:1, 2:1, or 1:1 modes, respectively.

Pin Descriptions *(continued)*

Pin Name	Pin #	Description
LCLK	81	Latch Clock input (TTL compatible). The rising edge of this signal latches P7:0 (A–D) or VGA [7:0], and CBLANK*, CDE, CSYNC*, and PORTSEL. The information latched by this signal is synchronized internally with SCLK. Because of this synchronization process, there is a timing window on both sides of SCLK where LCLK must not rise (see AC Characteristics section). This timing window is necessary so that data latched by LCLK does not interfere with the setup and hold times required by the internal synchronizing latch. Data is synchronized with the selected pixel clock after being internally latched with SCLK. When the multiplexing rate is 8:1, 4:1, 2:1, or 1:1, this signal is equal to the selected pixel clock divided by 8, 4, 2, or 1, respectively.
P7:0 (A–D)	1–32	Pixel port inputs (TTL compatible). This port is selected if PORTSEL is a logical one and PORTSEL is not masked by CR25. The appropriate pins on this port are multiplexed at rates of either 1:1, 2:1, 4:1, or 8:1, depending on the operating mode selected. This port is latched on the rising edge of LCLK. P0 is the LSB. Unused inputs should be connected to GND.
VGA[7:0]	67–74	VGA port inputs (TTL compatible). This port is selected if PORTSEL is a logical zero. This port is multiplexed 1:1. This port is latched on the rising edge of LCLK. P0 is the LSB. Unused inputs should be connected to GND.
PORTSEL	66	VGA/pixel port select input (TTL compatible). This pin is ANDed with control register bit CR25 to determine whether the pixel port or VGA port is selected. A logical zero on this pin selects the VGA port regardless of the state of CR25. A logical one selects the pixel port if CR25 = 1. This pin may be used in 1:1 mode to switch between the pixel and VGA ports on a pixel-by-pixel basis. This pin may also be used to switch between the VGA and pixel ports in 2:1, 4:1, or 8:1 MUX modes on a frame-by-frame basis. This pin should not be left floating.
WR*	48	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of WR*, and RS0–RS3 are latched on the falling edge of WR* during MPU write operations. RD* and WR* should not be asserted simultaneously.
RD*	49	Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0–RS3 are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously.
RS0–RS3	50–53	Register select inputs (TTL compatible). RS0–RS3 specify the type of read or write operation being performed, as shown in Tables 1 and 2.
D0–D7	54–61	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
SENSE*	46	Comparator sense output (CMOS compatible). This pin will be low if one or more of the IOR, IOG, and IOB analog output levels exceed the internal comparator reference levels. The sense output can drive only one CMOS load.
IOR, IOG, IOB	35, 37, 39	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable. The PC Board Layout Considerations section contains further information.

Pin Descriptions *(continued)*

<table>
<tr><th>Pin Name</th><th>Pin #</th><th>Description</th></tr>
<tr><td>FSADJUST</td><td>33</td><td>Full-scale adjust control. The IRE relationships in Figures 4 and 5 are maintained, regardless of the full-scale output current.

When an external or the internal voltage reference (Figures 6 and 7 in the PC Board Layout Considerations section) is used, a resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between RSET and the full-scale output current on each output is:

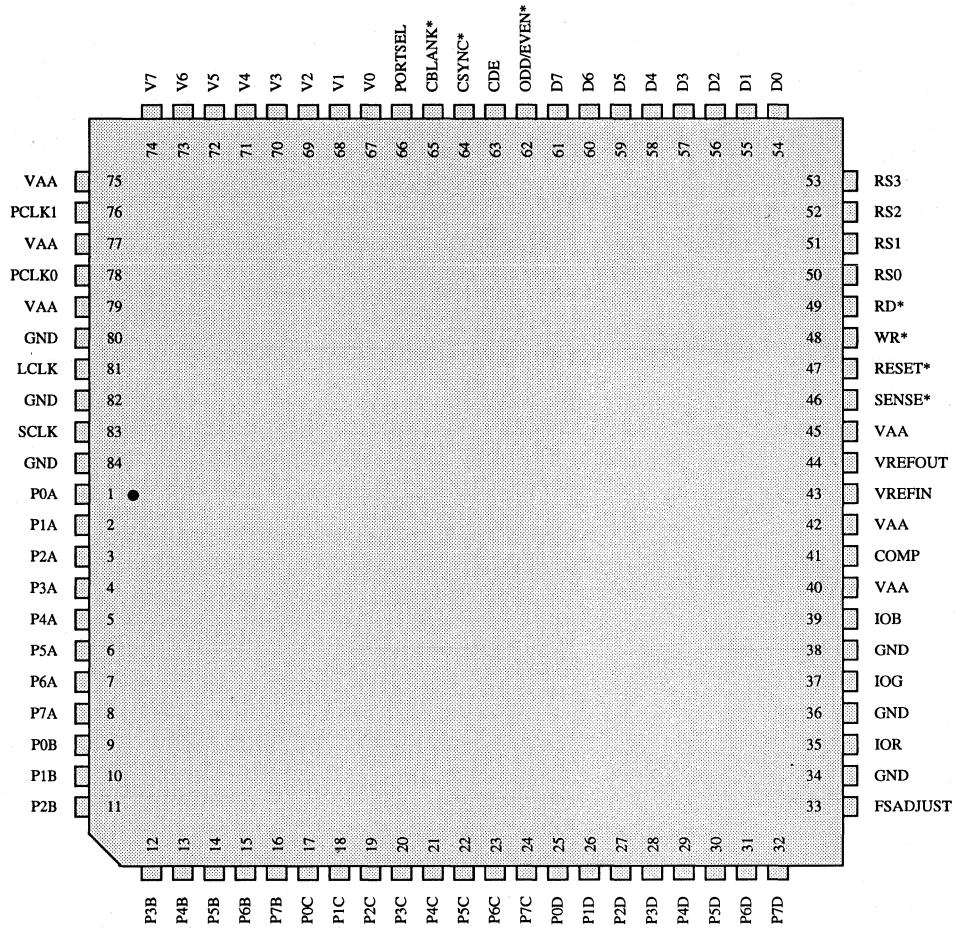
RSET (Ω) = K * 1,000 * VREF (V) / Iout (mA)

K is defined in the table below. It is recommended that a 147 Ω RSET resistor be used for doubly-terminated 75 Ω loads (i.e., RS-343A applications).

<table>
<tr><th></th><th colspan="2">Sync Enabled</th><th colspan="2">Sync Disabled</th></tr>
<tr><th>Setup</th><td>0 IRE</td><td>7.5 IRE</td><td>0 IRE</td><td>7.5 IRE</td></tr>
<tr><th>K (8 bits)</th><td>3.025</td><td>3.195</td><td>2.120</td><td>2.280</td></tr>
<tr><th>K (6 bits)</th><td>3.000</td><td>3.170</td><td>2.100</td><td>2.260</td></tr>
</table>

K values are subject to change upon completion of characterization.</td></tr>
<tr><td>VREF OUT</td><td>44</td><td>Voltage reference output. This output provides a 1.235 V (typical) reference and may be connected directly to the VREF pin. If the on-chip reference is not used, this pin may be left floating. (See Figures 6 and 7.) Up to four Bt485s can be driven by this output.</td></tr>
<tr><td>VREF IN</td><td>43</td><td>Voltage reference input. If an external voltage reference is used (Figure 7), it must supply this input with a 1.235 V (typical) reference. A 0.1 µF ceramic capacitor must be used to decouple this input to GND, as shown in Figures 6 and 7. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. When the internal reference is used, this pin should not drive any external circuitry, except the decoupling capacitor (Figure 6).</td></tr>
<tr><td>COMP</td><td>41</td><td>Compensation pin. A 0.1 µF ceramic capacitor must be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
<tr><td>VAA</td><td>40, 42, 45, 75, 77, 79</td><td>Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
<tr><td>GND</td><td>34, 36, 38, 80, 82, 84</td><td>Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup. Refer to the PC Board Layout Considerations section for critical layout criteria.</td></tr>
</table>

Pin Descriptions *(continued)*



PC Board Layout Considerations

PC Board Considerations

For optimum performance of the Bt485, proper CMOS RAMDAC layout techniques should be studied in the Bt451/7/8 Evaluation Module Operation and Measurements, Application Note (AN-16), before PC board layout is begun. This application note can be found in Brooktree's *Applications Handbook*.

The layout should be optimized for lowest noise on the Bt485 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

Component Placement

Components should be placed as close as possible to the associated RAMDAC pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt485 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt485 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 6 and 7. This bead should be located within 3 inches of the Bt485. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor, decoupling each of the two groups of VAA pins to GND. For operation above 75 MHz, a 0.1 µF capacitor in parallel with a 0.01 µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 10 µF capacitor shown in Figures 6 and 7 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to GND.

Digital Signal Interconnect

The digital inputs to the Bt485 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω). The RS-select inputs and RD*/WR* lines must be verified for proper levels with no ringing, undershoot, or overshoot. Ringing on these lines can cause improper operation.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Clock Interfacing

The Bt485 requires a pixel clock with monotonic clock edges for proper operation. Impedance mismatch on the pixel clock line will induce reflections on the pixel clock, which may cause erratic operation.

The Pixel Clock Pulse Width High Time and Pixel Clock Pulse Width Low Time minimum specifications (see the AC Characteristics section) must not be violated, or erratic operation can occur.

The pixel clock line must be terminated to prevent impedance mismatch. A series termination of 33–68 Ω placed at the pixel clock driver may be used, or a parallel termination may be used at the pixel clock input to the RAMDAC. A parallel termination of 220 Ω to VCC and 330 Ω to ground will provide a Thevenin equivalent of a 110 Ω termination, which is normally sufficient to absorb reflections. The series or parallel resistor values should be adjusted to provide the optimum clock signal fidelity.

MPU Control Signal Interfacing

The Bt485 uses the RD*, WR*, and RS lines to determine which MPU accesses will take place. Glitches or ringing on any of these lines may cause improper MPU operation. When a VGA controller with edge rate control is used on these lines, a series termination is not necessary. In non-VGA controller application or in applications where the MPU control signals are daisy chained, a series termination, pull-down resistors, or additional capacitance to ground should be used to prevent glitches that could cause improper MPU accesses.

Analog Signal Interconnect

The Bt485 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt485 to minimize reflections. Unused analog outputs should be connected to GND.

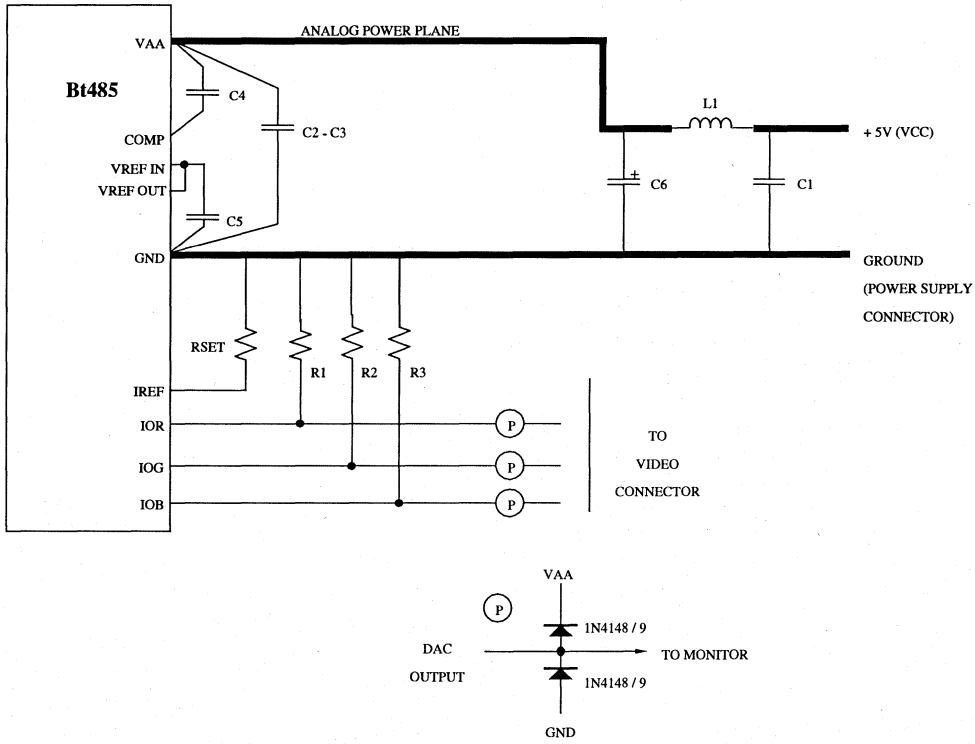
Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt485 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figures 6 and 7 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations *(continued)*



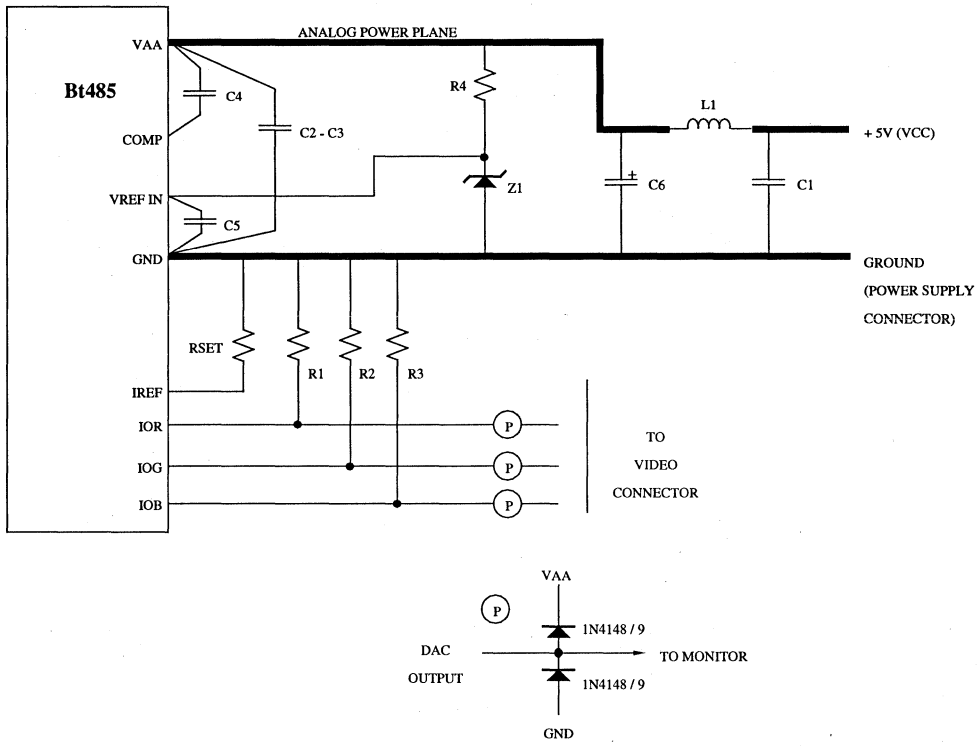
Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt485.

Figure 6. Typical Connection Diagram and Parts List (Internal Voltage Reference).

PC Board Layout Considerations *(continued)*



Note: Each set of VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1 kΩ 5% resistor	
RSET	147 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt485.

Figure 7. Typical Connection Diagram and Parts List (External Voltage Reference).

Application Information

Using Multiple Devices

When multiple Bt485s are used, each Bt485 should have its own power plane ferrite bead. If the internal reference is used, each Bt485 should use its own internal reference.

Although the multiple Bt485s may be driven by a common external voltage/current reference, higher performance may be obtained if each RAMDAC uses its own reference. This will reduce the amount of color channel crosstalk and color palette interaction.

Each Bt485 must still have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and reference capacitors.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Reference Selection

An external voltage reference provides about ten times the power supply rejection on the analog outputs than does an external current reference.

Sleep Operation

When the internal or external voltage reference is used, the DACs will be turned off during sleep mode.

When an external voltage reference is used, some internal circuitry will still be powered during the sleep mode, resulting in 0.5 mA of power supply current being drawn (above the rated supply current specifications). This unnecessary current drain can be disabled by turning off the external voltage reference during sleep mode.

Recommended Operating Conditions

(All numbers are preliminary and will be finalized upon completion of characterization)

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Voltage Reference Configuration	VREF				V
Reference Voltage		1.112	1.235	1.359	

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on Any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

(All numbers are preliminary and will be finalized upon completion of characterization)

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT			7	pF

See test conditions on next page.

DC Characteristics *(continued)*

(All numbers are preliminary and will be finalized upon completion of characterization)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Gray-Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level		6.29	7.62	8.96	mA
Sync Level		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.5	V
Output Impedance	RAOUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT			30	pF
Onboard VREF	VREFOUT	TBD	TBD	TBD	V
Voltage Reference Input Current	IVR IN				mA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR			0.5	% / % ΔVAA

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, SETUP = 7.5 IRE, RSET = 147 Ω, and VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

When the internal voltage reference is used, RSET may require adjustment to meet these limits. Also, the gray-scale output current (white level relative to black) will have a typical tolerance of ±10 percent rather than the ±5 percent specified above.

Note 1: When the Bt485 is in the 6-bit mode, the output levels are approximately 1.5-percent lower than these values.

AC Characteristics

(All numbers are preliminary and will be finalized upon completion of characterization)

		135 MHz Devices			110 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
PCLK 0, PCLK 1 All MUX Rates	Fmax			135			110	MHz
RS0–RS3 Setup Time (Figure 8)	1	10			10			ns
RS0–RS3 Hold Time	2	10			10			ns
RD* Asserted to D0–D7 Driven	3	2			2			ns
RD* Asserted to D0–D7 Valid	4			40			40	ns
RD* Negated to D0–D7 3-Stated	5			20			20	ns
Read D0–D7 Hold Time	6	2			2			ns
Write D0–D7 Setup Time	7	10			10			ns
Write D0–D7 Hold Time	8	10			10			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	6*pclk			6*pclk			ns
LCLK Rates (Figures 9 and 10)	Lmax							
8:1 Multiplexing				16.9			13.75	MHz
4:1 Multiplexing				33.8			27.5	MHz
2:1 Multiplexing				67.5			55	MHz
1:1 Multiplexing or VGA				90			90	MHz
SCLK Rate	Smax							
8:1 Multiplexing				16.9			13.75	MHz
4:1 Multiplexing				33.8			27.5	MHz
2:1 Multiplexing				42.50			37.50	MHz
1:1 Multiplexing or VGA				50.35			50.35	MHz
PCLK 0, PCLK 1 Cycle Time (Note 1) All MUX Rates	11	14.81			18.18			ns
PCLK 0, PCLK 1 Pulse Width High All MUX Rates	12	tbd			tbd			ns
PCLK 0, PCLK 1 Pulse Width Low All MUX Rates	13	tbd			tbd			ns
Duty Cycle 2xPCLK		tbd	tbd	tbd	tbd	tbd	tbd	%
LCLK Cycle Time	14							
8:1 Multiplexing		59.17			72.72			ns
4:1 Multiplexing		29.58			36.36			ns
2:1 Multiplexing		14.81			18.18			ns
1:1 Multiplexing or VGA		11.11			11.11			ns
LCLK Pulse Width High	15							
8:1 Multiplexing		4			4			ns
4:1 Multiplexing		4			4			ns
2:1 Multiplexing		4			4			ns
1:1 Multiplexing or VGA		4			4			ns
LCLK Pulse Width Low	16							
8:1 Multiplexing		4			4			ns
4:1 Multiplexing		4			4			ns
2:1 Multiplexing		4			4			ns
1:1 Multiplexing or VGA		4			4			ns

See test conditions at end of this section.

AC Characteristics *(continued)*

(All numbers are preliminary and will be finalized upon completion of characterization)

		135 MHz Devices			110 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
SCLK Cycle Time	17							
8:1 Multiplexing		59.17			72.72			ns
4:1 Multiplexing		29.58			36.36			ns
2:1 Multiplexing		23.53			26.67			ns
1:1 Multiplexing or VGA		19.86			19.86			ns
Data Setup to LCLK P7:0(A-D)	18	1			1			ns
Data Hold from LCLK P7:0(A-D)	19	5			5			ns
Data Setup and Hold to LCLK VGA(7:0), CDE, CBLANK*	20	3			3			ns
CSYNC*, PORTSEL								ns
LCLK valid skew with respect to SCLK (Note 2)	21	–3		T–14	–3		T–14	ns
SCLK Output Delay (1:1 mode) (Note 3)								
SCLK Output Delay (MUX mode) (Note 3)	22		6	11			11	ns
Analog Output Delay			10	20			20	ns
Analog Output Rise/Fall Time				30			30	ns
Analog Output Settling Time (Note 4)	23		3					ns
Clock and Data Feedthrough (Note 4)	24		13					ns
Glitch Impulse (Note 4)	25		–30					dB
SENSE* Output Delay			75					pV - sec
DAC-to-DAC Crosstalk	26		1					µs
Analog Output Skew			–23					dB
				2			2	ns
VAA Supply Current (Note 5)								
Normal Operation	IAA							mA
Sleep Mode (Note 6)			TBD	TBD			TBD	mA
			TBD	TBD			TBD	mA

See test conditions at end of this section.

Pipeline Delay	MIN	MAX
1:1/VGA mode	8 LCLKS	8 LCLKS
2:1 mode	1 LCLK + 7 PCLKS	1 LCLK + 8 PCLKS
4:1 mode	1 LCLK + 7 PCLKS	1 LCLK + 10 PCLKS
8:1 mode	1 LCLK + 7 PCLKS	1 LCLK + 14 PCLKS

Pipeline delay (MIN) is the minimum number of clocks required to output 1 pixel after all pixels have been latched. Pipeline delay (MAX) is the maximum number of clocks required to output all pixels after all pixels have been latched. In the 1:1/VGA mode, LCLK is the primary clock latching and pipelining for the pixels.

AC Characteristics *(continued)*

(All numbers are preliminary and will be finalized upon completion of characterization)

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, SETUP = 7.5 IRE, VREF = 1.235 V, and RSET = 147 Ω. TTL input values are 0–3 V with input rise/fall times ≤3 ns, measured between the 10-percent and 90-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤10 pF; SENSE* and D0–D7 output load ≤50 pF. SCLK output load = 50 pF. See timing notes in Figures 8 and 9. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

Note 1: To pipeline data at 110 or 135 MHz, the 2 x clock multiplier must be activated. Duty cycle range TBD.

Note 2: T = SCLK cycle time. Approximate numbers based on Bt484. Actual specifications will be determined upon characterization of the Bt485.

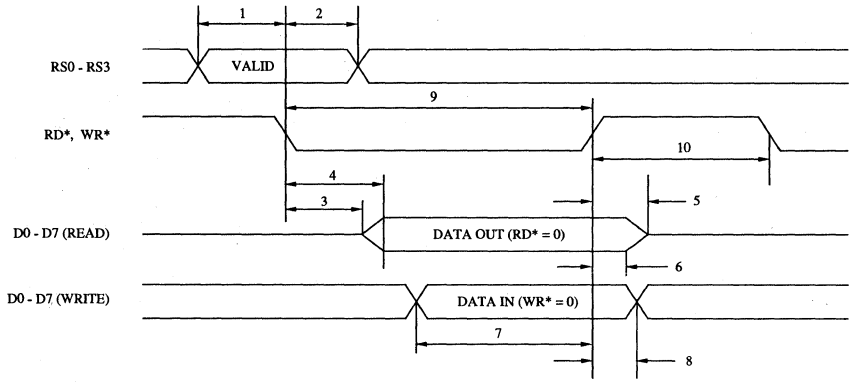
Note 3: Approximate numbers based on Bt484. Actual specifications will be determined upon characterization of the Bt485.

Note 4: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 5: At 135 MHz. IAA (typ) at VAA = 5.0 V, 25°C. IAA (max) at VAA = 5.25 V, 70°C. 4:1 MUX mode at 40-percent blanking.

Note 6: External voltage reference is disabled during sleep mode, all inputs are low, and clock is running.

Timing Waveforms



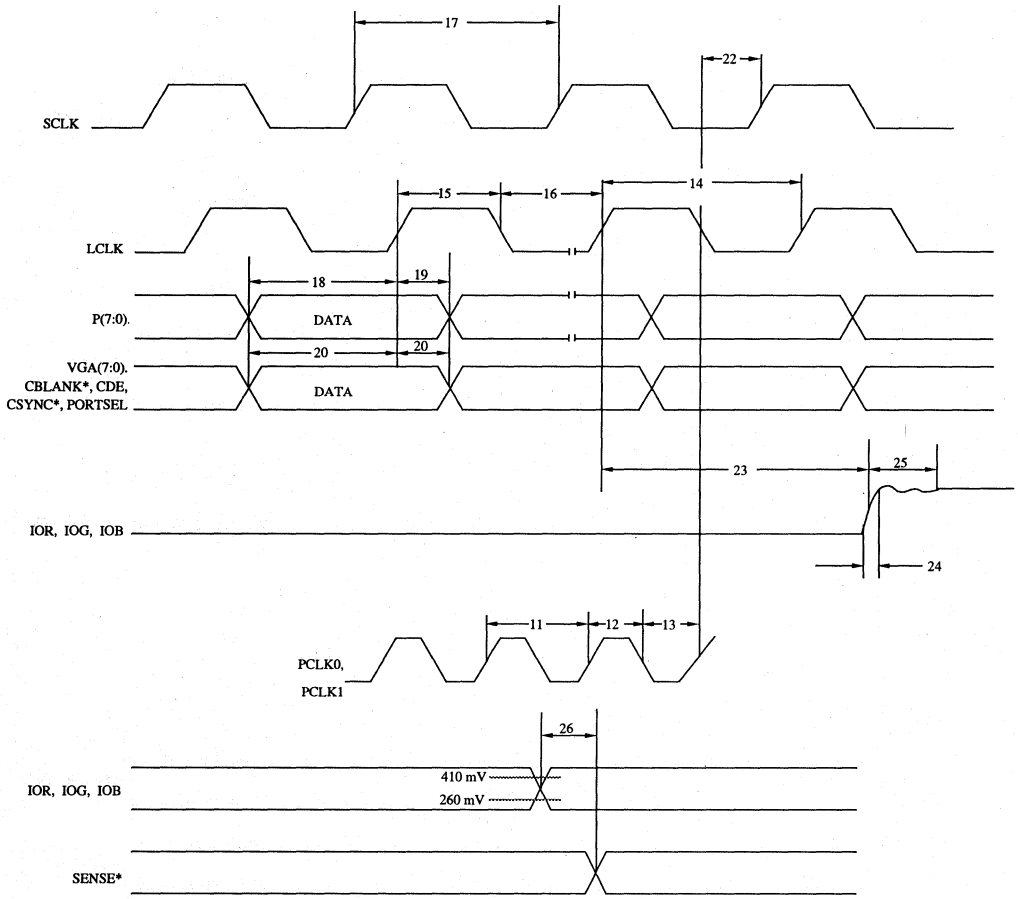
Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 8. MPU Read/Write Timing.

Timing Waveforms *(continued)*



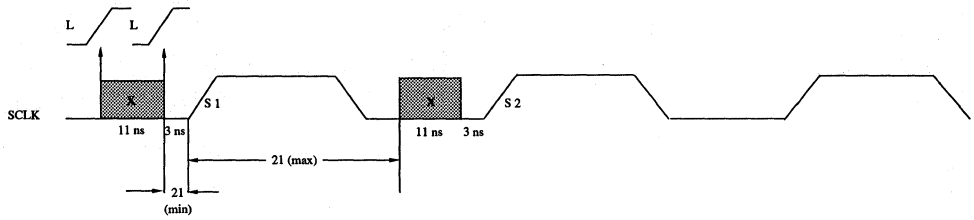
Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of

Figure 9. Video Input/Output Timing (Non-1:1).

Timing Waveforms *(continued)*



L = LCLK rising edges

S1 = First SCLK rising edge

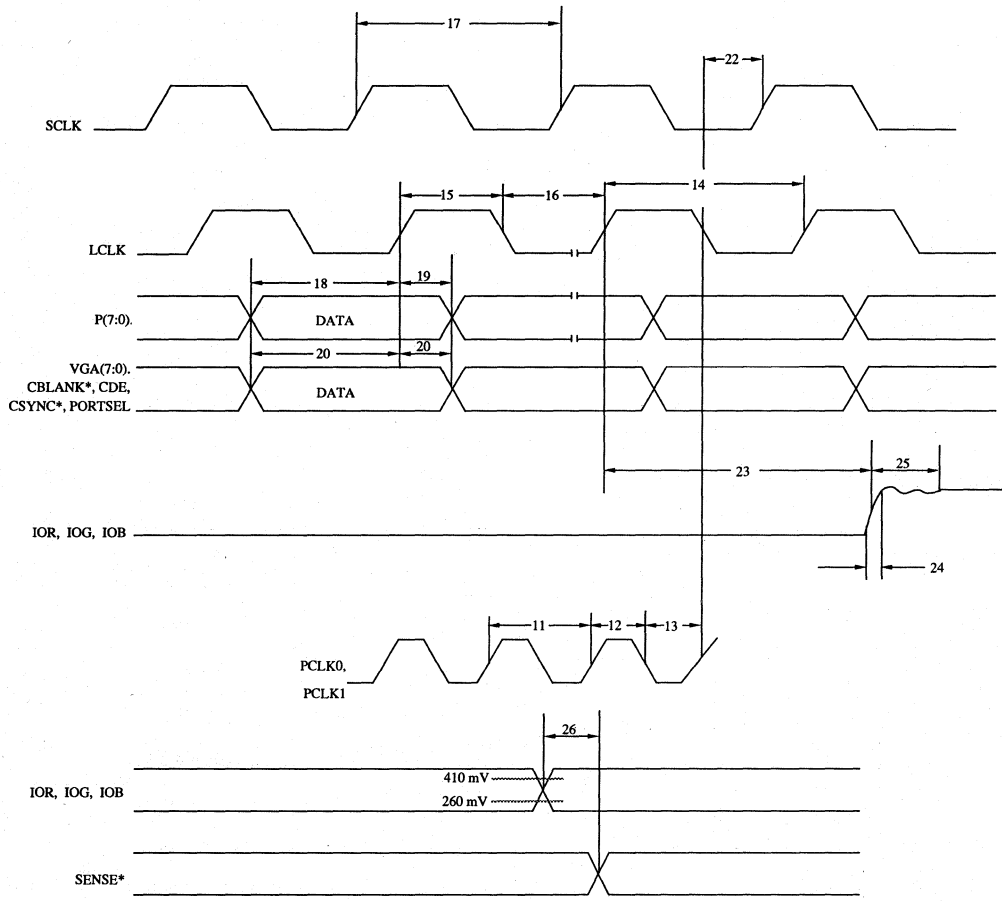
S2 = Second SCLK rising edge

In order for the pixel data latched by LCLK to be synchronized correctly with the internal PCLK clock, an LCLK rising edge cannot occur in an invalid window, as illustrated above.

If L occurs within the 11 ns invalid region (X), it is not guaranteed on which rising edge of SCLK (S1 or S2) the data will be synchronized. If L occurs before the 11 ns invalid region (X), then the data is guaranteed to be synchronized on S1. If L occurs after the 11 ns invalid region (X), then the data will not be synchronized on S1 and is guaranteed to be synchronized on S2.

Figure 9 (continued). Video Input/Output Timing (Non-1:1).

Timing Waveforms *(continued)*



Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 10. Video Input/Output Timing (1:1 MUX Rates).

4

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt485KPJ135	135 MHz	84-pin Plastic J-Lead	0° to +70°C
Bt485KPJ110	110 MHz	84-pin Plastic J-Lead	0° to +70°C