Semiconductor Corporation

CS4231

Parallel Interface, Multimedia Audio Codec

Features

- ADPCM Compression/Decompression
- Free Windows™ Software Drivers
- MPC Compatible Mixer
- Dual DMA Count Registers for Full Duplex Operation
- DMA Transfers with On-chip FIFOs.
- Timer for Audio/Visual Synchronization
- 16 mA Bus Drive Capability
- Digital 3.3/5V Operation
- Pin Compatible with CS4248/AD1848

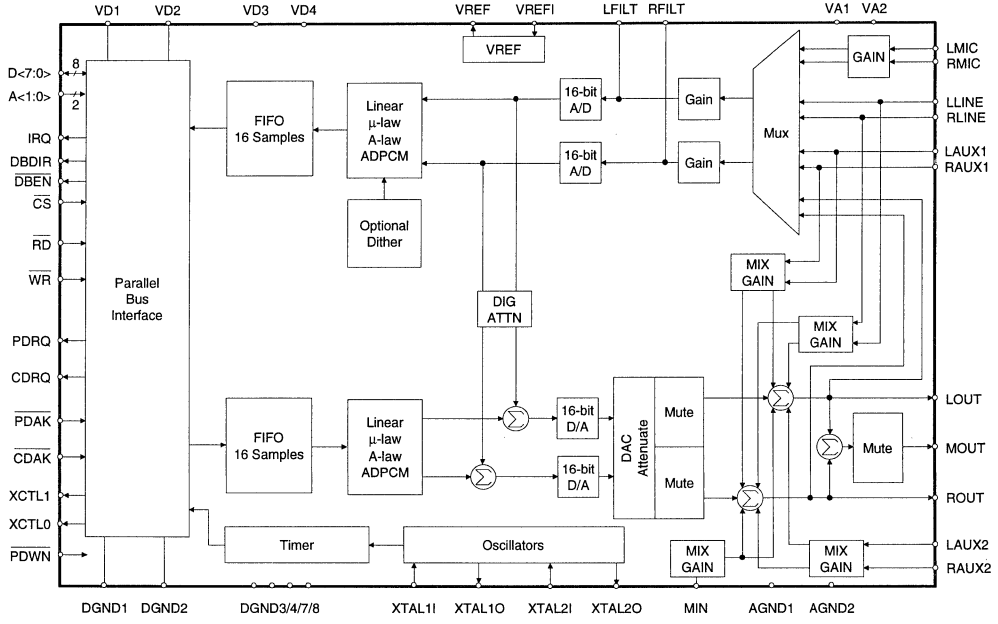
General Description

mwave The CS4231 is an Mwave™ audio codec.

The CS4231 provides 16-bit audio for computer multimedia systems. The CS4231 includes stereo audio converters and complete on chip filtering for record and playback of 16-bit audio data, plus analog mixing and programmable gain and attenuation are included to provide a complete audio subsystem. Free high-performance Windows software drivers are available that support all the CS4231 features including full duplex transfers. The CS4231 is a pin compatible upgrade to the CS4248 and AD1848 (PLCC Version).

ORDERING INFORMATION:

CS4231-KL	0 to 70°C	68-pin PLCC
CS4231-KQ	0 to 70°C	100-pin TQFP



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
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ANALOG CHARACTERISTICS (T_A = 25°C; VA1, VA2, VD1-VD4 = +5V;

Input Levels: Logic 0 = 0V, Logic 1 = VD1-VD4; 1 kHz Input Sine wave; Conversion Rate = 48 kHz; Measurement Bandwidth is 10 Hz to 20 kHz, 16-bit linear coding.)

Parameter *		Symbol	Min	Typ	Max	Units
Analog Input Characteristics - Minimum gain setting (0 dB); unless otherwise specified.						
ADC Resolution	(Note 1)		16	-	-	Bits
ADC Differential Nonlinearity	(Note 1)		-	-	±0.5	LSB
Instantaneous Dynamic Range	Line Inputs (Note 2) Mic Inputs	IDR	80 72	85 77	- -	dB dB
Total Harmonic Distortion	Line Inputs Mic Inputs	THD	0.02 0.025	0.003 0.01	- -	% %
Signal-to-Intermodulation Distortion			-	90	-	dB
Interchannel Isolation	Line to Line Inputs Line to Mic Inputs Line-to-AUX1 Line-to-AUX2		- - - -	80 80 90 90	- - - -	dB dB dB dB
Interchannel Gain Mismatch	Line Inputs Mic Inputs		- -	- -	0.5 0.5	dB dB
Programmable Input Gain Span	Line Inputs		21.5	22.5	-	dB
Gain Step Size			1.3	1.5	1.7	dB
ADC Offset Error	0 dB gain		-	10	100	LSB
Gain Error			-	-	5	%
Full Scale Input Voltage:	(MGE=1) MIC Inputs (MGE=0) MIC Inputs LINE, AUX1, AUX2, MIN Inputs		0.266 2.66 2.66	0.29 2.9 2.9	0.31 3.1 3.1	V_{pp} V_{pp} V_{pp}
Gain Drift			-	100	-	ppm/°C
Input Resistance	(Note 1)		20	-	-	kΩ
Input Capacitance	(Note 1)		-	-	15	pF

Notes: 1. This specification is guaranteed by characterization, not production testing.
2. MGE = 1 and a 10µF capacitor on the VREF pin.

* Parameter definitions are given at the end of this data sheet.

ANALOG CHARACTERISTICS (Continued)

Parameter *			Symbol	Min	Typ	Max	Units
Analog Output Characteristics - Minimum Attenuation (0 dB); Unless Otherwise Specified.							
DAC Resolution				16	-	-	Bits
DAC Differential Nonlinearity		(Note 1)		-	-	±0.5	LSB
Dynamic Range	- Total - Instantaneous	All Outputs	TDR IDR	- 80	95 85	- -	dB dB
Total Harmonic Distortion		(Note 4)	THD	0.02	0.01	-	%
Signal-to-Intermodulation Distortion				-	85	-	dB
Interchannel Isolation	Line Out	(Note 4)		-	95	-	dB
Interchannel Gain Mismatch		Line Out		-	0.1	0.5	dB
Voltage Reference Output				2.0	2.15	2.3	V
Voltage Reference Output Current		(Note 3)		-	100	-	µA
DAC Programmable Attenuation Span				93	94.5	-	dB
DAC Attenuation Step Size		0 dB to -81 dB -82.5 dB to -94.5 dB		1.3 1.0	1.5 1.5	1.7 2	dB dB
DAC Offset Voltage				-	1	10	mV
Full Scale Output Voltage	OLB = 0 OLB = 1	(Notes 4, 5) OUT, MOUT		1.85 2.66	2.0 2.9	2.25 3.2	V_{pp} V_{pp}
Gain Drift				-	100	-	ppm/°C
Deviation from Linear Phase		(Note 1)		-	-	1	Degree
External Load Impedance				10	-	-	kΩ
Mute Attenuation (0 dB)				80	-	-	dB
Total Out-of-Band Energy	(Note 1)	0.6×Fs to 3 MHz		-	-	-45	dB
Audible Out-of-Band Energy	(Fs = 8kHz)	0.6×Fs to 22 kHz		-	-	-60	dB
Power Supply							
Power Supply Current		Digital, Operating Analog, Operating Total Digital, Power Down Analog, Power Down		- - - - -	55 43 98 - -	65 60 120 1 1	mA mA mA mA mA
Power Supply Rejection	1kHz	(Note 1)		40	-	-	dB

Notes: 3. DC current only. If dynamic loading exists, then the voltage reference output must be buffered or the performance of ADCs and DACs will be degraded.
4. 10 kΩ, 100 pF load.
5. All mixer and output gain tables assume the output level bit, OLB, in indirect register 16 (I16) is set, wherein the input and output full scale values are equal. When OLB=0, the output value is 3 dB below the input value, given no gain or attenuation.

AUXILIARY INPUT MIXERS (T_A = 25°C; VA1, VA2, VD1-VD4 = +5V;

Input Levels: Logic 0 = 0V, Logic 1 = VD1-VD4; 1 kHz Input Sine Wave)

Parameter		Symbol	Min	Typ	Max	Units
Mixer Gain Range Span	LINE, AUX1, AUX2 (Note 6) MIN		45 42	46.5 45	- -	dB dB
Step Size	LINE, AUX1, AUX2 MIN		1.3 2.3	1.5 3.0	1.7 3.4	dB dB

Note: 6. All mixer gain values assume OLB=1. If OLB=0, the analog output will be 3 dB below listed settings.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Max	Units
Power Supplies:	Digital Analog	VD1-VD4 VA1,VA2	-0.3 -0.3	6.0 6.0	V V
Input Current Per Pin	(Except Supply Pins)		-10	10	mA
Output Current Per Pin	(Except Supply Pins)		-50	50	mA
Analog Input Voltage			-0.3	VA+0.3	V
Digital Input Voltage			-0.3	VD+0.3	V
Ambient Temperature	(Power Applied)		-55	+125	°C
Storage Temperature			-65	+150	°C

Warning: Operation beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies:	Digital Analog	VD1-VD4 VA1,VA2	4.75 4.75	5.0 5.0	5.25 5.25	V V
Operating Ambient Temperature		T_A	0	25	70	°C

DIGITAL FILTER CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
Passband			0	-	0.40×Fs	Hz
Frequency Response			-0.5	-	+ 0.2	dB
Passband Ripple	(0-0.4×Fs)		-	-	±0.1	dB
Transition Band			0.40×Fs	-	0.60×Fs	Hz
Stop Band			0.60×Fs	-	-	Hz
Stop Band Rejection			74	-	-	dB
Group Delay			-	-	30/Fs	s
Group Delay Variation vs. Frequency	ADCs DACs		- -	- -	0.0 0.1/Fs	µs µs

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DIGITAL CHARACTERISTICS (T_A = 25°C; VA1, VA2, VD1-VD4 = 5V; AGND1, AGND2, DGND1-DGND4, DGND7, DGND8 = 0V.)

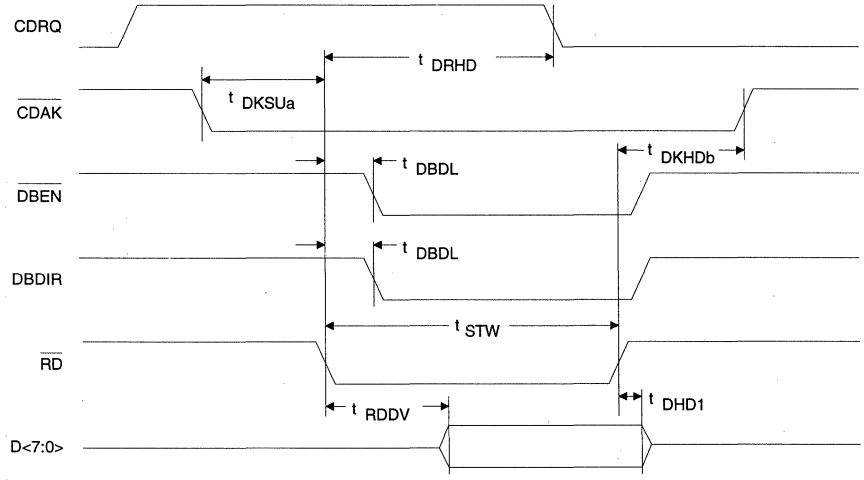
Parameter			Symbol	Min	Max	Units
High-level Input Voltage		Digital Inputs XTAL1I/XTAL2I, $\overline{PDWN}$	V_{IH}	2.0 VD-1.0	VD+ 0.3 VD+ 0.3	V V
Low-level Input Voltage			V_{IL}	-0.3	0.8	V
High-level Output Voltage:	D<7:0> All Others	I_O = -16.0 mA I_O = -1.0 mA	V_{OH}	2.4 2.4	VD VD	V V
Low-level Output Voltage:	D<7:0> All Others	I_O = 16.0 mA I_O = 4.0 mA	V_{OL}	- -	0.4 0.4	V V
Input Leakage Current		(Digital Inputs)	-	-10	10	µA
Output Leakage Current		(High-Z Digital Outputs)	-	-10	10	µA

TIMING PARAMETERS

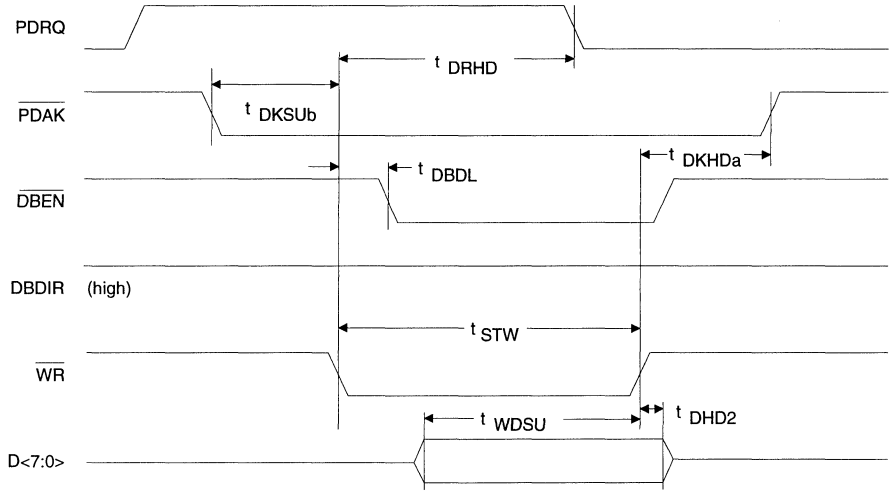
Parameter	Description		Min	Max	Units
t_{STW}	$\overline{WR}$ or $\overline{RD}$ strobe width		90	-	ns
t_{WDSU}	Data valid to $\overline{WR}$ rising edge	(write cycle)	22	-	ns
t_{RDDV}	$\overline{RD}$ falling edge to data valid	(read cycle)	-	60	ns
t_{CSSU}	$\overline{CS}$ setup to $\overline{WR}$ or $\overline{RD}$ falling edge		10	-	ns
t_{CSHD}	$\overline{CS}$ hold from $\overline{WR}$ or $\overline{RD}$ rising edge		0	-	ns
t_{ADSU}	ADDR <> setup to $\overline{RD}$ or $\overline{WR}$ falling edge		22	-	ns
t_{ADHD}	ADDR <> hold from $\overline{WR}$ or $\overline{RD}$ rising edge		10	-	ns

TIMING PARAMETERS (continued)

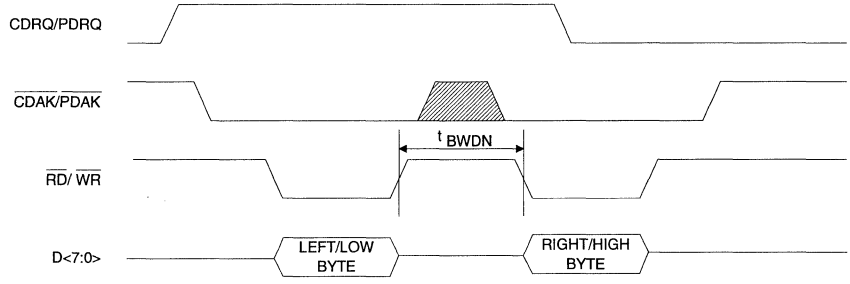
Parameter	Description	Min	Max	Units
t_{SUDK1}	$\overline{DAK}$ inactive to $\overline{WR}$ or $\overline{RD}$ falling edge (DMA cycle completion immediately followed by a PIO cycle)	60	-	ns
t_{SUDK2}	$\overline{DAK}$ active from $\overline{WR}$ or $\overline{RD}$ rising edge (PIO cycle completion immediately followed by DMA cycle)	0	-	ns
t_{DKSUa} t_{DKSUb}	$\overline{DAK}$ setup to $\overline{RD}$ falling edge (DMA cycles) $\overline{DAK}$ setup to $\overline{WR}$ falling edge	25 25	- -	ns ns
t_{DHD2}	Data hold from $\overline{WR}$ rising edge	15	-	ns
t_{DRHD}	DRQ hold from $\overline{WR}$ or $\overline{RD}$ falling edge (assumes no more DMA cycles needed)	0	25	ns
t_{BWDN}	Time between rising edge of $\overline{WR}$ or $\overline{RD}$ to next falling edge of $\overline{WR}$ or $\overline{RD}$	80	-	ns
t_{DHD1}	Data hold from $\overline{RD}$ rising edge	0	20	ns
t_{DKHDa} t_{DKHDb}	$\overline{DAK}$ hold from $\overline{WR}$ rising edge $\overline{DAK}$ hold from $\overline{RD}$ rising edge	25 25	- -	ns ns
t_{DBDL}	$\overline{DBEN}$ or $\overline{DBDIR}$ active from $\overline{WR}$ or $\overline{RD}$ falling edge		40	ns
t_{PDWN}	$\overline{PDWN}$ pulse width low	200	-	ns



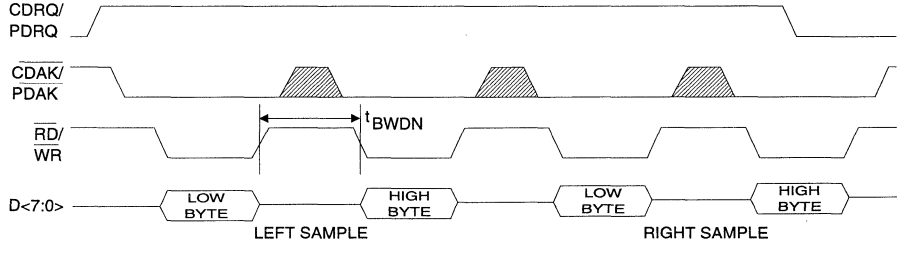
8-Bit Mono DMA Read/Capture Cycle



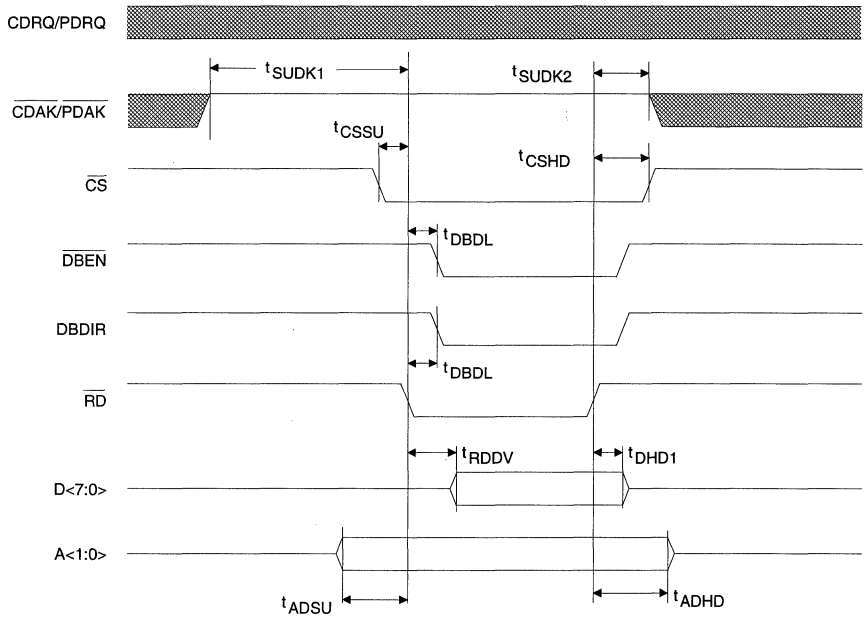
8-Bit Mono DMA Write/Playback Cycle



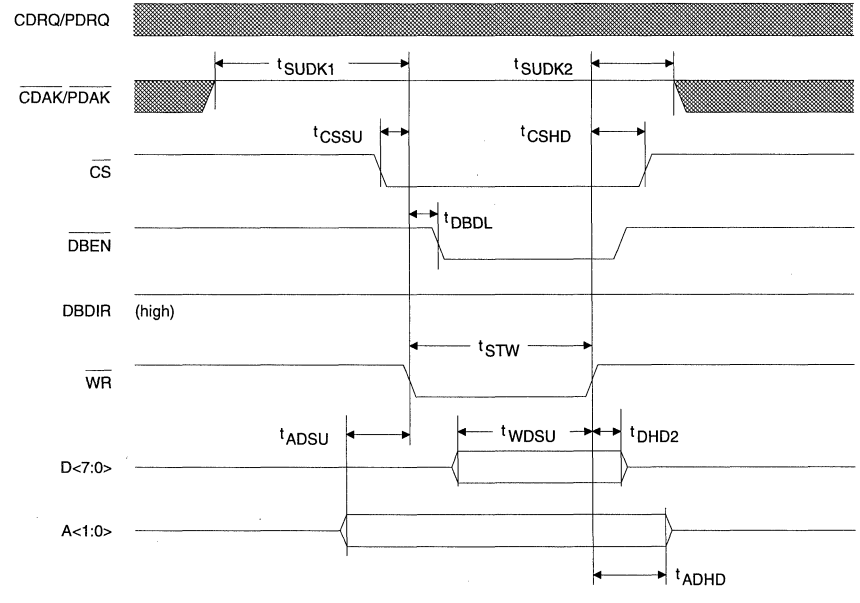
8-Bit Stereo or 16-Bit Mono DMA Cycle



16-Bit Stereo DMA Cycle



I/O Read Cycle



I/O Write Cycle

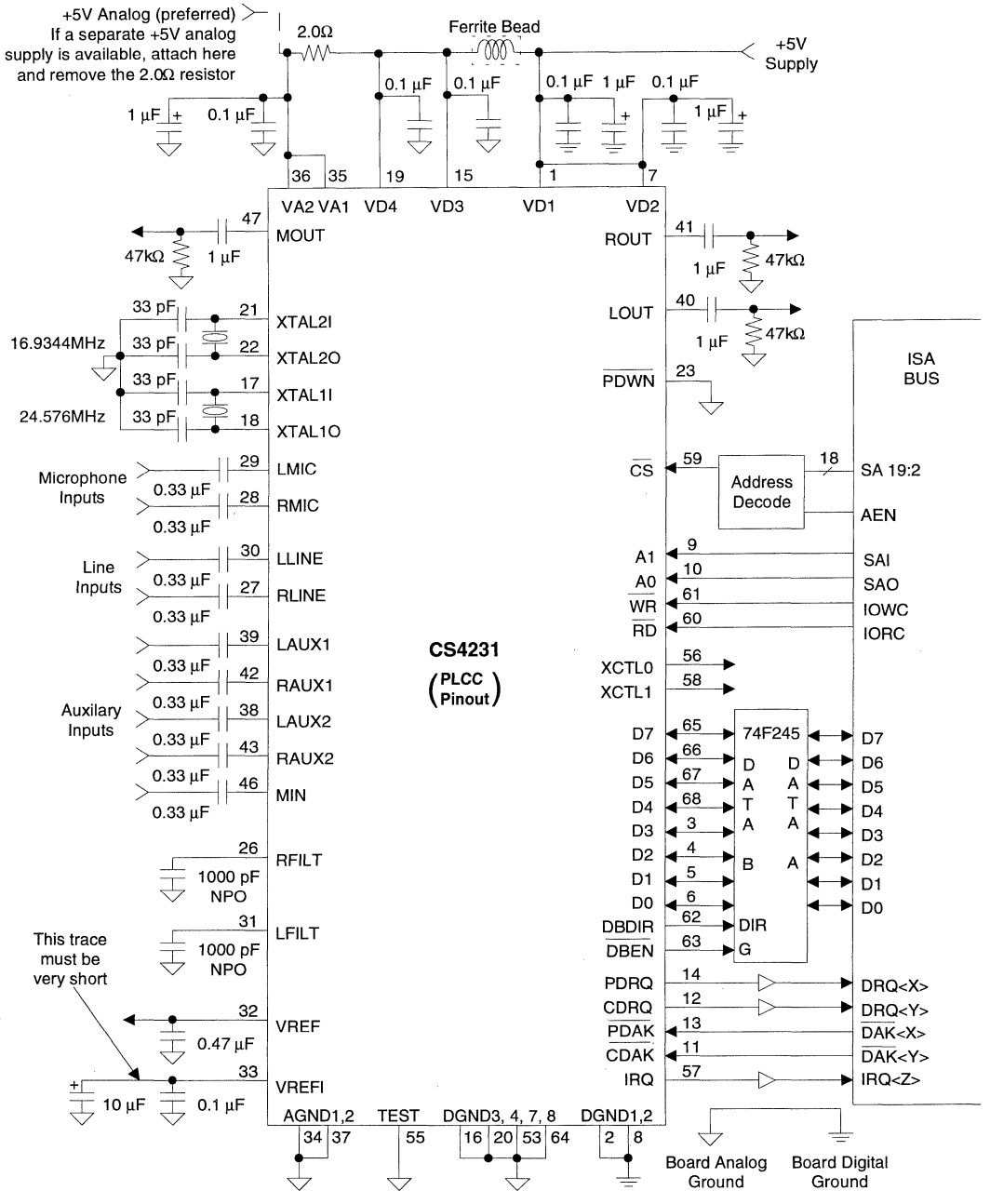


Figure 1. Recommended Connection Diagram
(See Figures 16 & 17 for Layout Recommendations)

GENERAL DESCRIPTION

The CS4231 is a monolithic integrated circuit that provides audio in personal computers or other parallel interface environments. The functions include stereo Analog-to-Digital and Digital-to-Analog converters (ADCs and DACs), analog mixing, anti-aliasing and reconstruction filters, line and microphone level inputs, optional A-Law / μ-Law coding, simultaneous capture and playback (at the same sample rates) and a parallel bus interface. Five analog inputs are provided and three can be multiplexed to the ADC. The line input, two auxiliary inputs and a mono input can be mixed with the output of the DAC with full volume control. Several data modes are supported including 8- and 16-bit linear as well as 8-bit companded, 4-bit ADPCM compressed, and 16-bit big Endian. The CS4231 is packaged in a 68-pin PLCC or a 100-pin TQFP.

Enhanced Functions (MODE 2)

The CS4231's initial state is labeled MODE 1 and forces the CS4231 to appear as a CS4248. Enhanced functionality is provided by a second mode on the CS4231. To switch from MODE 1 to MODE 2, the MODE2 bit should be set to one in the MODE and ID register (I12). When MODE 2 is selected, the bit IA4 in the Index Address register (R0) will be decoded as a valid index pointer providing 16 additional registers and increased functionality over the CS4248.

To reverse the procedure, clear the MODE2 bit and the CS4231 will resume operation in MODE 1. Since previous code should write a zero to bit IA4 of the Index Address register (R0), the CS4231 is backwards compatible with the CS4248 and the AD1848.

Mixer Attenuation Control on Line Input

The CS4231 adds mixer attenuation control for the LINE inputs which are then summed into the output mixer. This fourth input to the mixer completes the recommended mixer configuration for MPC Level-2 compliance. The LINE mix register provides 32 volume adjustments in 1.5 dB steps. In addition, there is a one bit mute control.

The additional MODE 2 functions are:

1. Full-Duplex DMA support
2. A programmable timer
3. Mono output with mute control
4. Mono input with mixer volume control
5. ADPCM and Big Endian audio data formats
6. Independent selection of capture and playback audio data formats

ANALOG HARDWARE DESCRIPTION

The analog hardware consist of an MPC Level 2-compatible mixer (four stereo mix sources), three line-level stereo inputs, a stereo microphone input, a mono input, a mono output, and a stereo line output. This section describes the analog hardware needed to interface with these pins.

Analog Inputs

The analog inputs consist of four stereo analog inputs, and one mono input. As shown on this data sheet cover, the input to the ADCs comes from a multiplexer that selects between two analog line-level inputs (LINE, AUX1), a microphone level input (MIC), and the output from the MPC-compatible mixer. The LINE and AUX1 lines also feed the MPC mixer and include individual volume controls. Unused analog inputs should be connected together and then connected through a capacitor to analog ground.

Line-Level Inputs plus MPC Mixer

The analog input interface is designed to accommodate four stereo inputs and one mono input.

Three of these sources are multiplexed to the ADC. These inputs are: a stereo line-level input (LINE), a stereo microphone input (MIC), and a stereo auxiliary line-level input (AUX1). The LINE and AUX1 inputs have a separate path, with volume control, to the output analog mixer which has the additional inputs of a stereo AUX2 channel, a mono input channel, and the output of the DACs. All audio inputs should be capacitively coupled to the CS4231.

Since some analog inputs can be as large as 2 V_{RMS}, the circuit shown in Figure 2 can be used to attenuate the analog input to 1 V_{RMS} which is the maximum voltage allowed for the line-level inputs on the CS4231.

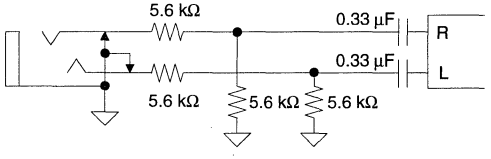


Figure 2. Line Inputs

Microphone Level Inputs

The microphone level inputs, LMIC and RMIC, include a selectable + 20dB gain stage for interfacing to an external microphone. The 20dB gain block can be turned off to provide another stereo line-level input. Figure 3 illustrates a single-ended microphone input buffer circuit that will support lower gain mics.

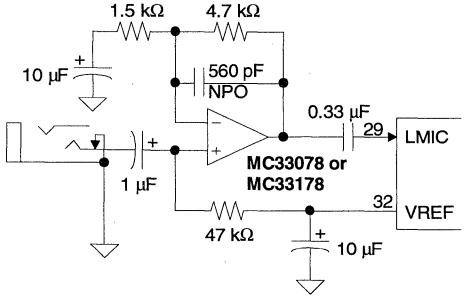


Figure 3. Left or Mono Microphone Input

Mono Input with Attenuation and Mute

The mono input, MIN, is useful for mixing the output of the "beeper" (timer chip), provided in all PCs, with the rest of the audio signals. The attenuation control allows 16 levels in -3dB steps. In addition, a mute control is provided. The attenuator is a single channel block with the resulting signal sent to the output mixer where it is mixed with the left and right outputs. Figure 4 illustrates a typical input circuit for the Mono In. Although this input is described for a low-quality beeper, the input is of the same high-quality as all other analog inputs and may be used for other purposes. At power-up, the MIN line is unmuted (as is the mono out line) allowing the initial beeps heard, when the computer is initializing, to pass through.

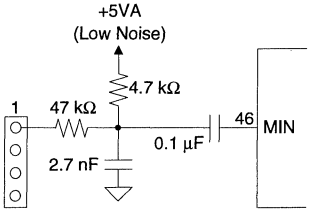


Figure 4. Mono Input

Analog Outputs

The analog output section of the CS4231 provides a stereo line-level output. The other output types (headphone and speaker) can be implemented with external circuitry. LOUT and ROUT outputs should be capacitively coupled to external circuitry. Figure 1 shows the simplicity of the analog output interface.

Mono Output with Mute Control

The mono output, MOUT, is a sum of the left and right output channels, attenuated by 6dB to prevent clipping at full scale. The mono out channel can be used to drive the PC-internal mono speaker using an appropriate drive circuit. This approach allows the traditional PC-sounds

to be integrated with the rest of the audio system. Figure 5 illustrates a typical speaker driver circuit. The mute control is independent of the line outputs allowing the mono channel to mute the speaker without muting the line outputs. The power-up default has MIN and MOUT enabled to provide a pass-through for the beeps heard at power-up.

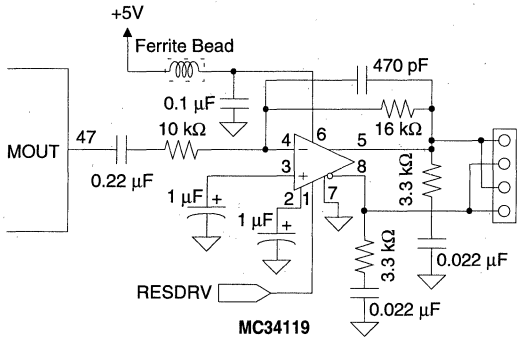


Figure 5. Mono Output

Miscellaneous Analog Signals

The LFILT and RFILT pins must have a 1000 pF NPO capacitor to analog ground. These capacitors, along with an internal resistor, provide a single-pole low-pass filter used at the inputs to the ADCs. By placing these filters at the input to the ADCs, low-pass filters at each analog input pin is avoided.

The VREFI pin is used to lower the noise of the internal voltage reference. A 10µF and 0.1µF capacitor to analog ground should be connected with a short wide trace to this pin. No other connection should be made, as any coupling onto this pin will degrade the analog performance of the codec. Likewise, digital signals should be kept away from VREFI for similar reasons.

The VREF pin is typically 2.1 V and provides a common mode signal for single-supply external circuits. VREF only supports DC loads and should be buffered if AC loading is needed. For typical use, a 0.47 µF capacitor should be connected to VREF. High-gain microphone circuits can be improved by increasing the capacitance to 10 µF.

DIGITAL HARDWARE DESCRIPTION

The digital hardware consist of the data bus, address bus, and control signals needed for the parallel bus, as well as an interrupt and DMA signals.

Parallel Data Interface

The 8-bit parallel port of the CS4231 provides an interface which is compatible with most computer peripheral busses. This parallel interface is designed to operate on the Industry Standard Architecture (ISA) bus, but the CS4231 will easily interface with other buses such as EISA and microchannel. Two types of accesses can occur via the parallel interface: Programmed I/O (PIO) access, and DMA access.

There is no provision for the CS4231 to "hold off" or extend a cycle occurring on the parallel interface. Therefore, the internal architecture of the CS4231 accepts asynchronous parallel bus cycles without interfering with the flow of data to or from the ADC and DAC sections.

FIFOs

The CS4231 contains 16-sample FIFOs in both the playback and capture paths. The FIFOs are transparent and have no programming associated with them.

When playback is enabled, the playback FIFO continually requests data until the FIFO is full, and then makes requests as positions inside the FIFO are emptied, thereby keeping the playback FIFO as full as possible. Thus when the system cannot respond within a sample period, the FIFO

is emptied, avoiding a momentary loss of audio data. If the FIFO runs out of data, the last valid sample can be continuously output to the DACs (if DACZ in I16 is set) which will eliminate pops from occurring.

When capture is enabled, the capture FIFO tries to continually stay empty by making requests every sample period. Thus when the system cannot respond within a sample period, the capture FIFO starts filling thereby avoiding a loss of data in the audio data stream.

High Current Data Bus Drivers

The CS4231 provides 16 mA drivers eliminating the need for off chip drivers in many cases. If a full 24 mA drive is required, the appropriate direction and driver select lines are provided. The current drivers are provided for the data bus, DMA request line, and the interrupt request line.

PIO Registers Interface

The first type of parallel bus access is programmed I/O (PIO) to the four control registers. The control registers allow access to status, audio data, and all indirect registers via the index registers. The $\overline{RD}$ and $\overline{WR}$ signals are used to define the read and write cycles respectively. The PIO register cycle is defined by the assertion of the CS4231 $\overline{CS}$ signal while the DMA acknowledge signals, $\overline{CDAK}$ and $\overline{PDAK}$, are inactive. For read cycles, the CS4231 will drive data on the DATA lines while the host asserts the $\overline{RD}$ strobe. Write cycles require the host to assert data on the DATA lines and strobe the $\overline{WR}$ signal. The CS4231 will latch data into the PIO register on the rising edge of the $\overline{WR}$ strobe. The CS4231 $\overline{CS}$ signal should remain active until after completion of the read or write cycle. I/O cycles are the only type of cycle which can access the internal control and status registers.

The audio data interface typically uses DMA request/grant pins to transfer the digital audio data between the CS4231 and the bus. The CS4231 is responsible for asserting a request signal whenever the CS4231's internal buffers need updating. The logic interfaced with the CS4231 responds with an acknowledge signal and strobes data to and from the CS4231, 8 bits at a time. The CS4231 keeps the request pin active until the appropriate number of 8-bit cycles have occurred to transfer one audio sample. Notice that different audio data types will require a different number of 8-bit transfers.

DMA Interface

The second type of parallel bus cycle on the CS4231 is a DMA transfer. DMA cycles are distinguished from PIO register cycles by the assertion by the CS4231 of a CDRQ (or PDRQ) followed by an acknowledgment by the host by the assertion of $\overline{CDAK}$ (or $\overline{PDAK}$). While the acknowledgment is received from the host, the CS4231 assumes that any cycles occurring are DMA cycles and ignores the addresses on the address lines and the $\overline{CS}$ line.

The CS4231 may assert the DMA request signal at any time. Once asserted, the DMA request will remain asserted until a DMA cycle occurs to the CS4231. Once the falling edge of the final $\overline{WR}$ or $\overline{RD}$ strobe of a full sample of a DMA cycle occurs, the DMA request signal is negated immediately. DMA transfers may be terminated by resetting the PEN and/or CEN bits in the Interface Configuration register (I9), depending on the DMA that is in progress (playback, capture, or both). Termination of DMA transfers may only happen between sample transfers on the bus. If PDRQ and/or CDRQ goes active while resetting PEN and/or CEN, the request must be acknowledged ($\overline{PDAK}$ and/or $\overline{CDAK}$) and a final sample transfer completed. The CS4231 supports up to two DMA channels.

Dual DMA Channel Mode

In dual DMA channel mode, playback and capture DMA requests and acknowledges occur on independent DMA channels. In this mode, capture and playback are enabled and set for DMA transfers. In addition, the dual DMA mode must be set (SDC = 0). The Playback- and Capture-Enables (PEN, CEN, I9) can be changed without a Mode Change Enable (MCE, R0). This allows for proper full duplex control where applications are independently using playback and capture.

Single DMA Channel (SDC) Mode

When two DMA channels are not available, the SDC mode forces all DMA transfers (capture or playback) to occur on a single DMA channel (playback channel). The trade-off is that the CS4231 will no longer be able to perform simultaneous DMA capture and playback.

To enable the SDC mode, set the SDC bit in the Interface Configuration register (I9). With the SDC bit asserted, the internal workings of the CS4231 remain exactly the same as dual mode, except for the manner in which DMA request and acknowledges are handled.

The playback of audio data will occur on the playback channel exactly as dual channel operation. However, the capture audio channel is now diverted to the playback channel. This means that the capture DMA request occurs on the PDRQ pin and the $\overline{\text{PDAK}}$ pin is used to acknowledge the capture request. (In MODE 2, the capture data format is always set in register I28.) Note, simultaneous capture and playback cannot occur in SDC mode. If both playback and capture are enabled, the default will be playback.

In SDC mode, the CDRQ pin is logic low (inactive). The $\overline{\text{CDAK}}$ pin is ignored by the CS4231. SDC does not have any affect when using PIO accesses.

Miscellaneous Signals

The power supply providing analog power should be as clean as possible to minimize coupling into the analog section and degrading analog performance. The VD1 and VD2 pins are isolated from the rest of the digital power pins and provide digital power for the asynchronous parallel bus. These two pins can be connected directly to the digital power supply. VD3 and VD4 digital power supply pins provide power to the internal digital section of the codec and should be optimally quieter than VD1 and VD2. This can be achieved by using a ferrite bead as shown in the typical connection diagram in Figure 1. Grounding is covered in the *Grounding and Layout* section.

An interrupt pin, IRQ, is provided to allow for host notification by the CS4231. Since the interrupt is mainly a software function, it is described in more detail under the software section.

Crystals / Clocks

Four pins have been allocated to allow the interfacing of two crystal oscillators to the CS4231: XTAL1I, XTAL1O, XTAL2I, XTAL2O. The crystals should be designed as fundamental mode, parallel resonant, with a load capacitor of between 10 and 20 pF. The capacitors shown in Figure 1, connected to each of the crystal pins, should be twice the load capacitance specified to the crystal manufacturer. The XTAL1 oscillator is designed with slightly more gain to handle higher frequencies, but any crystal with the above specifications should suffice. The standard crystals for audio are:

XTAL1: 24.576 MHz
Fundamental Mode
Parallel Resonant, C_L = 20 pF

XTAL2: 16.9344 MHz
Fundamental Mode
Parallel Resonant, C_L = 20 pF

These crystal frequencies support the standard sample frequencies listed in Table 7.

External CMOS clocks may be connected the crystal inputs (XTAL1I, XTAL2I) in lieu of the crystals. When using external CMOS clocks, the XTAL out pins should be left floating. Extreme care should be used when laying out a board using external clocks since coupling between clocks can degrade analog performance.

Power Down - $\overline{PDWN}$

The $\overline{PDWN}$ signal places the CS4231 into maximum power conservation mode. When $\overline{PDWN}$ goes low, any reads of the codec's parallel interface return 80 hex, all analog outputs are muted, and the voltage reference then slowly decays to ground. The $\overline{PDWN}$ signal should be held low while power is applied to the codec. Once the power supplies have settled, $\overline{PDWN}$ should be brought high which starts an initialization procedure and causes a full calibration cycle to occur. While the codec is initializing, any reads from the parallel interface will return 80 hex and writes will be ignored. When initialization is completed, the registers will contain their reset value as stated in the register section of the data sheet.

$\overline{DBEN}$/DBDIR

If needed, the $\overline{DBEN}$ and DBDIR pins can control an external data buffer to the CS4231. The CS4231 contains 16 mA bus drivers so the external data buffer is only needed when driving a full 24 mA bus. $\overline{DBEN}$ enables the external drivers and DBDIR controls the direction of the data flow. Both signals are normally high, where DBDIR high points the transceiver towards the codec and low points the transceiver towards the data bus. See Figure 1 for a typical connection diagram.

SOFTWARE DESCRIPTION

The CS4231 must be in Mode Change Enable Mode (MCE=1) before any changes to the Interface Configuration register (I9) or the Data Format registers (I8, I28) are allowed. The exceptions are CEN and PEN which can be changed "on-the-fly" via programmed I/O writes to these bits. All outstanding DMA transfers must be completed before new values of CEN or PEN are recognized.

4

Procedures

Power-Down and Initialization

To put the CS4231 into a power-down mode, the $\overline{PDWN}$ pin is pulled low. In this state the host interface reads 80h indicating that it is unable to respond and all analog circuits are turned off.

To let the CS4231 go through its reset initialization the $\overline{PDWN}$ pin should be set high. This rising edge starts the initialization process in which a full calibration occurs. While the CS4231 is initializing, 80 hex is returned from all reads by the host computer. All writes during initialization of the CS4231 will be ignored. At the end of the initialization, all registers are set to known reset values as documented in the register definition section.

Auto Calibration

The CS4231 has the ability to calibrate the ADCs and DACs. Auto-calibration occurs whenever the CS4231 returns from Mode Change Enable (MCE) AND the ACAL bit in the Interface Configuration register (I9) has been set.

The completion of calibration can be determined by polling the Auto-Calibrate In-Progress bit in the Error Status and Initialization register (ACI, I11). This bit will be high while the calibration is in progress and low once completed. The auto-calibration sequence will take at least 168

sample periods. Transfers enabled during calibrate will not begin until the calibration cycle has completed.

The auto-calibrate procedure is as follows:

1) Place the CS4231 in Mode Change Enable using the MCE bit of the Index Address register (R0).
2) Set the ACAL bit in the Interface Configuration register (I9).
3) Return from Mode Change Enable by resetting the MCE bit of the Index Address register (R0).
4) Wait until 80h NOT returned
5) Wait until ACI (I11) cleared to proceed

Changing Sampling Rate

The internal states of the CS4231 are synchronized by the selected sampling frequency defined in the Data Format registers (I8, I28). The changing of either the clock source or the clock frequency divide requires a special sequence for proper CS4231 operation:

1) Place the CS4231 in Mode Change Enable using the MCE bit of the Index Address register (R0).
2) During a single write cycle, change the Clock Frequency Divide Select (CFS) and/or Clock Source Select (CSL) bits of the Fs & Playback Data Format register (I8) to the desired value. (The data format may also be changed.)
3) The CS4231 resynchronizes its internal states to the new clock. During this time the CS4231 will be unable to respond at its parallel interface. Writes to the CS4231 will not be recognized and reads will always return the value 80 hex.
4) The host now polls the CS4231's Index Address register (R0) until the value 80 hex is no longer returned.
5) Once the CS4231 is no longer responding to reads with a value of 80 hex, normal operation can resume and the CS4231 can be removed from MCE.
The CSL and CFS bits cannot be changed unless the MCE bit has been set. Attempts to change the Data Format registers (I8, I28) or Interface Configuration register (I9, except CEN and PEN) without MCE set, will not be recognized.

Audio Data Formats

In MODE 1 operation, all data formats of the CS4231 are in "little endian" format. This format defines the byte ordering of a multibyte word as having the least significant byte occupying the lowest memory address. Likewise, the most significant byte of a little endian word occupies the highest memory address.

The sample frequency is always selected in the Fs and Playback Data Format register (I8). In MODE 1 the same register, I8, determines the audio data format for both playback and capture; however, in MODE 2, I8 only selects the playback data format and the capture data format is independently selectable in the Capture Data Format register (I28).

The CS4231 always orders the left channel data before the right channel. Note that these definitions apply regardless of the specific format of the data. For example, 8-bit linear data streams look exactly like 8-bit companded data streams. Also, the left sample always comes first in the data stream regardless of whether the sample is 16-bit or 8-bit in size.

There are four data formats supported by the CS4231 during MODE 1 operation: 16-bit signed (little endian), 8-bit unsigned, 8-bit companded μ-Law, and 8-bit companded A-Law. See Figures 6 through 9.

Additional data formats are supported in MODE 2 operation: 4-bit ADPCM, and 16-bit

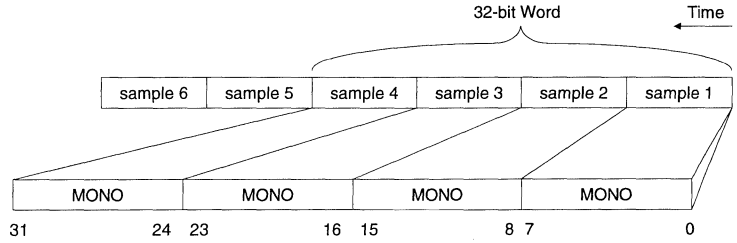


Figure 6. 8-bit Mono, Unsigned Audio Data

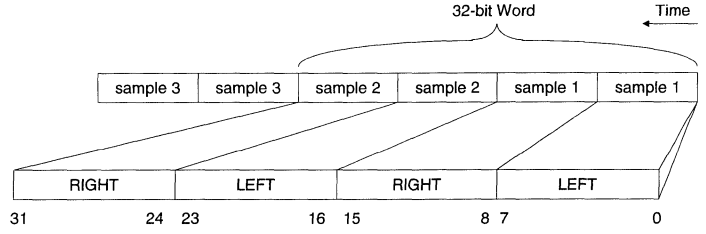


Figure 7. 8-bit Stereo, Unsigned Audio Data

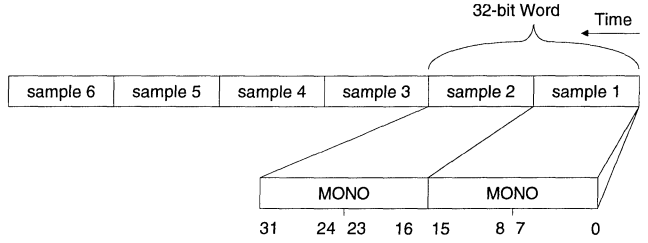


Figure 8. 16-bit Mono, Signed Little Endian Audio Data

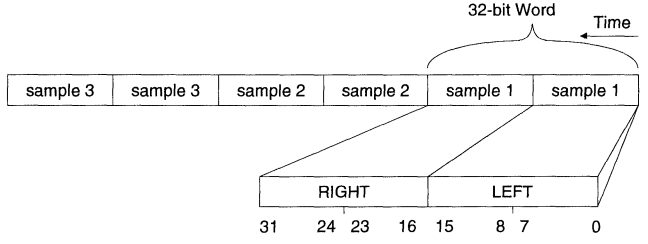


Figure 9. 16-bit Stereo, Signed Little Endian Audio Data

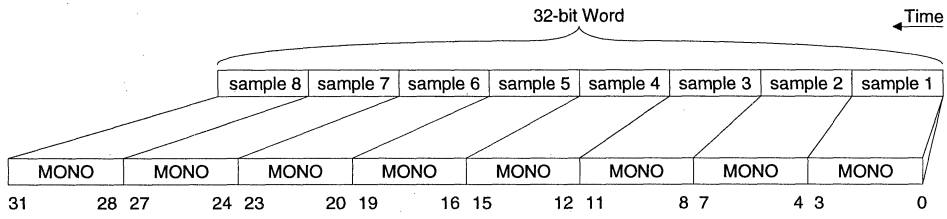


Figure 10. 4-bit Mono, ADPCM Audio Data

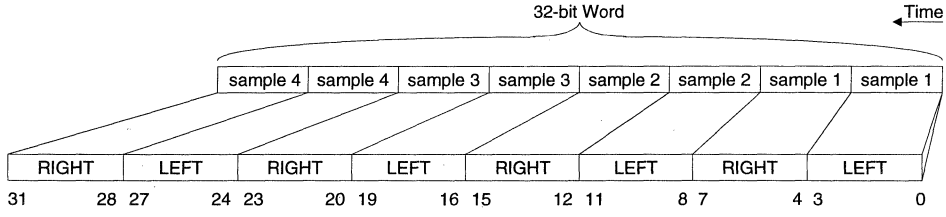


Figure 11. 4-bit Stereo, ADPCM Audio Data

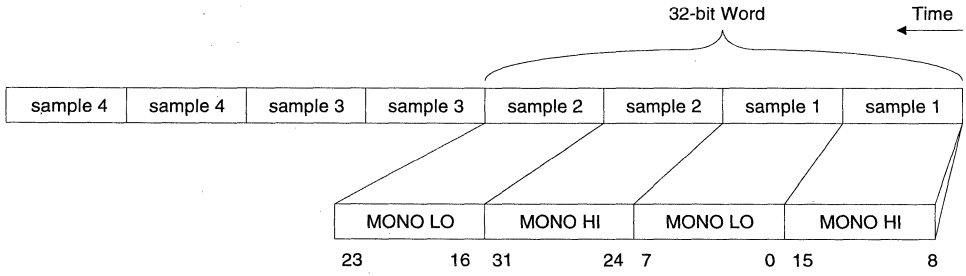


Figure 12. 16-bit Mono, Signed Big Endian Audio Data

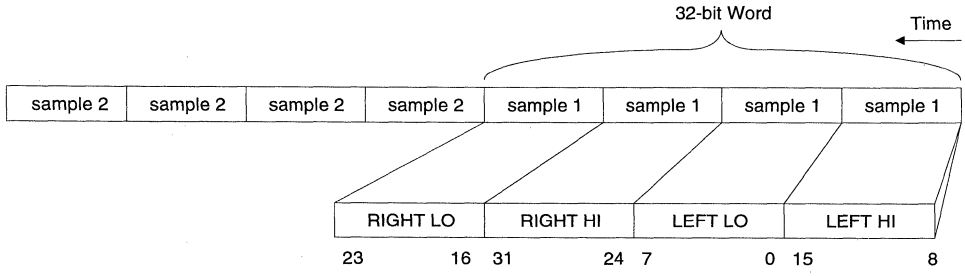


Figure 13. 16-bit Stereo, Signed Big Endian Audio Data

signed big endian. See Figures 10 through 13. With the addition of the big endian and ADPCM audio data formats, the CS4231 is compliant with the IMA recommendations for digital audio data formats (and sample frequencies).

16-bit Signed

The 16-bit signed format (also called 16-bit 2's complement) is the standard method of representing 16-bit digital audio. This format gives 96 dB theoretical dynamic range and is the standard for compact disk audio players. This format uses the value -32768 (8000h) to represent minimum analog amplitude while 32767 (7FFFh) represents maximum analog amplitude.

8-bit Unsigned

The 8-bit unsigned format is commonly used in the personal computer industry. This format delivers a theoretical dynamic range of 48 dB. This format uses the value 0 (00h) to represent minimum analog amplitude while 255 (FFh) represents maximum analog amplitude. The 16-bit signed and 8-bit unsigned transfer functions are shown in Figure 14.

8-bit Companded

The 8-bit companded formats (A-Law and μ-Law) come from the telephone industry. μ-Law is the standard for the United States/Japan while A-Law is used in Europe. Companded audio allows either 64 dB or 72 dB of dynamic range using only 8-bits per sample. This is accomplished using a non-linear companding transfer function which assigns more digitalization codes to lower amplitude analog signals with the sacrifice of precision on higher amplitude signals. The μ-Law and A-Law formats of the CS4231 conform to the CCITT G.711 specifications. Figure 15 illustrates the transfer function for both A- and μ-Law. Please refer to the standards mentioned above for an exact definition.

ADPCM Compression/Decompression

In MODE 2, the CS4231 also contains Adaptive Differential Pulse Code Modulation (ADPCM) for improved performance and compression ratios over μ-Law or A-Law. The ADPCM format is compliant with the IMA standard and provides a 4-to-1 compression ratio (i.e. 4 bits are saved for each 16-bit sample captured). For more information on the specifics of the format, contact the IMA at (202) 408-1000. See Figures 10 and 11.

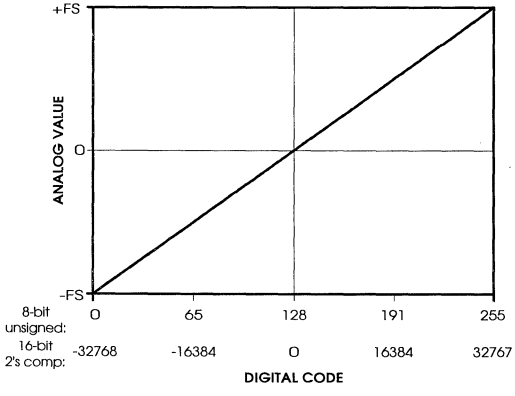


Figure 14. Linear Transfer Functions

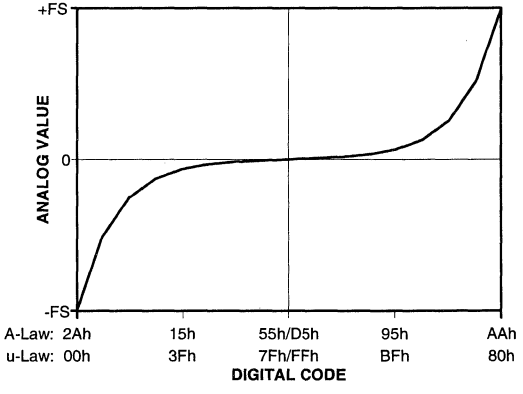


Figure 15. Companded Transfer Functions

When using the ADPCM data format, the DMA Base register count is not on a per sample basis.

DMA Registers

The DMA registers allow easier integration of the CS4231 in ISA systems. Peculiarities of the ISA DMA controller require an external count mechanism to notify the host CPU of a full DMA buffer via interrupt. The programmable DMA Base registers provide this service.

The act of writing a value to the Upper Base register cause both Base registers to load the Current Count register. DMA transfers are enabled by setting the PEN/CEN bit while PPIO/CPIO is clear. (PPIO/CPIO can only be changed while the MCE bit is set.) Once transfers are enabled, each sample that is transferred by a DMA cycle will decrement the Current Count register (with the exception of the ADPCM format) until zero is reached. The next sample after zero generates an interrupt and reloads the Current Count registers with the values in the Base registers.

For all data formats except ADPCM, the DMA Base registers must be loaded with the number of samples, minus one, to be transferred between "DMA Interrupts". Stereo data contains twice as many samples as mono data; however, 8-bit data and 16-bit data contain the same number of samples. Symbolically:

DMA Base register$_{16}$ = N_S - 1

Where N_S is the number of samples transferred between interrupts and the "DMA Base register$_{16}$" consists of the concatenation of the upper and lower DMA Base registers.

For the ADPCM data format, the contents of the DMA Base registers is calculated differently from any other data format. The Base registers must be loaded with the number of BYTES to be transferred between "DMA interrupts", divided by four, minus one. The same number is used whether the data format is stereo or mono ADPCM. Symbolically:

DMA Base register$_{16}$ = N_b/4 - 1

Where N_b is the number of BYTES transferred between interrupts and the "DMA Base register$_{16}$" consists of the concatenation of the upper and lower DMA Base registers.

Playback DMA Registers

The playback DMA registers (I14/15) are used for sending playback data to the DACs in MODE 2. In MODE 1, these registers (I14/15) are used for both playback and capture; therefore, full-duplex DMA operation is not possible.

When the playback Current Count register rolls under, the Playback Interrupt bit, PI, (I24) is set causing the INT bit (R2) to be set. The interrupt is cleared by a write of any value to the Status register (R2), or writing a "0" to the Playback Interrupt bit, PI (I24).

Capture DMA Registers

The Capture DMA Base registers (I30/31) provide a second pair of Base registers that allow full-duplex DMA operation. With full-duplex operation capture and playback can occur simultaneously. These registers are provided in MODE 2 operation only.

When the capture Current Count register rolls under, the Capture Interrupt bit, CI, (I24) is set causing the INT bit (R2) to be set. The interrupt is cleared by a write of any value to the Status register (R2), or writing a "0" to the Capture Interrupt bit, CI (I24).

Digital Loopback

Digital Loopback is enabled via the LBE bit in the Loopback Control register (I13). This loop-

back routes the digital data from the ADCs to the DACs. This loopback can be digitally attenuated via additional bits in the Loopback Control register (I13). Loopback is then summed with DAC data supplied at the digital bus interface. When loopback is enabled, it will "freerun" synchronous with the sample rate. The digital loopback is shown in the CS4231 Block Diagram on the front cover. This loopback can be used to mix the incoming microphone data with data from the DACs. Since the CS4231 allows selection of different data formats between capture and playback, if the capture channel is set to mono and the playback channel set to stereo, the mono input (mic) data will be mixed into both channels of the output mixer.

If the sum of the loopback and bus data are greater than full scale, CS4231 will send the appropriate full scale value to the DACs (clipping).

Timer Registers

The Timer registers are provided for synchronization, watch dog and other functions where a high resolution time reference is required. This counter is 16 bits and the exact time base, listed in the register description, is determined by the crystal selected.

The Timer register is set by loading the high and low registers to the appropriate values and setting the Timer Enable bit, TE, in the Alternate Feature Enable register (I16). This value will be loaded into an internal Current Count register and will decrement at approximately a 10 µsec rate. When the value of the Current Count register reaches zero, an interrupt will be posted to the host and the Timer Interrupt bit, TI, is set in the Alternate Feature Status register (I24). On the next timer clock the value of the Timer registers will be loaded into the internal Current Count register and the process will begin again. The interrupt is cleared by any write to the Status register (R2) or by writing a "0" to the Timer Interrupt bit, TI, in the Alternate Feature Status register (I24).

Interrupts

The INT bit of the Status register (R2) always reflects the status of the CS4231 internal interrupt state. A roll-over from any Current Count register (DMA playback, DMA capture, or Timer) sets the INT bit. This bit remains set until cleared by a write of ANY value to Status register (R2), or by clearing the appropriate bit or bits (PI, CI, TI) in the Alternate Feature Status register (I24). The IRQ pin of the CS4231 may or may not go active on an interrupt event.

The Interrupt Enable (IEN) bit in the Pin Control register (I10) determines whether the interrupt pin responds to the interrupt event in the CS4231. When the IEN bit is low, the interrupt is masked and the IRQ pin of the CS4231 is forced low. However, the INT bit in the Status register (R2) always responds to the counter.

Error Conditions

Data overrun or underrun could occur if data is not supplied to or read from the CS4231 in an appropriate amount of time. The amount of time for such data transfers depends on the frequency selected within the CS4231.

Should an overrun condition occur during data capture, the last whole sample (before the overrun condition) will be read by the DMA interface. A sample will not be overwritten while the DMA interface is in the process of transferring the sample.

Should an underrun condition occur in a playback case the last valid sample will be output (assuming DACZ = 0) to the digital mixer. This will mask short duration error conditions. When the next complete sample arrives from the host computer the data stream will resume on the next sample clock.

CS4231 REGISTER MAPPING

	Addr.	Register Name
R0	0	Index Address register
R1	1	Indexed Data register
R2	2	Status register
R3	3	PIO Data register

Table 1. Direct Registers

The two address pins of the CS4231 allow access to four 8-bit registers. Two of these registers provide indirect accessing to more CS4231 registers via an index register. The other two registers provide status information and allow audio data to be transferred to and from the CS4231 without using DMA cycles or indexing.

Physical Mapping

The PIO registers are I/O mapped via four locations. Two address pins provide access to all of the CS4231's registers. The four direct registers are shown in Table 1. The first two direct registers are used to access 32 indirect registers shown in Table 2. As indicated by the arrows, the Index Address register (R0) points to the indirect register that is accessed through the Indexed Data register (R1).

This section describes all the direct and indirect registers. Table 3 details a summary of each bit in each register with Tables 4 through 10 illustrating the majority of decoding needed when programming the CS4231 and are included for reference. Tables 4 through 8 indicate gain settings at internal nodes. If OLB= 1 then the output will reflect the gain setting. If OLB= 0, the output will be attenuated by 3 dB as indicated in the specifications. The CS4231 powers up into the reset state which is defined as MODE 1. MODE 1 is backwards compatible with the CS4248 and only allows access to the first 16 indirect registers. Setting the MODE2 bit in the MODE and ID register (I12) enables

Index	Register Name
I0	Left ADC Input Control
I1	Right ADC Input Control
I2	Left Aux #1 Input Control
I3	Right Aux #1 Input Control
I4	Left Aux #2 Input Control
I5	Right Aux #2 Input Control
I6	Left DAC Output Control
I7	Right DAC Output Control
I8	Fs & Playback Data Format
I9	Interface Configuration
I10	Pin Control
I11	Error Status and Initialization
I12	MODE and ID (MODE2 bit)
I13	Loopback Control
I14	Playback Upper Base Count
I15	Playback Lower Base Count
I16	Alternate Feature Enable I
I17	Alternate Feature Enable II
I18	Left Line Input Control
I19	Right Line Input Control
I20	Timer Low Byte
I21	Timer High Byte
I22	RESERVED
I23	RESERVED
I24	Alternate Feature Status
I25	Version / Chip ID
I26	Mono Input & Output Control
I27	RESERVED
I28	Capture Data Format
I29	RESERVED
I30	Capture Upper Base Count
I31	Capture Lower Base Count

Table 2. Indirect Registers

MODE 2 which allows access to indirect registers 16 through 31 and enables all the features of the CS4231.

Index Address Register (R0)

D7	D6	D5	D4	D3	D2	D1	D0
INIT	MCE	TRD	IA4	IA3	IA2	IA1	IA0

IA3-IA0 — Index Address: These bits define the address of the CS4231 register accessed by the Indexed Data register (R1). These bits are read/write.

IA4 — Allows access to indirect registers 16 - 31. Only available in MODE 2. In MODE 1,this bit is reserved.

MCE — Mode Change Enable: This bit must be set whenever the current mode of the CS4231 is changed. The Data Format (I8, I28) and Interface Configuration (I9) registers CANNOT be changed unless this bit is set. The exceptions are CEN and PEN which can be changed "on-the-fly". The DAC output is muted when MCE is set.

TRD — Transfer Request Disable: This bit, when set, causes DMA transfers to cease when the INT bit of the status register is set. Independent for playback and capture interrupts.

0 - Transfers Enabled (PDRQ and CDRQ occur uninhibited)
1 - Transfers Disabled (PDRQ and CDRQ only occur if INT bit is 0)

INIT — CS4231 Initialization: This bit is read as 1 when the CS4231 is in a state in which it cannot respond to parallel interface cycles. This bit is read-only.

Immediately after RESET (and once the CS4231 has left the INIT state), the state of this register is: 010x0000

During initialization and power down, this register CANNOT be written and always reads 10000000 (80h)

Indexed Data Register (R1)

D7	D6	D5	D4	D3	D2	D1	D0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

ID7-ID0 — Indexed Data register: These bits are the indirect register referenced by the Indexed Address register (R0).

During initialization and power down, this register can NOT be written and is always read 10000000 (80h)

4

I/O Data Registers

The PIO Data register is two registers mapped to the same address. Writes to this register sends data to the Playback Data register. Reads from this register will receive data from the Capture Data register.

During initialization and power down, this register CANNOT be written and is always read 10000000 (80h)

Capture I/O Data Register (R3, Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0

CD7-CD0 — Capture Data Port. This is the control register where capture data is read during programmed I/O data transfers.

The reading of this register will increment the state machine so that the following read will be from the next appropriate byte in the sample. The exact byte which is next to be read can be determined by reading the Status register (R2). Once all relevant bytes have been read, the state machine will point to the last byte of the sample until a new sample is received from the ADCs. Once this has occurred, and a read of the status has occurred, the state machine and Status register (R2) will point to the first byte of the new sample.

Direct Registers: (R0-R3)

	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	INIT	MCE	TRD	IA4†	IA3	IA2	IA1	IA0
R1	0	1	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R2	1	0	CU/$\overline{L}$	CL/$\overline{R}$	CRDY	SER	PU/$\overline{L}$	PL/$\overline{R}$	PRDY	INT
R3	1	1	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
R3	1	1	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Indirect Registers: (I0-I31)

IA4-IA0	D7	D6	D5	D4	D3	D2	D1	D0
0	LSS1	LSS0	LMGE	-	LAG3	LAG2	LAG1	LAG0
1	RSS1	RSS0	RMGE	-	RAG3	RAG2	RAG1	RAG0
2	LX1M	-	-	LX1G4	LX1G3	LX1G2	LX1G1	LX1G0
3	RX1M	-	-	RX1G4	RX1G3	RX1G2	RX1G1	RX1G0
4	LX2M	-	-	LX2G4	LX2G3	LX2G2	LX2G1	LX2G0
5	RX2M	-	-	RX2G4	RX2G3	RX2G2	RX2G1	RX2G0
6	LDM	-	LDA5	LDA4	LDA3	LDA2	LDA1	LDA0
7	RDM	-	RDA5	RDA4	RDA3	RDA2	RDA1	RDA0
8 §	FMT1†	FMT0	C/$\overline{L}$	S/$\overline{M}$	CSF2	CSF1	CSF0	C2SL
9 §	CPIO	PPIO	-	-	ACAL	SDC	CEN	PEN
10	XCTL1	XCTL0	-	-	DEN	-	IEN	-
11	COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0
12	1	MODE2	-	-	ID3	ID2	ID1	ID0
13	LBA5	LBA4	LBA3	LBA2	LBA1	LBA0	-	LBE
14 *	PUB7	PUB6	PUB5	PUB4	PUB3	PUB2	PUB1	PUB0
15 *	PLB7	PLB6	PLB5	PLB4	PLB3	PLB2	PLB1	PLB0
16	OLB	TE	-	-	-	-	-	DACZ
17	-	-	-	-	-	-	-	HPF
18	LLM	-	-	LLG4	LLG3	LLG2	LLG1	LLG0
19	RLM	-	-	RLG4	RLG3	RLG2	RLG1	RLG0
20	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0
21	TU7	TU6	TU5	TU4	TU3	TU2	TU1	TU0
22	-	-	-	-	-	-	-	-
23	-	-	-	-	-	-	-	-
24	-	TI	CI	PI	CU	CO	PO	PU
25	V2	V1	V0	-	-	CID2	CID1	CID0
26	MIM	MOM	-	-	MIA3	MIA2	MIA1	MIA0
27	-	-	-	-	-	-	-	-
28 §	FMT1	FMT0	C/$\overline{L}$	S/$\overline{M}$	-	-	-	-
29	-	-	-	-	-	-	-	-
30	CUB7	CUB6	CUB5	CUB4	CUB3	CUB2	CUB1	CUB0
31	CLB7	CLB6	CLB5	CLB4	CLB3	CLB2	CLB1	CLB0

† IA4 and FMT2 bits are only available in MODE 2 (IA = 12, bit 6 = 1)
Since IA4 is only available in MODE 2, registers 16-31 are only available in MODE 2

* When in MODE 1, the playback base registers (upper and lower) are used for both playback and capture.

§ MCE must be set before changing any bits in these registers (except CEN and PEN).

Table 3. Register Bit Summary

NOTE: Output level relative to input level assuming OLB=1.

	AG3	AG2	AG1	AG0	Level
0	0	0	0	0	0.0 dB
1	0	0	0	1	1.5 dB
2	0	0	1	0	3.0 dB
3	0	0	1	1	4.5 dB
.			.		.
.			.		.
.			.		.
12	1	1	0	0	18.0 dB
13	1	1	0	1	19.5 dB
14	1	1	1	0	21.0 dB
15	1	1	1	1	22.5 dB

Table 4. ADC Input Gain

	A5	A4	A3	A2	A1	A0	Level
0	0	0	0	0	0	0	0.0 dB
1	0	0	0	0	0	1	-1.5 dB
2	0	0	0	0	1	0	-3.0 dB
3	0	0	0	0	1	1	-4.5 dB
.				.			.
.				.			.
.				.			.
60	1	1	1	1	0	0	-90.0 dB
61	1	1	1	1	0	1	-91.5 dB
62	1	1	1	1	1	0	-93.0 dB
63	1	1	1	1	1	1	-94.5 dB

Table 6. DAC & Loopback Attenuation

	MIA3	MIA2	MIA1	MIA0	Level
0	0	0	0	0	0.0 dB
1	0	0	0	1	-3.0 dB
2	0	0	1	0	-6.0 dB
3	0	0	1	1	-9.0 dB
.			.		.
.			.		.
.			.		.
12	1	1	0	0	-36.0 dB
13	1	1	0	1	-39.0 dB
14	1	1	1	0	-42.0 dB
15	1	1	1	1	-45.0 dB

Table 7. Mono Mixer Attenuation

	SS1	SS0	ADC Input Multiplexer
0	0	0	Line
1	0	1	Auxiliary 1
2	1	0	Microphone
3	1	1	Line Output Loopback

Table 9. ADC Input Selector

	G4	G3	G2	G1	G0	Level
0	0	0	0	0	0	12.0 dB
1	0	0	0	0	1	10.5 dB
2	0	0	0	1	0	9.0 dB
3	0	0	0	1	1	7.5 dB
4	0	0	1	0	0	6.0 dB
5	0	0	1	0	1	4.5 dB
6	0	0	1	1	0	3.0 dB
7	0	0	1	1	1	1.5 dB
8	**0**	**1**	**0**	**0**	**0**	**0.0 dB**
9	0	1	0	0	1	-1.5 dB
10	0	1	0	1	0	-3.0 dB
11	0	1	0	1	1	-4.5 dB
12	0	1	1	0	0	-6.0 dB
.			.			.
.			.			.
.			.			.
24	1	1	0	0	0	-24.0 dB
25	1	1	0	0	1	-25.5 dB
26	1	1	0	1	0	-27.0 dB
27	1	1	0	1	1	-28.5 dB
28	1	1	1	0	0	-30.0 dB
29	1	1	1	0	1	-31.5 dB
30	1	1	1	1	0	-33.0 dB
31	1	1	1	1	1	-34.5 dB

Table 5. AUX1 & AUX2 & LINE Mixer Gain

	CFS2	CFS1	CFS0	XTAL1 24.576 MHz	XTAL2 16.9344MHz
0	0	0	0	8.0 kHz	5.51 kHz
1	0	0	1	16.0 kHz	11.025 kHz
2	0	1	0	27.42 kHz	18.9 kHz
3	0	1	1	32.0 kHz	22.05 kHz
4	1	0	0	N/A	37.8 kHz
5	1	0	1	N/A	44.1 kHz
6	1	1	0	48.0 kHz	33.075 kHz
7	1	1	1	9.6 kHz	6.62 kHz

Table 8. Sample Frequency Select

	FMT1	FMT0	C/$\overline{L}$	Audio Data Format
0	0	0	0	Linear, 8-bit unsigned
1	0	0	1	μ-Law, 8-bit
2	0	1	0	Linear, 16-bit, 2's C, LEnd.
3	0	1	1	A-Law, 8-bit
5	1	0	1	ADPCM, 4-bit IMA
6	1	1	0	Linear, 16-bit, 2'sC, BEnd.

Table 10. Audio Data Format

During initialization and power down, this register can NOT be written and is always read 10000000 (80h)

Playback I/O Data Register (R3, Write Only)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

PD7-PD0 Playback Data Port. This is the control register where playback data is written during programmed IO data transfers.

Writing data to this register will increment the playback byte tracking state machine so that the following write will be to the correct byte of the sample. Once all bytes of a sample have been written, subsequent byte writes to this port are ignored. The state machine is reset when the current sample is sent to the DACs.

Status Register (R2, Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
CU/L	CL/R	CRDY	SER	PU/L	PL/R	PRDY	INT

INT Interrupt Status: This indicates the status of the internal interrupt logic of the CS4231. This bit is cleared by any write of any value to this register. The IEN bit of the Pin Control register (I10) determines whether the state of this bit is reflected on the IRQ pin of the CS4231.
Read States

0 - Interrupt inactive
1 - Interrupt active

PRDY Playback Data Ready. The Playback Data register (R3) is ready for more data. This bit would be used when direct programmed I/O data transfers are desired.

0 - Data still valid. Do not overwrite.
1 - Data stale. Ready for next host data write value.

PL/$\overline{R}$ Playback Left/Right Sample: This bit indicates whether data needed is for the Left channel or Right channel.

0 - Right Channel Data
1 - Left Channel or Mono Data

PU/$\overline{L}$ Playback Upper/Lower Byte: This bit indicates whether the playback data needed is for the upper or lower byte of the channel.

0 - Lower Byte needed
1 - Upper Byte needed or any 8-bit mode

SER Sample Error: This bit indicates that a sample was not serviced in time and an error has occurred. The bit indicates an overrun for capture and underrun for playback. If both the capture and playback are enabled, the source which set this bit can not be determined. However, the Alternate Feature Status register (I24) can indicate the exact source of the error.

CRDY Capture Data Ready. The Capture Data register (R3) contains data ready for reading by the host. This bit would be used for direct programmed I/O data transfers.

0 - Data is stale. Do not reread the information.
1 - Data is fresh. Ready for next host data read.

CL/$\overline{R}$ Capture Left/Right Sample: This bit indicates whether the capture data waiting is for the Left channel or Right channel.

0 - Right Channel Data
1 - Left Channel or Mono Data

CU/$\overline{L}$ Capture Upper/Lower Byte: This bit indicates whether the capture data ready is for the upper or lower byte of the channel.

0 - Lower byte ready
1 - Upper byte or any 8-bit ready

Note on PRDY/CRDY: These two bits are designed to be read as one when action is required by the host. For example, when PRDY is set to one, the device is ready for more data; or when the CRDY is set to one, data is available to the host. The definition of the CRDY and PRDY bits are therefore consistent in this regard.

Indirect Mapped Registers

These registers are accessed by placing the appropriate index in the Index Address register (R0) and then accessing the Indexed Data register (R1). A detailed description of each indirect register is given below. All reserved bits should be written zero and may be 0 or 1 when read. Note that indirect registers 16-31 are only available when the MODE2 bit in MODE and ID register (I12) is set.

Left ADC Input Control (I0)

D7	D6	D5	D4	D3	D2	D1	D0
LSS1	LSS0	LMGE	res	LAG3	LAG2	LAG1	LAG0

LAG3-LAG0 Left ADC Gain. The least significant bit represents +1.5 dB, with 0000 = 0 dB. See Table 4.

LMGE Left Mic Gain Enable: This bit enables the 20 dB gain stage of the left mic input signal, LMIC.

LSS1-LSS0 Left ADC Input Source Select. These bits select the input source for the left ADC channel.

0 - Left Line: LLINE
1 - Left Auxiliary 1: LAUX1
2 - Left Microphone: LMIC
3 - Left Line Output Loopback

This register's initial state after reset is: 000x0000

Right ADC Input Control (I1)

D7	D6	D5	D4	D3	D2	D1	D0
RSS1	RSS0	RMGE	res	RAG3	RAG2	RAG1	RAG0

RAG3-RAG0 Right ADC Gain. The least significant bit represents +1.5 dB, with 0000 = 0 dB. See Table 4.

RMGE Right Mic Gain Enable: This bit enables the 20 dB gain stage of the right mic input signal, RMIC.

RSS1-RSS0 Right ADC Input Select. These bits select the input source for the right ADC channel.

0 - Right Line: RLINE
1 - Right Auxiliary 1: RAUX1
2 - Right Microphone: RMIC
3 - Right Line Out Loopback

This register's initial state after reset is: 000x0000

Left Auxiliary #1 Input Control (I2)

D7	D6	D5	D4	D3	D2	D1	D0
LX1M	res	res	LX1G4	LX1G3	LX1G2	LX1G1	LX1G0

LX1G4-LX1G0 Left Auxiliary #1, LAUX1, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 5.

LX1M Left Auxiliary #1 Mute. When set to 1, the left Auxiliary #1 input, LAUX1, to the mixer, is muted.

This register's initial state after reset is: 1xx01000.

Right Auxiliary #1 Input Control (I3)

D7	D6	D5	D4	D3	D2	D1	D0
RX1M	res	res	RX1G4	RX1G3	RX1G2	RX1G1	RX1G0

RX1G4-RX1G0 Right Auxiliary #1, RAUX1, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 5.

RX1M Right Auxiliary #1 Mute. When set to 1, the right Auxiliary #1 input, RAUX1, to the mixer, is muted.

This register's initial state after reset is: 1xx01000.

Left Auxiliary #2 Input Control (I4)

D7	D6	D5	D4	D3	D2	D1	D0
LX2M	res	res	LX2G4	LX2G3	LX2G2	LX2G1	LX2G0

LX2G4-LX2G0 Left Auxiliary #2, LAUX2, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 5.

LX2M Left Auxiliary #2 Mute. When set to 1, the left Auxiliary #2 input, LAUX2, to the mixer, is muted.

This register's initial state after reset is: 1xx01000.

Right Auxiliary #2 Input Control (I5)

D7	D6	D5	D4	D3	D2	D1	D0
RX2M	res	res	RX2G4	RX2G3	RX2G2	RX2G1	RX2G0

RX2G4-RX2G0 Right Auxiliary #2, RAUX2, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 5.

RX2M Right Auxiliary #2 Mute. When set to 1, the right Auxiliary #2 input, RAUX2, to the mixer, is muted.

This register's initial state after reset is: 1xx01000.

Left DAC Output Control (I6)

D7	D6	D5	D4	D3	D2	D1	D0
LDM	res	LDA5	LDA4	LDA3	LDA2	LDA1	LDA0

LDA5-LDA0 Left DAC Attenuator. The least significant bit represents -1.5 dB, with 000000 = 0 dB. See Table 6.

LDM Left DAC Mute. When set to 1, the left DAC output to the mixer will be muted.

This register's initial state after reset is: 1x000000.

Right DAC Output Control (I7)

D7	D6	D5	D4	D3	D2	D1	D0
RDM	res	RDA5	RDA4	RDA3	RDA2	RDA1	RDA0

RDA5-RDA0 Right DAC Attenuator. The least significant bit represents -1.5 dB, with 000000 = 0 dB. See Table 6.

RDM Right DAC Mute. When set to 1, the right DAC output to the mixer will be muted.

This register's initial state after reset is: 1x000000.

Fs and Playback Data Format (I8)

D7	D6	D5	D4	D3	D2	D1	D0
FMT1	FMT0	C/$\overline{L}$	S/$\overline{M}$	CSF2	CFS1	CFS0	C2SL

C2SL Clock 2 Source Select: This bit selects the clock source used for the audio sample rates for both capture and playback.
CAUTION: See note below about changing these bits

0 - XTAL1 Typically 24.576 MHz
1 - XTAL2 Typically 16.9344 MHz

CFS2-CFS0 Clock Frequency Divide Select: These bits select the audio sample frequency for both capture and playback. The actual audio sample frequency depends on which clock source (C2SL) is selected and its frequency. Frequencies listed as N/A are not available because their sample frequency violates the maximum specifications; however, the decodes are available and may be used with crystals that do not violate the sample frequency specifications.
CAUTION: See note below about changing bits

Divide	XTAL1 24.576 MHz	XTAL2 16.9344 MHz
0 - 3072	8.0 kHz	5.51 kHz
1 - 1536	16.0 kHz	11.025 kHz
2 - 896	27.42 kHz	18.9 kHz
3 - 768	32.0 kHz	22.05 kHz
4 - 448	N/A	37.8 kHz
5 - 384	N/A	44.1 kHz
6 - 512	48.0 kHz	33.075 kHz
7 - 2560	9.6 kHz	6.62 kHz

S/$\overline{M}$ Stereo/Mono Select: This bit determines how the audio data streams are formatted. Selecting stereo will result in alternating samples representing left and right audio channels. Mono playback plays the same audio sample on both channels. Mono capture only captures data from the left channel. In MODE 1, this bit is used for both playback and capture. In MODE 2, this bit is only used for playback, and the capture format is independently selected via I28.

0 - Mono
1 - Stereo

The C/$\overline{L}$, FMT1, and FMT0 bits set the audio data format as shown below. In MODE 1, FMT1, which is forced low, FMT0, and C/$\overline{L}$ are used for both playback and capture. In MODE 2, these bits are only used for playback, and the capture format is independently selected via register I28.

FMT1† D7	FMT0 D6	C/$\overline{L}$ D5	
0	0	0	Linear, 8-bit unsigned
0	0	1	μ-Law, 8-bit companded
0	1	0	Linear, 16-bit two's complement, Little Endian
0	1	1	A-Law, 8-bit companded
1	0	0	RESERVED
1	0	1	ADPCM, 4-bit, IMA compatible
1	1	0	Linear, 16-bit two's complement, Big Endian
1	1	1	RESERVED

† FMT1 is not available in MODE 1 (forced to 0).

This register's initial state after reset is: 0000000.

Interface Configuration (I9)

D7	D6	D5	D4	D3	D2	D1	D0
CPIO	PPIO	res	res	ACAL	SDC	CEN	PEN

PEN Playback Enable. This bit enables playback. The CS4231 will generate PDRQ and respond to PDAK signals when this bit is enabled and PPIO=0. If PPIO=1, PEN enables PIO playback mode. PEN may be set and reset without setting the MCE bit.

0 - Playback Disabled (PDRQ and PIO inactive)
1 - Playback Enabled

CEN Capture Enabled. This bit enables the capture of data. The CS4231 will generate CDRQ and respond to CDAK signals when CEN is enabled and CPIO=0. If CPIO=1, CEN enables PIO capture mode. CEN may be set and reset without setting the MCE bit.

0 - Capture disabled (CDRQ and PIO inactive)
1 - Capture enabled

SDC Single DMA Channel: This bit will force BOTH capture and playback DMA requests to occur on the Playback DMA channel. The Capture DMA CDRQ pin will be zero. This bit forces the CS4231 to use one DMA channel. Should both capture and playback be enabled in this mode, only the playback will occur. See the DMA section for further explanation.

0 - Dual DMA channel mode
1 - Single DMA channel mode

ACAL — Auto-Calibrate Enable: This bit determines whether the CS4231 performs a calibration whenever the Mode Change Enable (MCE) bit changes from 1 to 0. If the ACAL bit is not set, previous calibration values are used, and no calibration takes place.

0 - No auto calibration
1 - Auto calibration enabled

PPIO — Playback PIO Enable: This bit determines whether the playback data is transferred via DMA or PIO.

0 - DMA transfers
1 - PIO transfers

CPIO — Capture PIO Enable: This bit determines whether the capture data is transferred via DMA or PIO.

0 - DMA transfers
1 - PIO transfers

Note: This register, except bits CEN and PEN, can only be written while in Mode Change Enable. See section on MCE for more details.

This register's initial state after reset is: 00xx1000

Pin Control (I10)

D7	D6	D5	D4	D3	D2	D1	D0
XCTL1	XCTL0	res	res	DEN	res	IEN	res

IEN — Interrupt Enable: This bit enables the interrupt pin. The Interrupt pin will reflect the value of the INT bit of the Status register (R2). The interrupt pin is active high.

0 - Interrupt disabled
1 - Interrupt enabled

DEN — Dither Enable: When set, triangular pdf dither is added before truncating the ADC 16-bit value to 8-bit, unsigned data. Dither is only active in the 8-bit unsigned mode.

0 - Dither enabled
1 - Dither disabled

XCTL1-XCTL0 — XCTL Control: These bits are reflected on the XCTL1,0 pins of the CS4231.

0 - TTL logic low on XCTL1,0 pins
1 - TTL logic high on XCTL1,0 pins

This registers initial state after reset is: 00xx0x0x

Error Status and Initialization (I11, Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0

ORL1-ORL0 — Overrange Left Detect: These bits determine the overrange on the left ADC channel. These bits are updated on a sample by sample basis.

0 - Less than -1.5 dB
1 - Between -1.5 dB and 0 dB
2 - Between 0 dB and 1.5 dB overrange
3 - Greater than 1.5 dB overrange

ORR1-ORR0 — Overrange Right Detect: These bits determine the overrange on the Right ADC channel.

0 - Less than -1.5 dB
1 - Between -1.5 dB and 0 dB
2 - Between 0 dB and 1.5 dB overrange
3 - Greater than 1.5 dB overrange

DRS — DRQ Status: This bit indicates the current status of the PDRQ and CDRQ pins of the CS4231.

0 - CDRQ AND PDRQ are presently inactive
1 - CDRQ OR PDRQ are presently active

ACI — Auto-calibrate In-Progress: This bit indicates the state of calibration.

0 - Calibration not in progress
1 - Calibration is in progress

PUR — Playback underrun: This bit is set when playback data has not arrived from the host in time to be played. As a result, if DACZ = 0, the last valid sample will be sent to the DACs. This bit is set when an error occurs and will not clear until the Status register (R2) is read.

COR — Capture overrun: This bit is set when the capture data has not been read by the host before the next sample arrives. The old sample will not be overwritten and the new sample will be ignored. This bit is set when an error condition occurs and will not clear until the Status register(R2) is read.

The SER bit in the Status register (R2) is simply a logical OR of the COR and PUR bits. This enables a polling host CPU to detect an error condition while checking other status bits.

This register's initial state after reset is: 00000000

MODE and ID (I12)

D7	D6	D5	D4	D3	D2	D1	D0
1	MODE2	res	res	ID3	ID2	ID1	ID0

ID3-ID0 — Codec ID: These four bits indicate the ID and initial revisions of the codec. Further revisions are expanded in indirect register 25. These bits are read only.

0001 - Revision "B". See Appendix
1010 - Revision "C" on. See register 25 and the Appendix.

MODE2 — MODE 2: Enables the expanded mode of the CS4231. Must be set to enable access to indirect registers 16-31 and their associated features.

0 - MODE 1: CS4248 "look-alike".
1 - MODE 2: Expanded features.

This register's initial state after reset is: 10xx1010

Loopback Control (I13)

D7	D6	D5	D4	D3	D2	D1	D0
LBA5	LBA4	LBA3	LBA2	LBA1	LBA0	res	LBE

LBE — Loopback Enable: When set to 1, the ADC data is digitally mixed with data sent to the DACs.

0 - Loopback disabled
1 - Loopback enabled

LBA5-LBA0 — Loopback Attenuation: These bits determine the attenuation of the loopback from ADC to DAC. The least significant bit represents -1.5 dB, with 000000 = 0 dB. See Table 6.

This register's initial state after reset is: 000000x0

Playback Upper Base (I14)

D7	D6	D5	D4	D3	D2	D1	D0
PUB7	PUB6	PUB5	PUB4	PUB3	PUB2	PUB1	PUB0

PUB7-PUB0 — Playback Upper Base: This register is the upper byte which represents the 8 most significant bits of the 16-bit Playback Base register. Reads from this register return the same value which was written. The Current Count registers cannot be read. When set for MODE 1 or SDC, this register is used for both the Playback and Capture Base registers.

This register's initial state after reset is: 0000000

Playback Lower Base (I15)

D7	D6	D5	D4	D3	D2	D1	D0
PLB7	PLB6	PLB5	PLB4	PLB3	PLB2	PLB1	PLB0

PLB7-PLB0 — Lower Base Bits: This register is the lower byte which represents the 8 least significant bits of the 16-bit Playback Base register. Reads from this register return the same value which was written. When set for MODE 1 or SDC, this register is used for both the Playback and Capture Base registers.

This register's initial state after reset is: 00000000

Alternate Feature Enable I (I16)

D7	D6	D5	D4	D3	D2	D1	D0
OLB	TE	res	res	res	res	res	DACZ

DACZ — DAC Zero: This bit will force the output of the playback channel to AC zero when an underrun error occurs

1 - Go to center scale
0 - Hold previous valid sample

TE — Timer Enable: This bit, when set, will enable the timer to run and interrupt the host at the specified frequency in the timer registers.

OLB — Output Level Bit: Sets the analog output level. When clear, analog line outputs are attenuated 3dB.

0 - Full scale of 2 Vpp (-3 dB)
1 - Full scale of 2.8 Vpp (0 dB)

This register's initial state after reset is: 00xxxxx0

Alternate Feature Enable II (I17)

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	HPF

HPF — High Pass Filter: This bit enables a DC-blocking high-pass filter in the digital filter of the ADC. This filter forces the ADC offset of 0.

0 - disabled
1 - enabled

This register's initial state after reset is: xxxxxxx0.

Left Line Input Control (I18)

D7	D6	D5	D4	D3	D2	D1	D0
LLM	res	res	LLG4	LLG3	LLG2	LLG1	LLG0

LLG4-LLG0 — Left Line, LLINE, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 5.

LLM — Left Line Mute. When set to 1, the left Line input, LLINE, to the mixer, is muted.

This register's initial state after reset is: 1xx01000.

Right Line Input Control (I19)

D7	D6	D5	D4	D3	D2	D1	D0
RLM	res	res	RLG4	RLG3	RLG2	RLG1	RLG0

RLG4-RLG0 — Right Line, RLINE, Mix Gain. The least significant bit represents 1.5 dB, with 01000 = 0 dB. See Table 5.

RLM — Right Line Mute. When set to 1, the Right Line input, RLINE, to the mixer, is muted.

This register's initial state after reset is: 1xx01000.

Timer Lower Byte (I20)

D7	D6	D5	D4	D3	D2	D1	D0
TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0

TL7-TL0 — Lower Timer Bits: This is the low order byte of the 16-bit timer.

This register's initial state after reset is: 00000000.

Timer Upper Byte (I21)

D7	D6	D5	D4	D3	D2	D1	D0
TU7	TU6	TU5	TU4	TU3	TU2	TU1	TU0

TU7-TU0 — Upper Timer Bits: This is the high order byte of the 16-bit timer. The time base is determined by the clock source selected.

C2SL = 0 - divide XTAL1 by 245 (24.576 MHz - 9.969 µs)

C2SL = 1 - divide XTAL2 by 168 (16.9344 MHz - 9.92 µs)

This register's initial state after reset is: 00000000

RESERVED (I22)

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

This register's initial state after reset is: xxxxxxxx

RESERVED (I23)

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

This register's initial state after reset is: xxxxxxxx

Alternate Feature Status (I24)

D7	D6	D5	D4	D3	D2	D1	D0
res	TI	CI	PI	CU	CO	PO	PU

PU — Playback Underrun: This bit, when set, indicates that the DAC has run out of data and a sample has been missed.

PO — Playback Overrun: This bit, when set, indicates that the host attempted to write data into a full FIFO and the data was discarded.

CO — Capture Overrun: This bit, when set, indicates that the ADC had a sample to load into the FIFO but the FIFO was full. In this case the bit is set and the new sample is discarded.

CU — Capture Underrun: This bit indicates that the host has read more data out of the FIFO than it contained. In this condition, the bit is set and the last valid byte is read by the host.

PI — Playback Interrupt: This bit indicates that an interrupt is pending from the playback DMA count registers.

CI — Capture Interrupt: This bit indicates that an interrupt is pending from the record DMA count registers.

TI — Timer Interrupt: This bit indicates that an interrupt is pending from the timer count registers

The PI, CI, and TI bits are reset by writing a "0" to the particular interrupt bit or by writing any value to the Status register (R2).

This register's initial state after reset is: x0000000

Version / ID (I25)

D7	D6	D5	D4	D3	D2	D1	D0
V2	V1	V0	res	res	CID2	CID1	CID0

V2-V0 — Version number. As enhancements are made to the CS4231, the version number is changed so software can distinguish between the different versions.

100 - Revision C, D, & E. This Data Sheet

CID2-CID0 — Chip Identification. Distinguishes between this chip and future chips that support this register set.

000 - CS4231

This register's initial state after reset is: 000xx000

Mono Input & Output Control (I26)

D7	D6	D5	D4	D3	D2	D1	D0
MIM	MOM	res	res	MIA3	MIA2	MIA1	MIA0

MIA3-MIA0 — Mono Input Attenuation. MIA0 is the least significant bit and represents 3 dB attenuation, with 0000 = 0 dB. See Table 7.

MOM — Mono Output Mute. The MOM bit will mute the mono mix output, MOUT. This mute is independent of the line output mute.

0 - no mute
1 - mute

MIM — Mono Input Mute. This bit controls the mute function on the mono input, MIN. The mono input provides mix for the "beeper" function in most personal computers.

0 - no mute
1 - muted

This register's initial state after reset is: 00xx0011.

4

RESERVED (I27)

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

This register's initial state after reset is: xxxxxxxx

Capture Data Format (I28)

D7	D6	D5	D4	D3	D2	D1	D0
FMT1	FMT0	C/$\overline{L}$	S/$\overline{M}$	res	res	res	res

S/$\overline{M}$ Stereo/Mono Select: This bit determines how the capture audio data stream is formatted. Selecting stereo will result with alternating samples representing left and right audio channels. Selecting mono only captures data from the left audio channel.

0 - Mono
1 - Stereo

The C/$\overline{L}$, FMT1, and FMT0 bits set the capture data format in MODE 2. See Table 10 or register I8 for the bit settings and data formats. The capture data format can be different that the playback data format; however, the sample frequency must be the same and is set in I8. MCE must be set to modify this register.
This register's initial state after reset is: 0000xxxx

RESERVED (I29)

D7	D6	D5	D4	D3	D2	D1	D0
res	res	res	res	res	res	res	res

This register's initial state after reset is: xxxxxxxx

Capture Upper Base (I30)

D7	D6	D5	D4	D3	D2	D1	D0
CUB7	CUB6	CUB5	CUB4	CUB3	CUB2	CUB1	CUB0

CUB7-CUB0 Capture Upper Base: This register is the upper byte which represents the 8 most significant bits of the 16-bit Capture Base register. Reads from this this register returns the same value that was written.

This register's initial state after reset is: 0000000

Capture Lower Base (I31)

D7	D6	D5	D4	D3	D2	D1	D0
CLB7	CLB6	CLB5	CLB4	CLB3	CLB2	CLB1	CLB0

CLB7-CLB0 Lower Base Bits: This register is the lower byte which represents the 8 least significant bits of the 16-bit Capture Base register. Reads from this register returns the same value which was written.

This register's initial state after reset is: 00000000

GROUNDING AND LAYOUT

Figure 16 is a suggested layout for the CS4231. Similar to other Crystal codecs, it is recommended that the device be located on a separate analog ground plane. With the CS4231's parallel data interface, however, optimum performance is achieved by extending the digital ground plane across pins 65 through 68 and pins 1 through 8. Pins 2 and 8 are grounds for the data bus and should be electrically connected to the digital ground plane which will minimize the effects of the bus interface due to transient currents during bus switching. Figure 17 shows the recommended positioning of the decoupling capacitors. The capacitors must be on the same layer as, and close to, the CS4231. The vias shown go through to the ground plane layer. Vias, power supply traces, and VREF traces should be as large as possible to minimize the impedance.

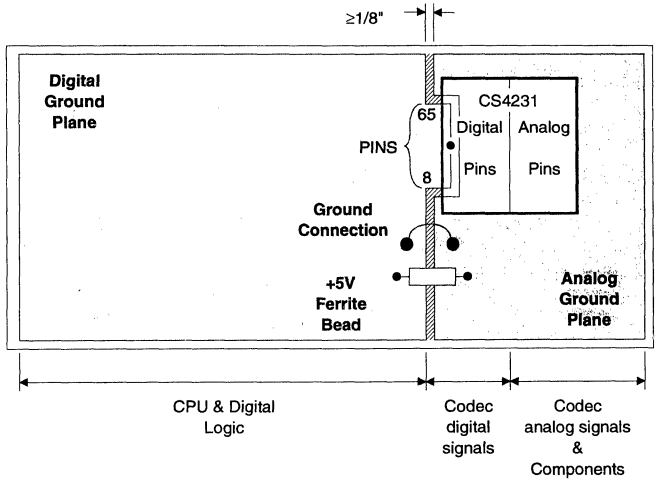


Figure 16. Suggested Layout Guideline

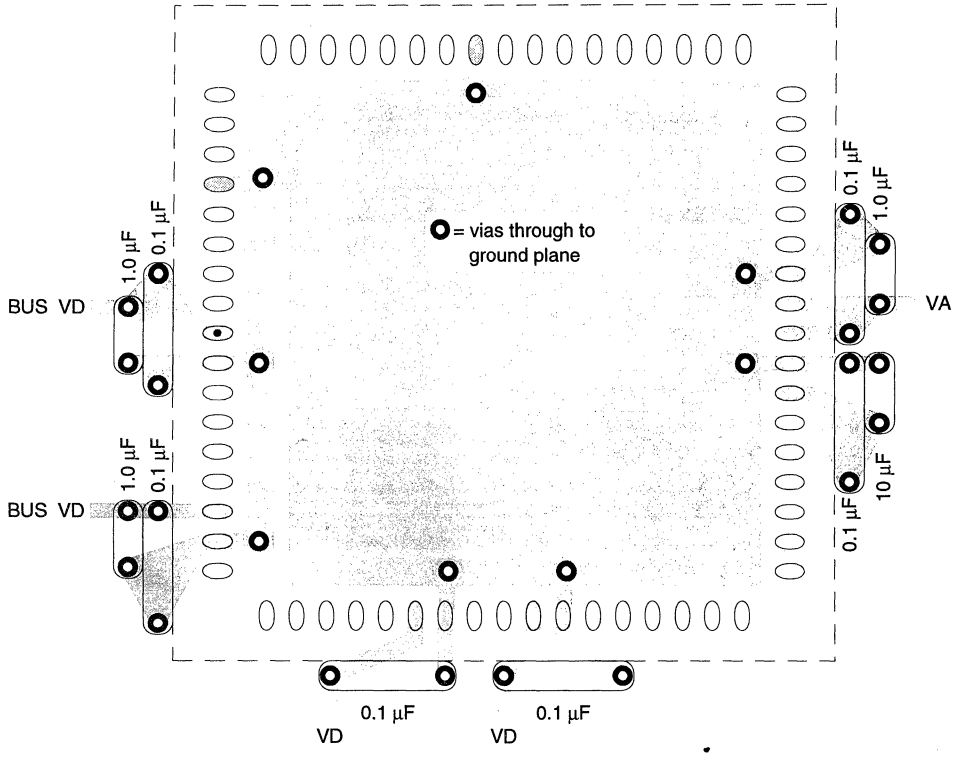


Figure 17. Recommended Decoupling Capacitor Positions

COMPATIBILITY WITH AD1848

The CS4231 is compatible with the AD1848 rev. J silicon and the CS4248 in terms of the applications circuit. The AD1848 rev K requires 0.1 µF capacitors (not 1000 pF) on pins 26 and 31. The CS4231 requires 1000 pF NPO-type capacitors on filter pins 26 and 31 (not 0.1 µF). To achieve compatibility with the CS4231:

1. Correct spacing of pads will ensure that either 0.1 µF capacitors (for the AD1848 rev K) or 1000 pF NPO capacitors (for the CS4248) may be installed.

2. The CS4231 does not require the input anti-aliasing filters included as an input R/C for the AD1848 (5.1kΩ and 560 pF). The additional R/C's can be used with the CS4231 if desired, with no degradation in performance.

3. Although optimum performance is achieved using the ground plane shown in Figure 16, any ground plane scheme that achieves acceptable performance with the AD1848 should work with the CS4231.

4. The AD1848 needs extra power and ground pins. The power pins (V_{DD}) are pins 24, 45, and 54. The ground pins (GNDD) are pins 25 and 44. The CS4231 PLCC package does not use these pins and the appropriate power/ground connections can be made.

5. The Mono In/Mono Out pins do not exist on the AD1848.

6. The AD1848 does not contain 16 mA bus drivers. Therefore, buffers must be used.

7. MODE 2 and all associated features do not exist on the AD1848.

8. The AD1848 does not contain the selectable dither (DEN, I10)

9. The AD1848 is not available in a 100-pin TQFP package.

ADC/DAC FILTER RESPONSE PLOTS

Figures 18 through 23 show the overall frequency response, passband ripple, and transition band for the CS4231 ADCs and DACs. Figure 24 shows the DACs' deviation from linear phase. Since the CS4231 scales filter response based on sample frequency selected, all frequency response plots x-axis' are shown from 0 to 1 where 1 is equivalent to Fs. Therefore, for any given sample frequency, multiply the x-axis values by the sample frequency selected to get the actual frequency.

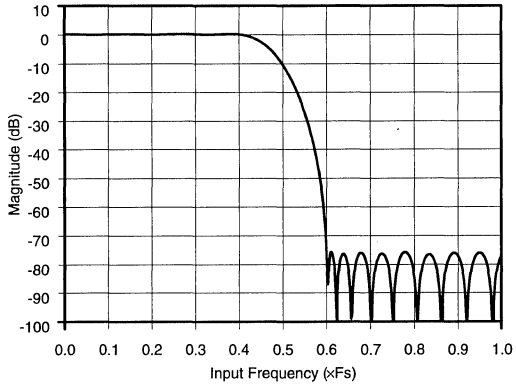


Figure 18. ADC Filter Response.

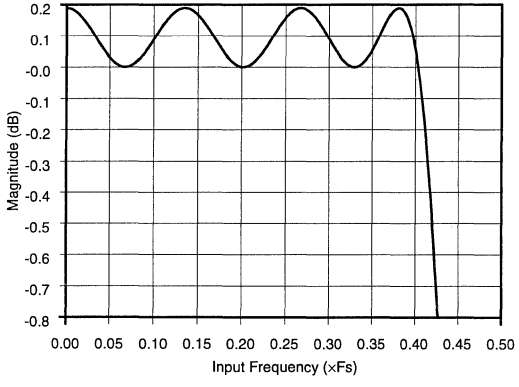


Figure 19. ADC Passband Ripple.

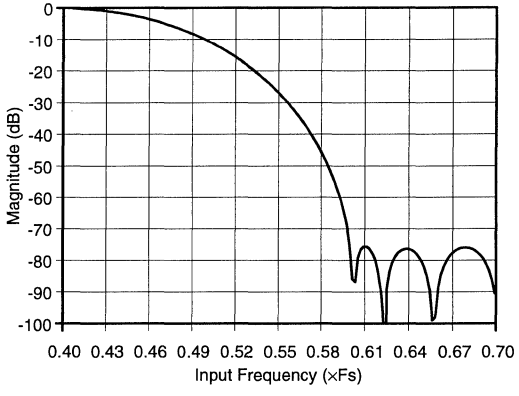


Figure 20. ADC Transition Band.

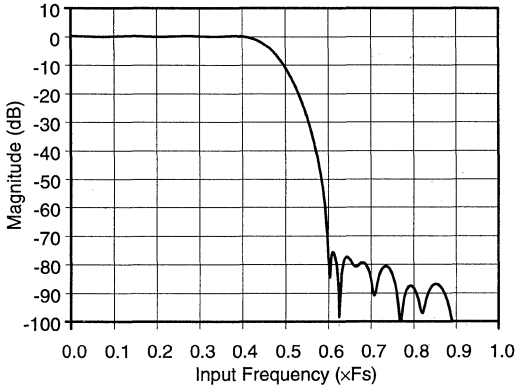


Figure 21. DAC Filter Response.

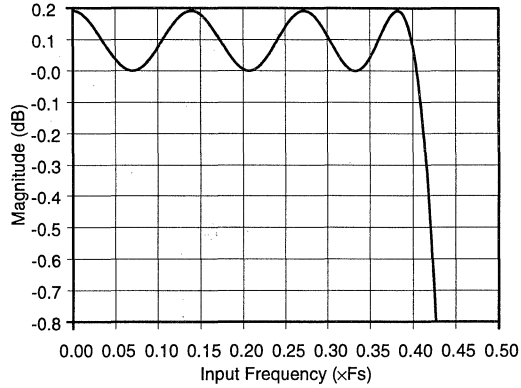


Figure 22. DAC Passband Ripple.

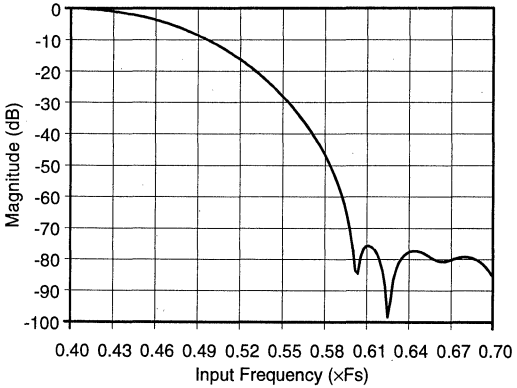


Figure 23. DAC Transition Band.

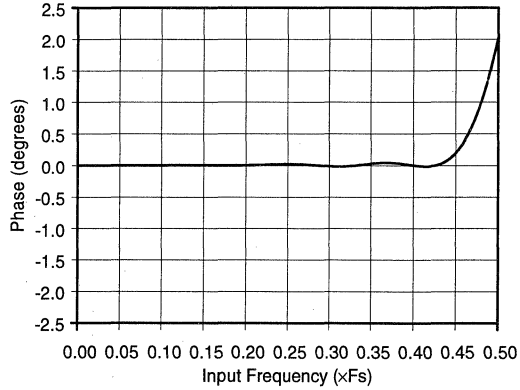
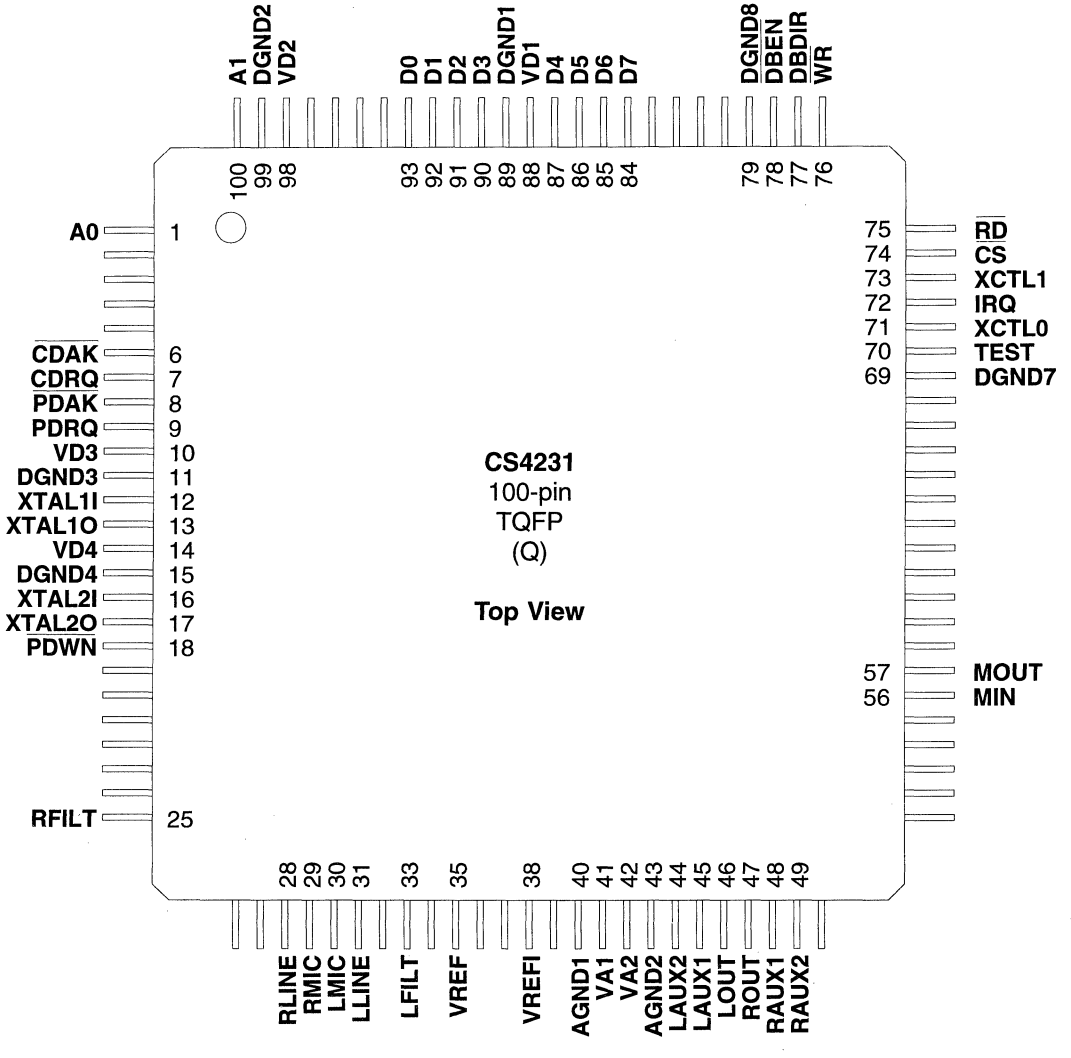
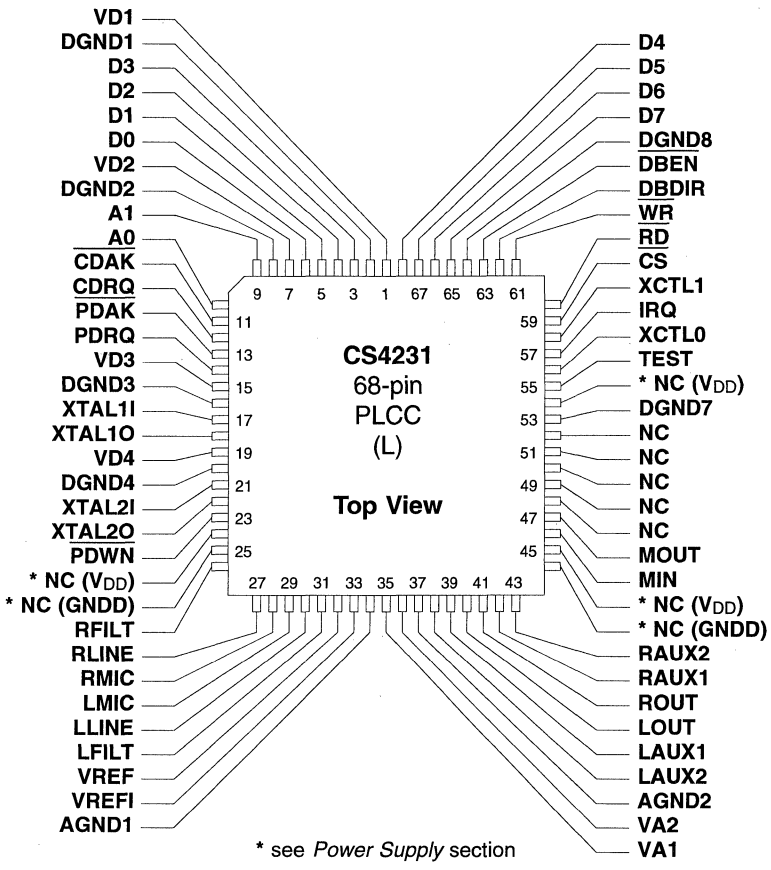


Figure 24. DAC Phase Response.

PIN DESCRIPTIONS





Parallel Bus Interface Pins

CDRQ - Capture Data Request, Output, Pin 12 (L), Pin 7 (Q).

The assertion of this signal indicates that the codec has a captured audio sample ready for transfer. This signal will remain asserted until all the bytes from the capture buffer have been transferred.

$\overline{\text{CDAK}}$ - Capture Data Acknowledge, Input, Pin 11 (L), Pin 6 ($\overline{\text{Q}}$).

The assertion of this active low signal indicates that the $\overline{\text{RD}}$ cycle occurring is a DMA read from the capture buffer.

PDRQ - Playback Data Request, Output, Pin 14 (L), Pin 9 (Q).

The assertion of this signal indicates that the codec is ready for more playback data. The signal will remain asserted until the bytes needed for a playback sample have been transferred.

$\overline{\text{PDAK}}$ - Playback Data Acknowledge, Input, Pin 13 (L), Pin 8 (Q).
The assertion of this active low signal indicates that the $\overline{\text{WR}}$ cycle occurring is a DMA write to the playback buffer.

A< 1:0> - Address Bus, Input, Pin 9, 10 (L), Pin 100, 1 (Q).
These address pins are read by the codec interface logic during an I/O cycle access. The state of these address lines determines which register (R0-R3) is accessed.

$\overline{\text{RD}}$ - Read Strobe, Input, Pin 60 (L), Pin 75 (Q).
This signal defines a read cycle to the codec. The cycle may be an I/O cycle read, or the cycle could be a read from the codec's DMA sample registers.

$\overline{\text{WR}}$ - Write Strobe, Input, Pin 61 (L), Pin 76 (Q).
This signal indicates a write cycle to the codec. The cycle may be an I/O cycle write, or the cycle could be a write to the codec's DMA sample registers.

$\overline{\text{CS}}$ - Chip Select, Input, Pin 59 (L), Pin 74 (Q).
The codec will not respond to any I/O cycle accesses unless this signal is active. This signal is ignored during DMA transfers.

D< 7:0> - Data Bus, Input/Output, Pin 65-68, 3-6 (L), Pin 84-87, 90-93 (Q).
These signals are used to transfer data to and from the CS4248.

$\overline{\text{DBEN}}$ - Data Bus Enable, Output, Pin 63 (L), Pin 78 (Q).
This pin indicates that the bus drivers attached to the CS4248 should be enabled. This signal is normally high.

DBDIR - Data Bus Direction, Output, Pin 62 (L), Pin 77 (Q).
This pin indicates the direction of the data bus transceiver. High points to the CS4231, low points to the host bus. This signal is normally high.

IRQ - Host Interrupt Pin, Output, Pin 57 (L), Pin 72 (Q).
This signal is used to notify the host of events which need servicing.

Analog Inputs

LLINE - Left Line Input, Pin 30 (L), Pin 31 (Q).
Nominally 1 V_{RMS} max analog input for the Left LINE channel, centered around VREF. The LINE inputs may be selected for A/D conversion via the input multiplexer (I0). A programmable gain block (I18) also allows routing to the mixer.

RLINE - Right Line Input, Pin 27 (L), Pin 28 (Q).
Nominally 1 V_{RMS} max analog input for the Right LINE channel, centered around VREF. The LINE inputs may be selected for A/D conversion via the input multiplexer (I1). A programmable gain block (I19) also allows routing to the mixer.

LMIC - Left Mic Input, Pin 29 (L), Pin 30 (Q).

Microphone input for the Left MIC channel, centered around VREF. This signal can be either 1 V_{RMS} (LMGE = 0) or 0.1 V_{RMS} (LMGE = 1). The MIC inputs may be selected for A/D conversion via the input multiplexer (I0).

RMIC - Right Mic Input, Pin 28 (L), Pin 29 (Q).

Microphone input for the Right MIC channel, centered around VREF. This signal can be either 1 V_{RMS} (RMGE = 0) or 0.1 V_{RMS} (RMGE = 1). The MIC inputs may be selected for A/D conversion via the input multiplexer (I1).

LAUX1 - Left Auxiliary #1 Input, Pin 39 (L), Pin 45 (Q).

Nominally 1 V_{RMS} max analog input for the Left AUX1 channel, centered around VREF. The AUX1 inputs may be selected for A/D conversion via the input multiplexer (I0). A programmable gain block (I2) also allows routing to the output mixer.

RAUX1 - Right Auxiliary #1 Input, Pin 42 (L), Pin 48 (Q).

Nominally 1 V_{RMS} max analog input for the Right AUX1 channel, centered around VREF. The AUX1 inputs may be selected for A/D conversion via the input multiplexer (I1). A programmable gain block (I3) also allows routing to the output mixer.

LAUX2 - Left Auxiliary #2 Input, Pin 38 (L), Pin 44 (Q).

Nominally 1 V_{RMS} max analog input for the Left AUX2 channel, centered around VREF. A programmable gain block (I4) allows routing of the AUX2 channels into the output mixer.

RAUX2 - Right Auxiliary #2 Input, Pin 43 (L), Pin 49 (Q).

Nominally 1 V_{RMS} max analog input for the Right AUX2 channel, centered around VREF. A programmable gain block (I5) allows routing of the AUX2 channels into the output mixer.

MIN - Mono Input, Pin 46 (L), Pin 56 (Q).

Nominally 1 V_{RMS} max analog input, centered around VREF, that goes through a programmable gain stage (I26) into both channels of the mixer. This is a general purpose mono analog input that is normally used to mix the typical "beeper" signal on most computers into the audio system.

Analog Outputs

LOUT - Left Line Level Output, Pin 40 (L), Pin 46 (Q).

Analog output from the mixer for the left channel. Nominally 1 V_{RMS} max centered around VREF when OLB = 1 (I16). When OLB = 0, the output is attenuated 3 dB and is a maximum of 0.707 V_{RMS}.

ROUT - Right Line Level Output, Pin 41 (L), Pin 47 (Q).

Analog output from the mixer for the right channel. Nominally 1 V_{RMS} max centered around VREF when OLB = 1 (I16). When OLB = 0, the output is attenuated 3 dB and is a maximum of 0.707 V_{RMS}.

MOUT - Mono Output, Pin 47 (L), Pin 57 (Q).

When OLB=1 (I16), MOUT is nominally 1 V_{RMS} max analog output, centered around VREF. When OLB=0, the maximum output voltage is 3 dB lower, 0.707 V_{RMS}. This output is a summed analog output from both the left and right output channels of the mixer. MOUT typically is connected to a speaker driver that drives the internal speaker in most computers. Independantly mutable via MOM in I26.

Miscellaneous

XTAL1I - Crystal #1 Input, Pin 17 (L), Pin 12 (Q).

This pin will accept either a crystal with the other pin attached to XTAL1O or an external CMOS clock. XTAL1 must have a crystal or clock source attached for proper operation. The standard crystal frequency is 24.576 MHz although other frequencies can be used. The crystal should be designed for fundamental mode, parallel resonance operation.

XTAL1O - Crystal #1 Output, Pin 18 (L), Pin 13 (Q).

This pin is used for a crystal placed between this pin and XTAL1I.

XTAL2I - Crystal #2 Input, Pin 21 (L), Pin 16 (Q).

If a second crystal is used, is should be placed between this pin and XTAL2O. The standard crystal frequency is 16.9344 MHz although other frequencies can be used. The crystal should be designed for fundamental mode, parallel resonance operation.

XTAL2O - Crystal #2 Output, Pin 22 (L), Pin 17 (Q).

This pin is used for a crystal placed between this pin and XTAL2I.

$\overline{\text{PDWN}}$ - Power Down, Input, Pin 23 (L), Pin 18 (Q).

Places CS4231 in lowest power consumption mode. All sections of the CS4231, except the digital bus interface which reads 80h, are shut down and consuming minimal power. The CS4231 is in power down mode when this pin is logic low.

XCTL0, XCTL1 - External Control, Output, Pin 56, 58 (L), Pin 71, 73 (Q).

These signals are controlled by the register bits XCTL0 and XCTL1 in register I10. They can be used to control external logic via TTL levels.

VREF - Voltage Reference, Output, Pin 32 (L), Pin 35 (Q).

All analog inputs and outputs are centered around VREF which is nominally 2.1 Volts. This pin may be used to level shift external circuitry, although any AC loads should be buffered. High internal-gain microphone inputs can be slightly improved by placing a 10µF capacitor on VREF.

VREFI - Voltage Reference Internal, Input, Pin 33 (L), Pin 38 (Q).

Voltage reference used internal to the CS4231 must have a 0.1 µF + 10 µF capacitor with short fat traces to attach to this pin. No other connections should be made to this pin.

LFILT - Left Channel Antialias Filter Input, Pin 31 (L), Pin 33 (Q).
This pin needs 1000 pF NPO capacitor attached and tied to analog ground.

RFILT - Right Channel Antialias Filter Input, Pin 26 (L), Pin 25 (Q).
This pin needs 1000 pF NPO capacitor attached and tied to analog ground.

TEST - Test, Pin 55 (L), Pin 70 (Q).
This pin must be tied to ground for proper operation.

Power Supplies

VA1, VA2 - Analog Supply Voltage, Pin 35, 36 (L), Pin 41, 42 (Q).
Supply to the analog section of the codec.

AGND1, AGND2 - Analog Ground, Pin 34, 37 (L), Pin 40, 43 (Q).
Ground reference to the analog section of the codec. Internally, these pins are connected to the substrate as are DGND3/4/7/8; therefore, optimum layout is achieved with the AGND pins on the same ground plane as DGND3/4/7/8 (see Figure 17). However, other ground arrangements should yield adequate results.

VD1, VD2 - Digital Supply Voltage, Pin 1, 7 (L), Pin 88, 98 (Q).
Digital supply for the parallel data bus section of the codec.

VD3, VD4 - Digital Supply Voltage, Pin 15, 19 (L), Pin 10, 14 (Q).
Digital supply for the internal digital section of the codec (except for the parallel data bus).

DGND1, DGND2 - Digital Ground, Pin 2, 8 (L), Pin 89, 99 (Q).
Digital ground reference for the parallel data bus section of the codec. These pins are isolated from the other digital grounds and should be connected to the digital ground section of the board (see Figure 17).

DGND3, DGND4, DGND7, DGND8 - Digital Ground, Pin 16, 20, 53, 64(L), Pin 11, 15, 69, 79(Q)
Digital ground reference for the internal digital section of the codec (except the parallel data bus). These pins are connected to the substrate of the die as are the AGND pins. Optimum layout is achieved by placing DGND3/4/7/8 on the analog ground plane with the AGND pins as shown in Figure 17. However, other ground arrangements should yield adequate results.

*** NC (V_{DD}) - No Connect, Pins 24, 45, 54 (L)**
These pins are no connects for the CS4231. When compatibility with the AD1848 is desired, these pins should be connected to the digital power supply. For other compatibility issues, see the *Compatibility with AD1848* section of the data sheet.

*** NC (GNDD) - No Connect, Pins 25, 44 (L)**
These pins are no connects for the CS4231. When compatibility with the AD1848 is desired, these pins should be connected to digital ground. For other compatibility issues, see the *Compatibility with AD1848* section of the data sheet.

PARAMETER DEFINITIONS

Resolution

The number of bits in the input words to the DACs, and in the output words in the ADCs.

Differential Nonlinearity

The worst case deviation from the ideal code width. Units in LSB.

Total Dynamic Range

TDR is the ratio of the rms value of a full scale signal to the lowest obtainable noise floor. It is measured by comparing a full scale signal to the lowest noise floor possible in the codec (i.e. attenuation bits for the DACs at full attenuation). Units in dB.

Instantaneous Dynamic Range

IDR is the ratio of a full-scale rms signal to the rms noise available at any instant in time, without changing the input gain or output attenuation settings. It is measured using S/(N+D) with a 1 kHz, -60 dB input signal, with 60 dB added to compensate for the small input signal. Use of a small input signal reduces the harmonic distortion components to insignificance when compared to the noise. Units in dB.

Total Harmonic Distortion (THD)

THD is the ratio of the test signal amplitude to the rms sum of all the in-band harmonics of the test signal.

Interchannel Isolation

The amount of 1 kHz signal present on the output of the grounded input channel with 1 kHz 0 dB signal present on the other channel. Units in dB.

Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units in dB.

Offset Error

For the ADCs, the deviation in LSBs of the output from mid-scale with the selected input grounded. For the DACs, the deviation in volts of the output from VREF with mid-scale input code.

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