

# HM514280 Series

Preliminary

262,144-Word x 18-Bit Dynamic Random Access Memory

## DESCRIPTION

The Hitachi HM514280 are CMOS dynamic RAM organized as 262,144-word x 18-bit. HM514280 have realized higher density, higher performance and various functions by employing 0.8  $\mu\text{m}$  CMOS process technology and some new CMOS circuit design technologies. The HM514280 offer Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514280 to be packaged in standard 400 mil 40-pin plastic SOJ, standard 475 mil 40-pin plastic ZIP.

## FEATURES

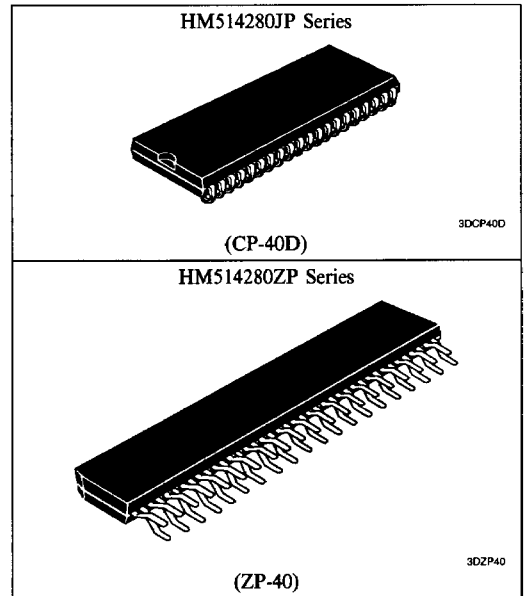
- Single 5V ( $\pm 10\%$ )
- High Speed
  - Access Time ..... 70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode ..... 935 mW/825 mW/715 mW (max)
  - Standby Mode ..... 11 mW (max)
- Fast Page Mode Capability
- 512 Refresh Cycles ..... (8 ms)
- 2CAS Byte Control
- 3 Variations of Refresh
  - RAS Only Refresh
  - CAS Before RAS Refresh
  - Hidden Refresh

## ORDERING INFORMATION

Part No.	Access Time	Package
HM514280JP-7	70 ns	400 mil 40-pin Plastic SOJ (CP-40D)
HM514280JP-8	80 ns	
HM514280JP-10	100 ns	
HM514280ZP-7	70 ns	475 mil 40-pin Plastic ZIP (ZP-40)
HM514280ZP-8	80 ns	
HM514280ZP-10	100 ns	

## PIN DESCRIPTION

Pin Name	Function
A <sub>0</sub> -A <sub>8</sub>	Address Input
—Row Address	A <sub>0</sub> -A <sub>8</sub>
—Column Address	A <sub>0</sub> -A <sub>8</sub>
—Refresh Address	A <sub>0</sub> -A <sub>8</sub>
I/O <sub>0</sub> -I/O <sub>17</sub>	Data-in/Data-out
RAS	Row Address Strobe
UCAS, LCAS	Column Address Strobe
WE	Read/Write Enable
OE	Output Enable
V <sub>CC</sub>	Power (+ 5V)
V <sub>SS</sub>	Ground



## PIN OUT

HM514280JP Series			
V <sub>CC</sub> □ 1	40 □ V <sub>SS</sub>		
I/O0 □ 2	39 □ I/O17		
I/O1 □ 3	38 □ I/O16		
I/O2 □ 4	37 □ I/O15		
I/O3 □ 5	36 □ I/O14		
V <sub>CC</sub> □ 6	35 □ V <sub>SS</sub>		
I/O4 □ 7	34 □ I/O13		
I/O5 □ 8	33 □ I/O12		
I/O6 □ 9	32 □ I/O11		
I/O7 □ 10	31 □ I/O10		
I/O8 □ 11	30 □ I/O9		
NC □ 12	29 □ LCAS		
WE □ 13	28 □ UCAS		
RAS □ 14	27 □ OE		
NC □ 15	26 □ A8		
A0 □ 16	25 □ A7		
A1 □ 17	24 □ A6		
A2 □ 18	23 □ A5		
A3 □ 19	22 □ A4		
V <sub>CC</sub> □ 20	21 □ V <sub>SS</sub>		

(Top View) 0151-1

HM514280ZP Series			
I/O <sub>11</sub> 2	1 I/O <sub>10</sub>		
I/O <sub>13</sub> 4	3 I/O <sub>12</sub>		
I/O <sub>14</sub> 6	5 V <sub>SS</sub>		
I/O <sub>16</sub> 8	7 I/O <sub>15</sub>		
V <sub>SS</sub> 10	9 I/O <sub>17</sub>		
I/O <sub>0</sub> 12	11 V <sub>CC</sub>		
I/O <sub>2</sub> 14	13 I/O <sub>1</sub>		
V <sub>CC</sub> 16	15 I/O <sub>3</sub>		
I/O <sub>5</sub> 18	17 I/O <sub>4</sub>		
I/O <sub>7</sub> 20	19 I/O <sub>6</sub>		
NC 22	21 I/O <sub>8</sub>		
RAS 24	23 WE		
A <sub>0</sub> 26	25 NC		
A <sub>2</sub> 28	27 A <sub>1</sub>		
V <sub>CC</sub> 30	29 A <sub>3</sub>		
A <sub>4</sub> 32	31 V <sub>SS</sub>		
A <sub>6</sub> 34	33 A <sub>5</sub>		
A <sub>8</sub> 36	35 A <sub>7</sub>		
UCAS 38	37 OE		
I/O <sub>9</sub> 40	39 LCAS		

(Bottom View)



## ■ TRUTH TABLE

Inputs					I/O		Operation
$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	I/O <sub>0</sub> -I/O <sub>8</sub>	I/O <sub>9</sub> -I/O <sub>17</sub>	
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	L	H	H	L	D <sub>out</sub>	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D <sub>out</sub>	Upper Byte Read
L	L	L	H	L	D <sub>out</sub>	D <sub>out</sub>	Word Read
L	L	H	L	H	D <sub>in</sub>	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D <sub>in</sub>	Upper Byte Write
L	L	L	L	H	D <sub>in</sub>	D <sub>in</sub>	Word Write
L	L	L	H	H	High-Z	High-Z	

## ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V <sub>SS</sub>	V <sub>T</sub>	- 1.0 to + 7.0	V
Supply Voltage Relative to V <sub>SS</sub>	V <sub>CC</sub>	- 1.0 to + 7.0	V
Short Circuit Output Current	I <sub>out</sub>	50	mA
Power Dissipation	P <sub>T</sub>	1.0	W
Operating Temperature	T <sub>opr</sub>	0 to + 70	°C
Storage Temperature	T <sub>stg</sub>	- 55 to + 125	°C

## ■ ELECTRICAL CHARACTERISTICS

### • Recommended DC Operating Conditions (T<sub>A</sub> = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V <sub>SS</sub>	0	0	0	V	
	V <sub>CC</sub>	4.5	5.0	5.5	V	1
Input High Voltage	V <sub>IH</sub>	2.4	—	6.5	V	1
Input Low Voltage	(I/O Pin) V <sub>IL</sub>	- 1.0	—	0.8	V	1
	(Others) V <sub>IL</sub>	- 2.0	—	0.8	V	1

Note: 1. All voltage referenced to V<sub>SS</sub>.

### • DC Electrical Characteristics (T<sub>A</sub> = 0 to + 70°C, V<sub>CC</sub> = 5V ± 10%, V<sub>SS</sub> = 0V)

Parameter	Symbol	HM514280-7		HM514280-8		HM514280-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I <sub>CC1</sub>	—	170	—	150	—	130	mA	$\overline{\text{RAS}}$ Cycling $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ Cycling t <sub>RC</sub> = Min	1, 2
Standby Current	I <sub>CC2</sub>	—	2	—	2	—	2	mA	TTL Interface $\overline{\text{RAS}}$ , $\overline{\text{LCAS}}$ , $\overline{\text{UCAS}}$ = V <sub>IH</sub> , D <sub>out</sub> = High-Z	
		—	1	—	1	—	1	mA	CMOS Interface $\overline{\text{RAS}}$ , $\overline{\text{LCAS}}$ , $\overline{\text{UCAS}}$ ≥ V <sub>CC</sub> - 0.2V, D <sub>out</sub> = High-Z	
$\overline{\text{RAS}}$ Only Refresh Current	I <sub>CC3</sub>	—	150	—	130	—	110	mA	t <sub>RC</sub> = Min	2
Standby Current	I <sub>CC5</sub>	—	5	—	5	—	5	mA	$\overline{\text{RAS}}$ = V <sub>IH</sub> , $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ = V <sub>IL</sub> , D <sub>out</sub> = Enable	1
CAS Before $\overline{\text{RAS}}$ Refresh Current	I <sub>CC6</sub>	—	150	—	130	—	110	mA	t <sub>RC</sub> = Min	
Fast Page Mode Current	I <sub>CC7</sub>	—	130	—	120	—	110	mA	t <sub>PC</sub> = Min	1, 3
Input Leakage Current	I <sub>LI</sub>	- 10	10	- 10	10	- 10	10	μA	0V ≤ V <sub>in</sub> ≤ 7V	



• **DC Electrical Characteristics** ( $T_A = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$ ) (continued)

Parameter	Symbol	HM514280-7		HM514280-8		HM514280-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Output Leakage Current	$I_{LO}$	-10	10	-10	10	-10	10	$\mu\text{A}$	$0\text{V} \leq V_{out} \leq 7\text{V}$ , $D_{out} = \text{Disable}$	
Output High Voltage	$V_{OH}$	2.4	$V_{CC}$	2.4	$V_{CC}$	2.4	$V_{CC}$	V	High $I_{out} = -5\text{mA}$	
Output Low Voltage	$V_{OL}$	0	0.4	0	0.4	0	0.4	V	Low $I_{out} = 4.2\text{mA}$	

- Notes: 1.  $I_{CC}$  depends on output load condition when the device is selected,  $I_{CC}$  max is specified at the output open condition.  
 2. Address can be changed  $\leq 1$  time while  $\overline{RAS} = V_{IL}$ .  
 3. Address can be changed  $\leq 1$  time while  $\overline{LCAS}$  and  $\overline{UCAS} = V_{IH}$ .

• **Capacitance** ( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ )

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	$C_{I1}$	—	5	pF	1
Input Capacitance (Clocks)	$C_{I2}$	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

- Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.  
 2.  $\overline{LCAS}$  and  $\overline{UCAS} = V_{IH}$  to disable  $D_{out}$ .

• **AC Electrical Characteristics** ( $T_A = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$ )<sup>1, 14, 15</sup>  
**Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)**

Parameter	Symbol	HM514280-7		HM514280-8		HM514280-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	$t_{RC}$	130	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	$t_{RP}$	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	$t_{RAS}$	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	$t_{CAS}$	20	10000	20	10000	25	10000	ns	
Row Address Setup Time	$t_{ASR}$	0	—	0	—	0	—	ns	
Row Address Hold Time	$t_{RAH}$	10	—	10	—	15	—	ns	
Column Address Setup Time	$t_{ASC}$	0	—	0	—	0	—	ns	
Column Address Hold Time	$t_{CAH}$	15	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	$t_{RCD}$	20	50	20	60	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	$t_{RAD}$	15	35	15	40	20	55	ns	9
$\overline{RAS}$ Hold Time	$t_{RSH}$	20	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	$t_{CSH}$	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	$t_{CRP}$	10	—	10	—	10	—	ns	
$\overline{OE}$ to $D_{in}$ Delay Time	$t_{ODD}$	20	—	20	—	25	—	ns	
$\overline{OE}$ Delay Time from $D_{in}$	$t_{DZO}$	0	—	0	—	0	—	ns	
$\overline{CAS}$ Setup Time from $D_{in}$	$t_{DZC}$	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	$t_T$	3	50	3	50	3	50	ns	7
Refresh Period	$t_{REF}$	—	16	—	16	—	16	ms	



## Read Cycle

Parameter	Symbol	HM514280-7		HM514280-8		HM514280-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{\text{RAS}}$	$t_{\text{RAC}}$	—	70	—	80	—	100	ns	2, 3
Access Time from $\overline{\text{CAS}}$	$t_{\text{CAC}}$	—	20	—	20	—	25	ns	3, 4, 13
Access Time from Address	$t_{\text{AA}}$	—	35	—	40	—	45	ns	3, 5, 13
Access Time from $\overline{\text{OE}}$	$t_{\text{OAC}}$	—	20	—	20	—	25	ns	
Read Command Setup Time	$t_{\text{RCS}}$	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{\text{CAS}}$	$t_{\text{RCH}}$	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{\text{RAS}}$	$t_{\text{RRH}}$	0	—	0	—	0	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	$t_{\text{RAL}}$	35	—	40	—	55	—	ns	
Output Buffer Turn-off Time	$t_{\text{OFF1}}$	0	15	0	15	0	20	ns	6
Output Buffer Turn-off to $\overline{\text{OE}}$	$t_{\text{OFF2}}$	0	15	0	15	0	20	ns	6
$\overline{\text{CAS}}$ to $\text{D}_{\text{in}}$ Delay Time	$t_{\text{CDD}}$	15	—	15	—	20	—	ns	

## Write Cycle

Parameter	Symbol	HM514280-7		HM514280-8		HM514280-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	$t_{\text{WCS}}$	0	—	0	—	0	—	ns	10
Write Command Hold Time	$t_{\text{WCH}}$	15	—	15	—	20	—	ns	
Write Command Pulse Width	$t_{\text{WP}}$	10	—	10	—	20	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	$t_{\text{RWL}}$	20	—	20	—	25	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	$t_{\text{CWL}}$	20	—	20	—	25	—	ns	
Data-in Setup Time	$t_{\text{DS}}$	0	—	0	—	0	—	ns	11
Data-in Hold Time	$t_{\text{DH}}$	15	—	15	—	20	—	ns	11

## Read-Modify-Write Cycle

Parameter	Symbol	HM514280-7		HM514280-8		HM514280-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	$t_{\text{RWC}}$	180	—	200	—	245	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	$t_{\text{RWD}}$	95	—	105	—	135	—	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	$t_{\text{CWD}}$	45	—	45	—	60	—	ns	10
Column Address to $\overline{\text{WE}}$ Delay Time	$t_{\text{AWD}}$	60	—	65	—	80	—	ns	10, 13
$\overline{\text{OE}}$ Hold Time from $\overline{\text{WE}}$	$t_{\text{OEH}}$	20	—	20	—	25	—	ns	

## Refresh Cycle

Parameter	Symbol	HM514280-7		HM514280-8		HM514280-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{\text{CAS}}$ Setup Time ( $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle)	$t_{\text{CSR}}$	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle)	$t_{\text{CHR}}$	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	$t_{\text{RPC}}$	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time in Normal Mode	$t_{\text{CPN}}$	10	—	10	—	10	—	ns	



## Fast Page Mode Cycle

Parameter	Symbol	HM514280-7		HM514280-8		HM514280-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	$t_{PC}$	45	—	50	—	55	—	ns	
Fast Page Mode CAS Precharge Time	$t_{CP}$	10	—	10	—	10	—	ns	
Fast Page Mode RAS Pulse Width	$t_{RASC}$	—	100000	—	100000	—	100000	ns	12
Access Time from CAS Precharge	$t_{ACP}$	—	40	—	45	—	50	ns	3, 13
RAS Hold Time from CAS Precharge	$t_{RHCP}$	40	—	45	—	50	—	ns	
Fast Page Mode Read-Modify-Write Cycle CAS Precharge to $\overline{WE}$ Delay Time	$t_{CPW}$	65	—	70	—	85	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	$t_{PCM}$	95	—	100	—	110	—	ns	

## Counter Test Cycle

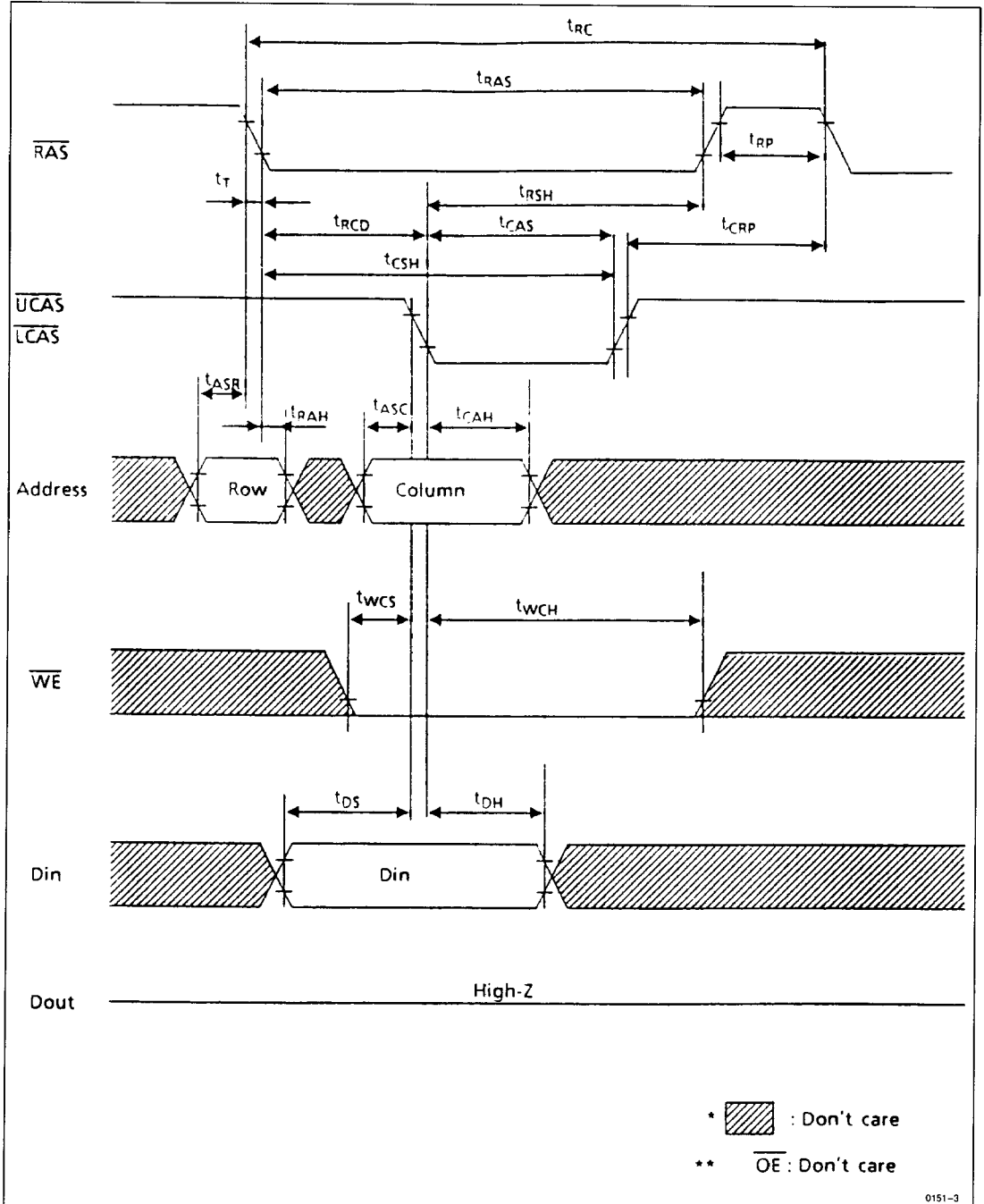
Parameter	Symbol	HM514280-7		HM514280-8		HM514280-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
CAS Precharge Time in Counter Test Cycle	$t_{CPT}$	50	—	50	—	50	—	ns	

- Notes:
1. AC measurements assume  $t_T = 5$  ns.
  2. Assumes that  $t_{RCD} \leq t_{RCD}(\max)$  and  $t_{RAD} \leq t_{RAD}(\max)$ . If  $t_{RCD}$  or  $t_{RAD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  exceeds the value shown.
  3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
  4. Assumes that  $t_{RCD} \geq t_{RCD}(\max)$  and  $t_{RAD} \leq t_{RAD}(\max)$ .
  5. Assumes that  $t_{RCD} \leq t_{RCD}(\max)$  and  $t_{RAD} \geq t_{RAD}(\max)$ .
  6.  $t_{OFF}(\max)$  defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
  7.  $V_{IH}(\min)$  and  $V_{IL}(\max)$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
  8. Operation with the  $t_{RCD}(\max)$  limit insures that  $t_{RAC}(\max)$  can be met,  $t_{RCD}(\max)$  is specified as a reference point only, if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\max)$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
  9. Operation with the  $t_{RAD}(\max)$  limit insures that  $t_{RAC}(\max)$  can be met,  $t_{RAD}(\max)$  is specified as a reference point only, if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\max)$  limit, then access time is controlled exclusively by  $t_{AA}$ .
  10.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if  $t_{WCS} \geq t_{WCS}(\min)$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{RWD} \geq t_{RWD}(\min)$ ,  $t_{CWD} \geq t_{CWD}(\min)$ ,  $t_{AWD} \geq t_{AWD}(\min)$  and  $t_{CPW} \geq t_{CPW}(\min)$ , the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
  11. These parameters are referenced to  $\overline{CAS}$  leading edge in an early write cycle and to  $\overline{WE}$  leading edge in a delayed write or a read-modify-write cycle.
  12.  $t_{RASC}$  defines RAS pulse width in fast page mode cycles.
  13. Access time is determined by the longer of  $t_{AA}$  or  $t_{CAC}$  or  $t_{ACP}$ .
  14. An initial pause of 100  $\mu$ s is required after power up followed by a minimum of eight initialization cycles ( $\overline{RAS}$  only refresh cycle or  $\overline{CAS}$  before  $\overline{RAS}$  refresh cycle). If the internal refresh counter is used, a minimum of eight CAS before RAS refresh cycles is required.
  15. In delayed write or read-modify-write cycles,  $\overline{OE}$  must disable output buffer prior to applying data to the device.
  16. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
  17. When both  $\overline{LCAS}$  and  $\overline{UCAS}$  go low at the same time, all 18-bits data are written into the device.  $\overline{LCAS}$  and  $\overline{UCAS}$  cannot be staggered within the same write/read cycles.





• Early Write Cycle



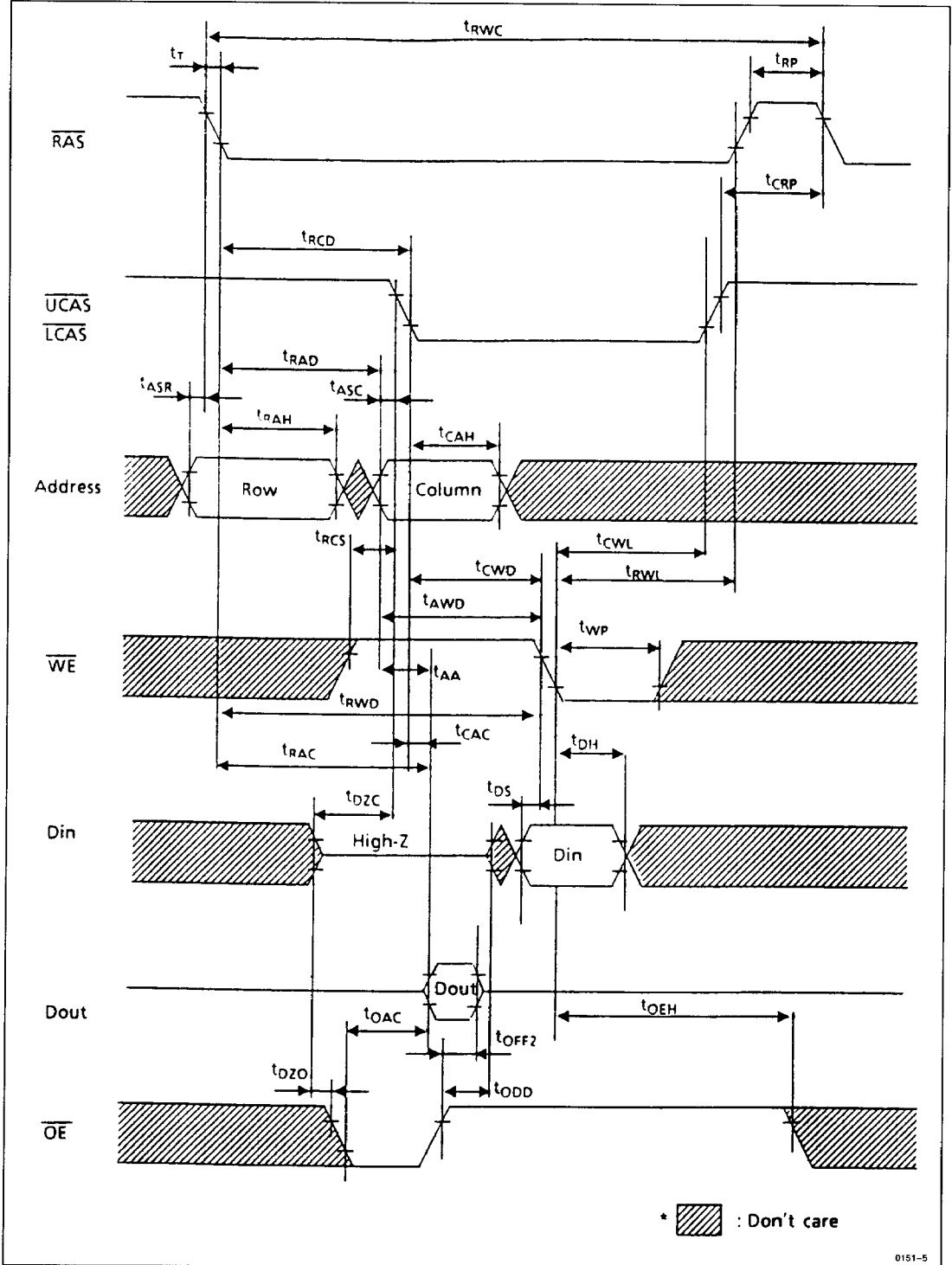
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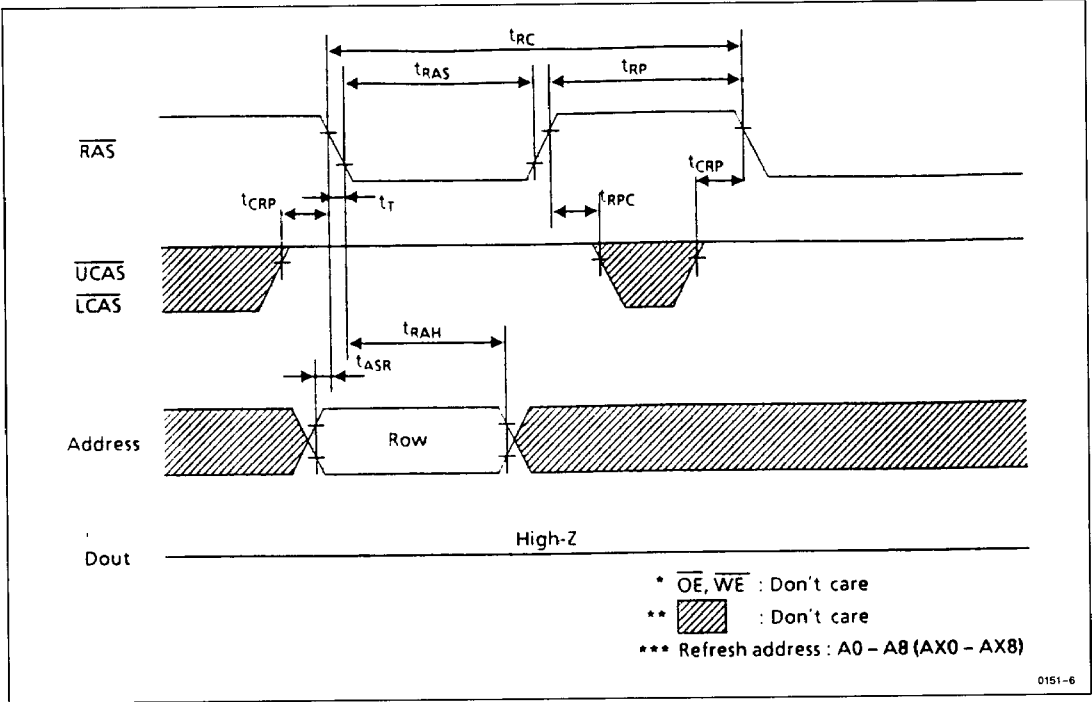
• Read-Modify-Write Cycle



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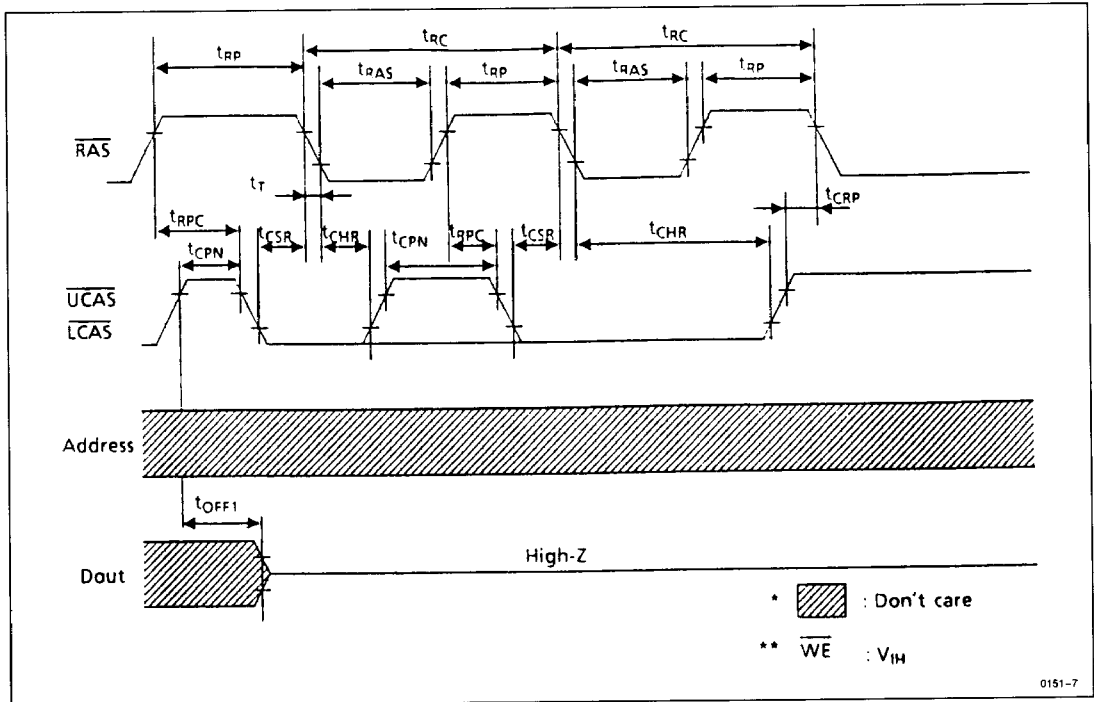


• **RAS Only Refresh Cycle**



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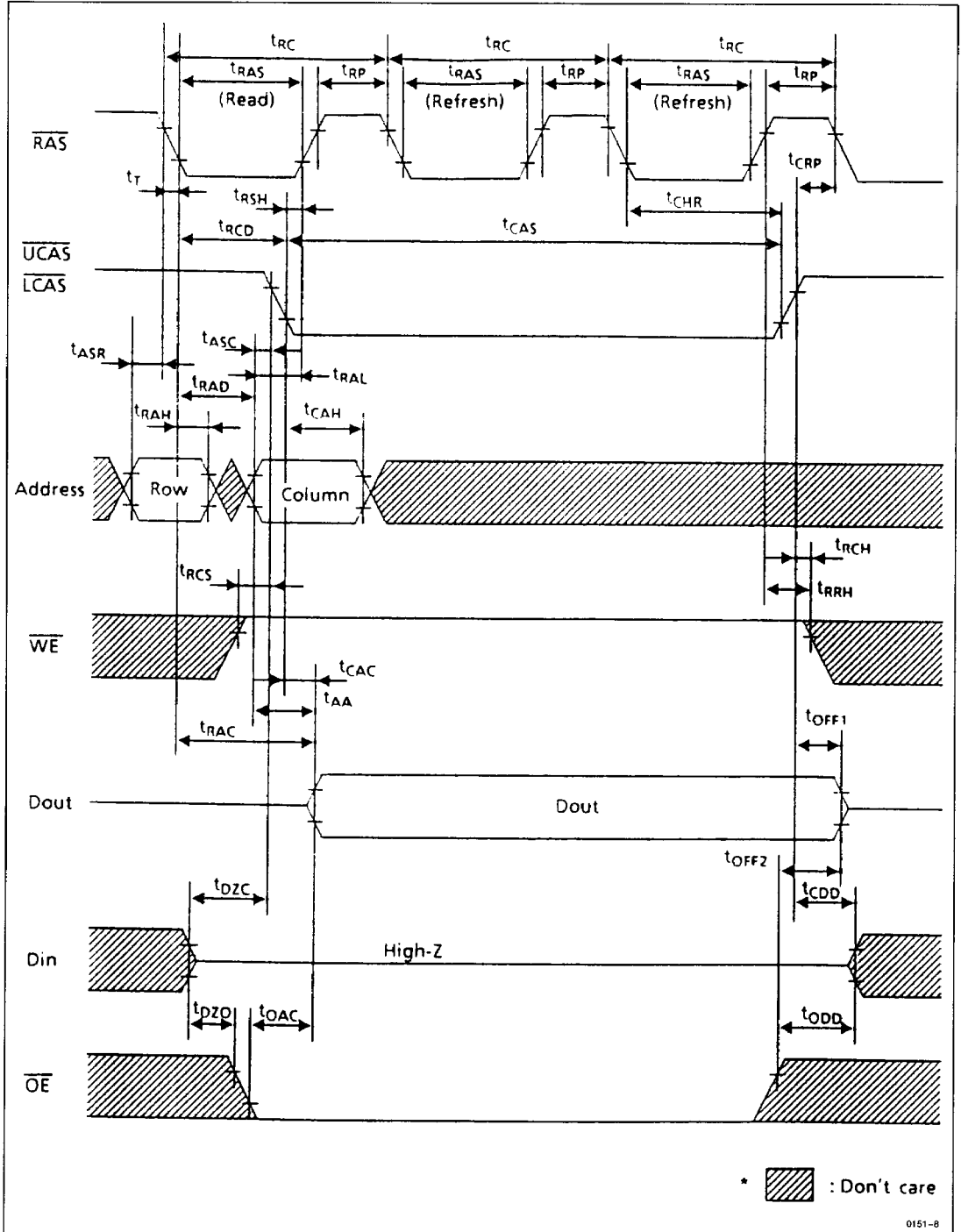
• **CAS Before RAS Refresh Cycle**



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• Hidden Refresh Cycle

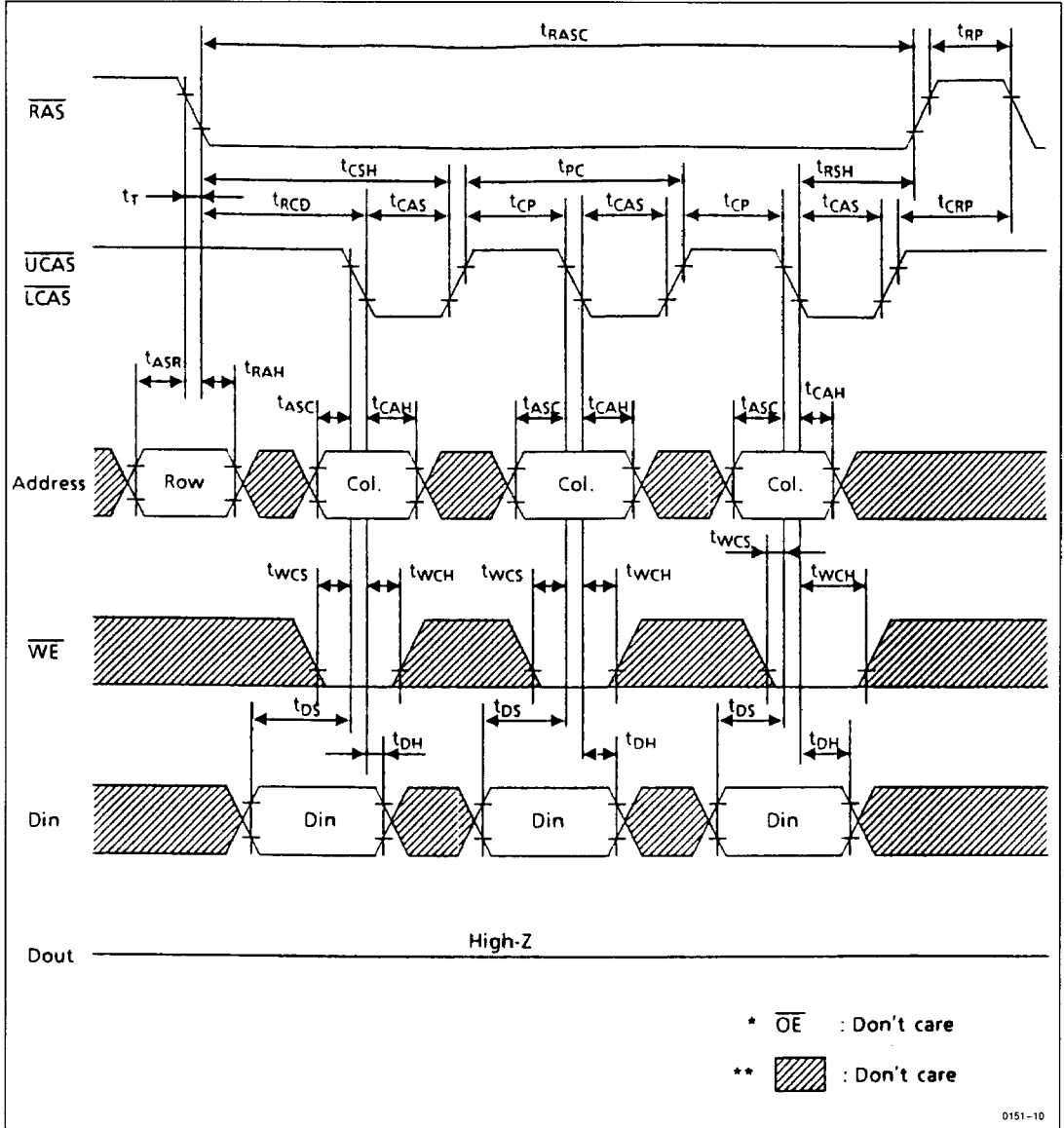


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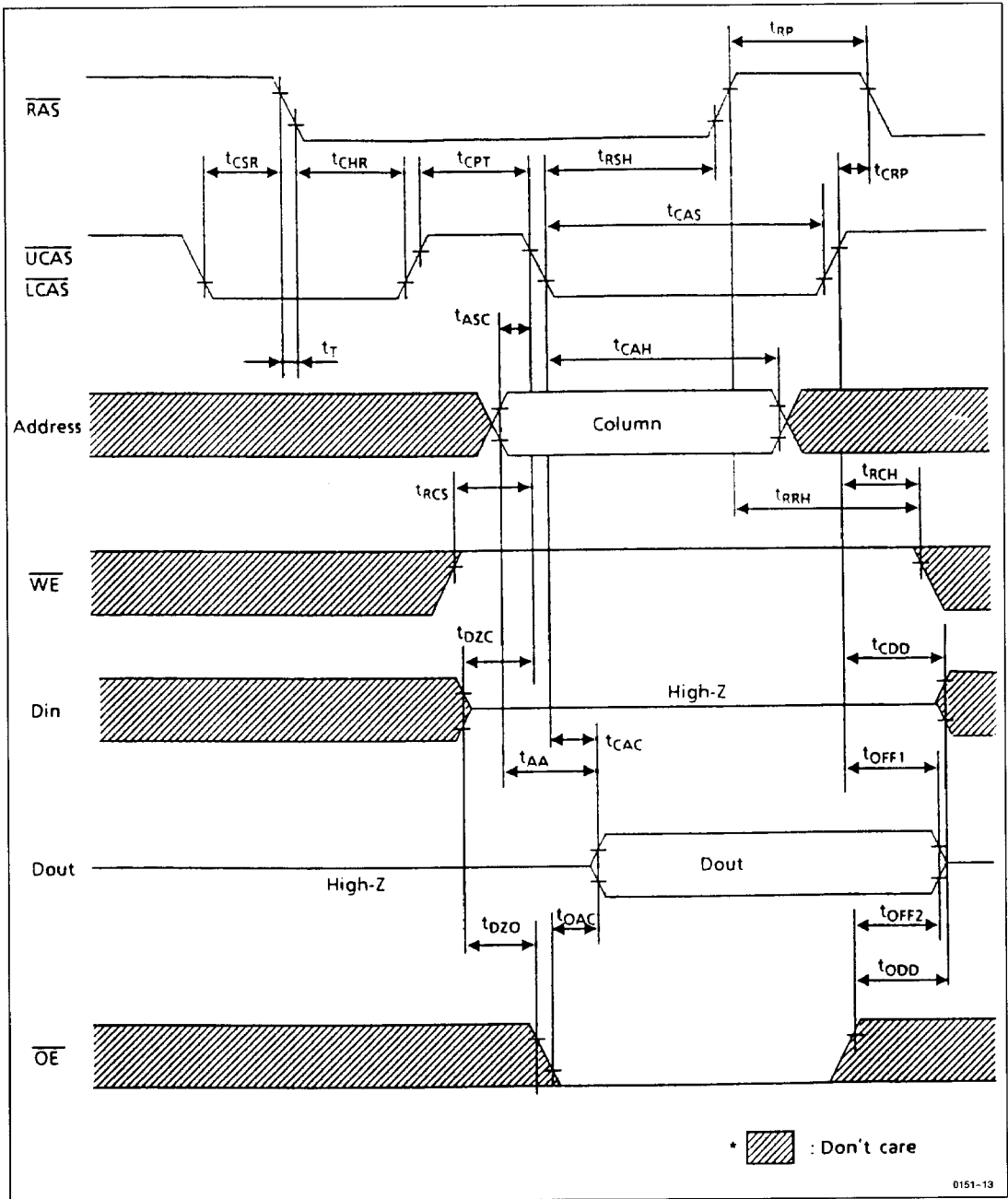
• Fast Page Mode Early Write Cycle





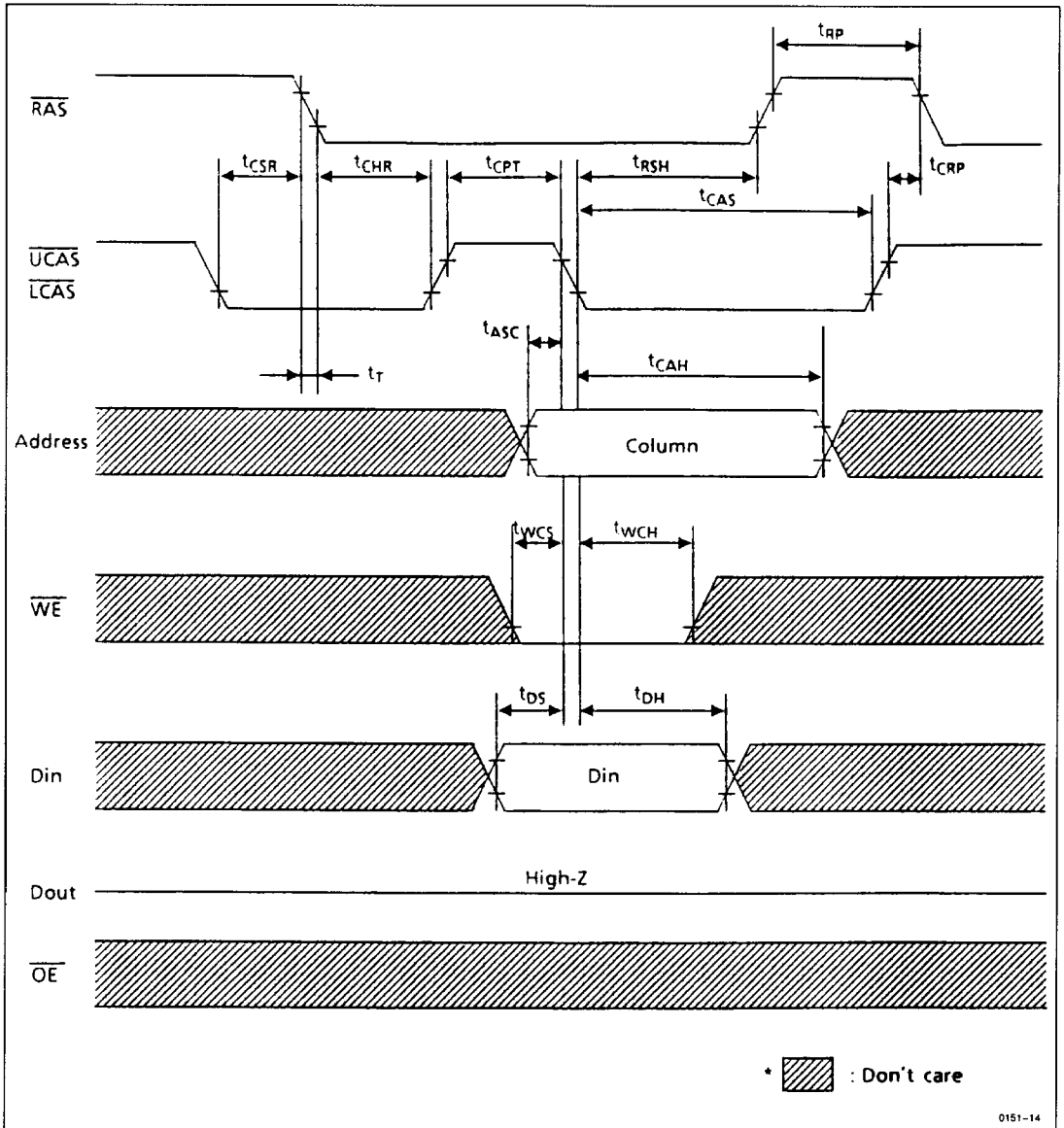


• CAS Before RAS Refresh Counter Check Cycle (Read)





• CAS Before RAS Refresh Counter Check Cycle (Write)



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