Motherboard Frequency Generator

Features

- AV9129 - 28 pin direct replacement for AV9127
- AV9128 - 20 pin version for space-critical applications
- Four independent clock generators
- Skew controlled outputs on AV9129
- Smooth frequency transitions
- Power down options
- Tri-state outputs
- Up to 11 output clocks
- On-chip loop filter components
- Can generate clocks up to 100 MHz
- 14.318 MHz oscillator circuitry
- 28 pin PDIP or SOIC package - AV9129
- 20 pin PDIP or SOIC package - AV9128

Applications

Desktop Computers/Workstations: The AV9128/9 can provide all of the necessary clocks for the motherboard, replacing crystals and oscillators, and can be a single chip solution for all different speeds and types of processors used. The AV9129 has up to five synchronized outputs that are skew controlled to within 1ns (typical) for the processor clock (Clock#2), making it ideal for high speed 386, 486 and RISC systems. The AV9129-06 and AV9129-23 are standard parts available to all customers.

Laptop/Notebook Computers: The AV9128/9 is the ideal solution for generating clocks in portables. The user can save power by running the processor clock at lower frequencies, depending on the task being performed. The AV9128/9 further reduces the current consumption by having the ability to completely shut down the individual clocks when not in use. Standard parts with power down for portable computers include the AV9129-08, AV9128-22, and AV9128-24.

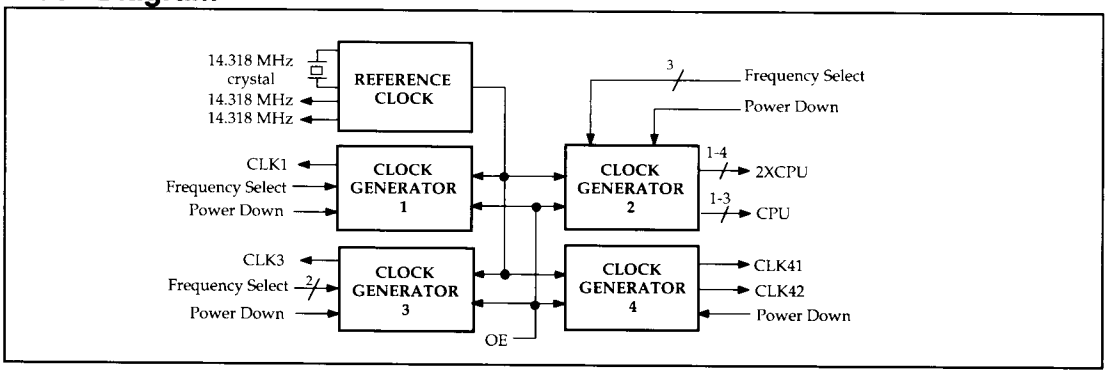
General Description

The AV9128/9 is designed to generate clocks for all 8088, 286, 386, 486, and RISC based motherboards, including laptops and notebook computers. The only external components required are an input crystal and decoupling capacitors. High performance applications may also require high speed clock termination components. The chip includes four independent clock generators plus the reference crystal oscillator clock to produce all necessary frequencies, including master clock, CPU clock, twice CPU clock frequency, keyboard clock, floppy disk controller clock, serial communications clock and bus clocks. Different frequencies from Clocks #1, #2 and #3 can be selected using the frequency select pins.

The frequencies and power down options in the AV9128/9 are mask programmable. Customer specific masks can be made and prototypes delivered within 6-8 weeks from receipt of order. ICS also offers standard versions such as those described in this data sheet.

The chip has multiple output buffers on key clocks to allow for improved EMI performance by isolating clocks going to different parts of the board, and thereby reducing the possibility of reflections. The chip provides slower clock edges compared to oscillators, further helping EMI.

Block Diagram

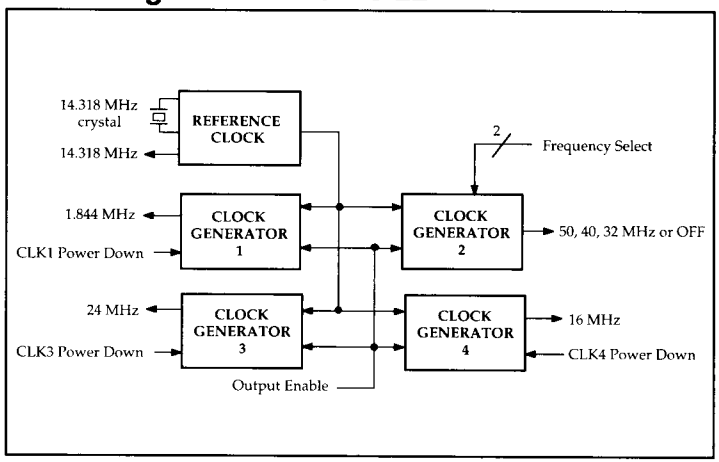


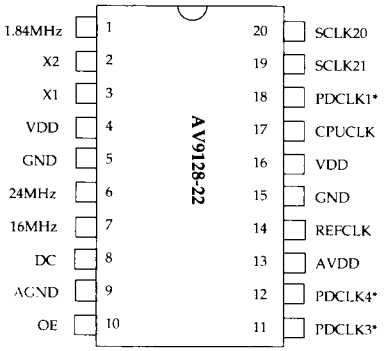
Pin Description for AV9128-22 (when using a 14.318MHz reference)

Pin Name	Pin #	Pin type	Description
CLK1	1	Output	CLOCK1. (1.84 MHz)
X2	2	Output	CRYSTAL connection for 14.318 MHz crystal
X1 / ICLK	3	Input	CRYSTAL connection for 14.318 MHz crystal or CLOCK INPUT
VDD	4	-	POWER SUPPLY (+5V)
GND	5	-	GROUND
CLK3	6	Output	CLOCK3 output (24 MHz)
CLK4	7	Output	CLOCK4 output (16 MHz)
DC	8	-	Don't Connect this pin
AGND	9	-	ANALOG GROUND
OE	10	Input	OUTPUT ENABLE. A low level tri-states all outputs. Note 1
PDCLK3*	11	Input	POWER DOWN. Powers down CLOCK3 when low
PDCLK4*	12	Input	POWER DOWN. Powers down CLOCK4 when low
AVDD	13	-	ANALOG POWER SUPPLY (+5V)
REFCLK	14	Output	REFERENCE CLOCK. Produces a 14.318 MHz clock
GND	15	-	GROUND
VDD	16	-	POWER SUPPLY (+5V)
CPUCLK	17	Output	CPU CLOCK. (see table)
PDCLK1*	18	Input	POWER DOWN. Powers down CLOCK1 when low
SCLK21	19	Input	CLOCK2 frequency SELECT 1
SCLK20	20	Input	CLOCK2 frequency SELECT 0

Note 1: Has internal pull-up resistor on this pin

Block Diagram for AV9128-22





D

Decoding Tables for AV9128-22
(using 14.318 MHz input. Actual frequencies shown, in MHz)

CLOCK#1

CLK1 (Pin 1)
1.844

CLOCK#3

CLK3 (Pin 6)
23.71

CLOCK#2

SCLK21 (Pin 19)	SCLK20 (Pin 20)	CPUCLK (Pin 17)
0	0	OFF
0	1	32.21
1	0	40.00
1	1	50.11

CLOCK#4

CLK4 (Pin 7)
16.00

REFERENCE CLOCK

REFCLK (Pin 14)
14.318

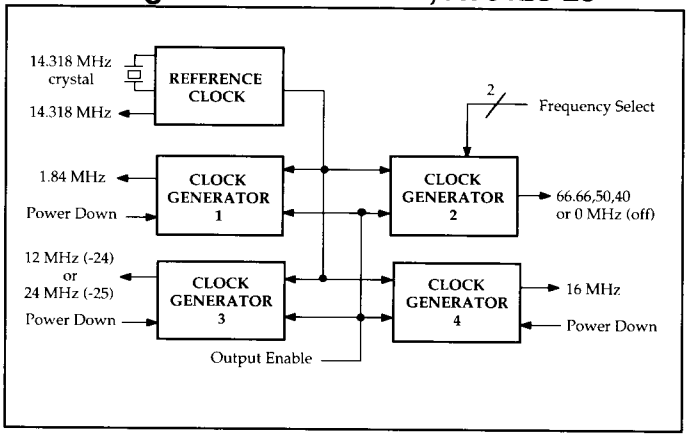
When all 4 clocks are powered down, the 14.318 MHz reference clock automatically powers down.

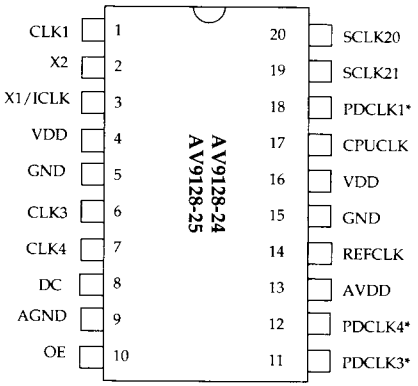
Pin Description for AV9128-24 and -25 (when using a 14.318MHz reference)

Pin Name	Pin #	Pin type	Description
CLK1	1	Output	CLOCK1 (1.84 MHz)
X2	2	Output	CRYSTAL connection for 14.318 MHz crystal. NC for clock input
X1/ICLK	3	Input	CRYSTAL connection or INPUT CLOCK
VDD	4	-	POWER SUPPLY (+5V)
GND	5	-	GROUND
CLK3	6	Output	CLOCK3 (12 MHz on AV9128-24, 24 MHz on AV9128-25)
CLK4	7	Output	CLOCK4 output (16 MHz)
DC	8	-	Don't Connect this pin
AGND	9	-	ANALOG GROUND
OE	10	Input	OUTPUT ENABLE. A low level tri-states all outputs. Note 1
PDCLK3*	11	Input	POWER DOWN. Powers down CLOCK3 when low
PDCLK4*	12	Input	POWER DOWN. Powers down CLOCK4 when low
AVDD	13	-	ANALOG POWER SUPPLY (+5V)
REFCLK	14	Output	REFERENCE CLOCK. Produces a 14.318 MHz clock.
GND	15	-	GROUND
VDD	16	-	POWER SUPPLY (+5V)
CPUCLK	17	Output	CPU CLOCK2 output (see table on following page)
PDCLK1*	18	Input	POWER DOWN. Powers down CLOCK1 when low
SCLK21	19	Input	CLOCK2 frequency SELECT 1
SCLK20	20	Input	CLOCK2 frequency SELECT 0

Note 1: Has internal pull-up resistor

Block Diagram for AV9128-24, AV9128-25





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Decoding Tables for AV9128-24, AV9128-25 (using 14.318 MHz input. Actual frequencies shown, in MHz)

CLOCK#1

CLK1 (Pin 1)
1.844

CLOCK#3

CLK3 (Pin 6)
11.86 or 23.71

CLOCK#2

SCLK21 (Pin 19)	SCLK20 (Pin 20)	CPUCLK (Pin 17)
0	0	OFF
0	1	40.00
1	0	50.11
1	1	66.58

CLOCK#4

CLK4 (Pin 7)
16.00

REFERENCE CLOCK

REFCLK (Pin 14)
14.318

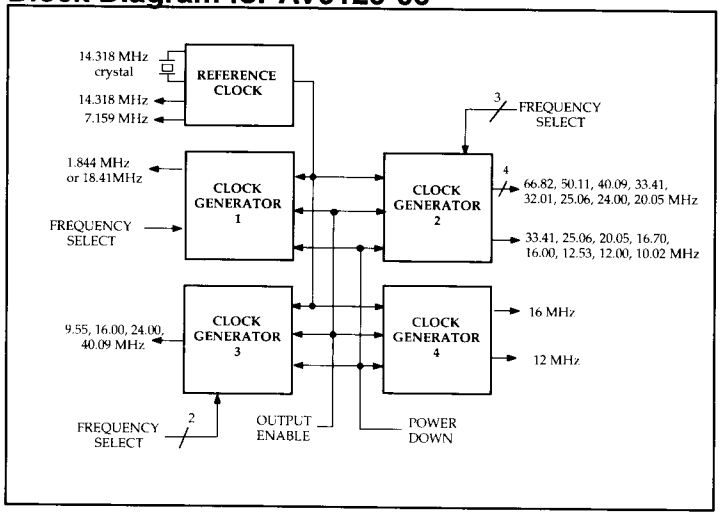
When all 4 clocks are powered down, the 14.318 MHz reference clock automatically powers down.

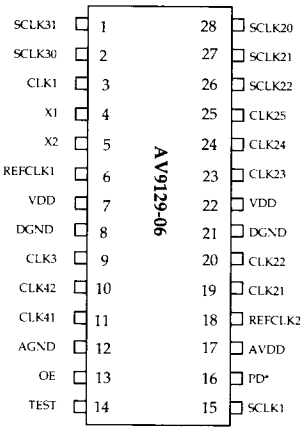
Pin Description for AV9129-06 (when using a 14.318MHz reference)

Pin Name	Pin #	Pin type	Description
SCLK31	1	Input	CLOCK3 frequency SELECT 1
SCLK30	2	Input	CLOCK3 frequency SELECT 0
CLK1	3	Output	CLOCK1 output
X1	4	Input	CRYSTAL connection for 14.318 MHz crystal, or input clock
X2	5	Output	CRYSTAL connection for 14.318 MHz crystal
REFCLK1	6	Output	REFERENCE CLOCK output #1. Produces 14.318 MHz clock
VDD	7	-	DIGITAL POWER SUPPLY (+5V)
DGND	8	-	DIGITAL GROUND
CLK3	9	Output	CLOCK3 output
CLK42	10	Output	CLOCK4 output #2
CLK41	11	Output	CLOCK4 output #1
AGND	12	-	ANALOG GROUND
OE	13	Input	OUTPUT ENABLE. A low tri-states the output clocks. Note 1
TEST	14	-	TEST. Connect to VDD or can be left floating. Note 1
SCLK1	15	Input	CLOCK1 frequency SELECT. Note 1
PD*	16	Input	POWER DOWN. A low shuts down all 4 clock generators. Note 1
AVDD	17	-	ANALOG POWER SUPPLY (+5V DC)
REFCLK2	18	Output	REFERENCE CLOCK output #2. Produces 7.159 MHz clock
CLK21	19	Output	CLOCK2 output #1
CLK22	20	Output	CLOCK2 output #2
DGND	21	-	DIGITAL GROUND
VDD	22	-	DIGITAL POWER SUPPLY (+5V)
CLK23	23	Output	CLOCK2 output #3
CLK24	24	Output	CLOCK2 output #4
CLK25	25	Output	CLOCK2 output #5
SCLK22	26	Input	CLOCK2 frequency SELECT 2
SCLK21	27	Input	CLOCK2 frequency SELECT 1
SCLK20	28	Input	CLOCK2 frequency SELECT 0

Note 1: These pins have internal pull-up resistors to maintain complete functionality when used in an AV9127 socket

Block Diagram for AV9129-06





D

Decoding Tables for AV9129-06
(using 14.318 MHz input. Actual frequencies shown, in MHz)

CLOCK#1

SCLK1 (Pin 15)	CLK1 (Pin 3)
0	18.44
1	1.844

CLOCK#2

SCLK22 (Pin 26)	SCLK21 (Pin 27)	SCLK20 (Pin 28)	CLK22-5 (Pins 20,23-25)	CLK21 (Pin 19)
0	0	0	66.63	33.32
0	0	1	50.11	25.06
0	1	0	40.09	20.05
0	1	1	33.32	16.66
1	0	0	31.98	15.99
1	0	1	25.06	12.53
1	1	0	23.98	11.99
1	1	1	20.05	10.02

CLOCK#3

SCLK31 (Pin #1)	SCLK30 (Pin #2)	CLK3 (Pin #9)
0	0	9.62
0	1	15.97
1	0	23.86
1	1	39.86

CLOCK#4

CLK41 (Pin 11)	CLK42 (Pin 10)
16.00	12.00

REFERENCE CLOCK

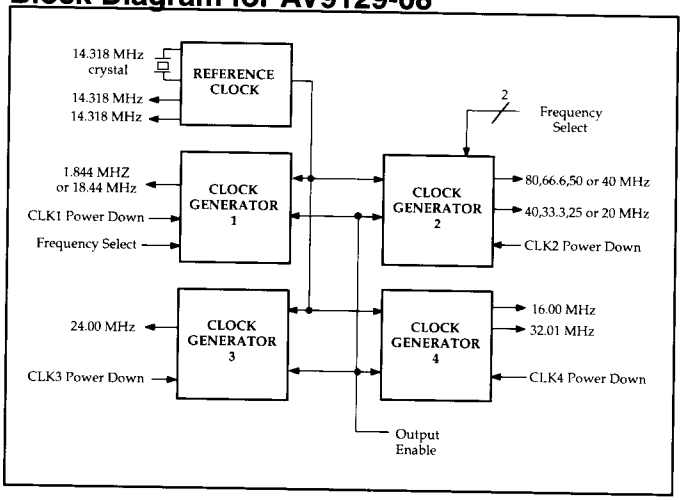
REFCLK1 (Pin 6)	REFCLK2 (Pin 18)
14.32	7.16

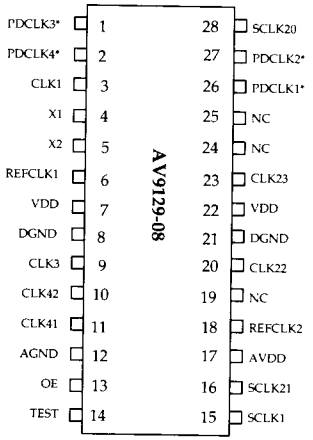
Pin Description for AV9129-08 (when using a 14.318MHz reference)

Pin Name	Pin #	Pin type	Description
PDCLK3*	1	Input	POWER DOWN CLOCK#3. Shuts off CLK3 when low
PDCLK4*	2	Input	POWER DOWN CLOCK#4. Shuts off CLK4 when low
CLK1	3	Output	CLOCK1 output
X1	4	Input	CRYSTAL connection for 14.318 MHz crystal, or input clock
X2	5	Output	CRYSTAL connection for 14.318 MHz crystal
REFCLK1	6	Output	REFERENCE CLOCK output #1. Produces 14.318 MHz clock
VDD	7	-	DIGITAL POWER SUPPLY (+5V)
DGND	8	-	DIGITAL GROUND
CLK3	9	Output	CLOCK3 output
CLK42	10	Output	CLOCK4 output #2
CLK41	11	Output	CLOCK4 output #1
AGND	12	-	ANALOG GROUND
OE	13	Input	OUTPUT ENABLE. A low tri-states the output clocks. Note 1
TEST	14	-	TEST. Connect to VDD or can be left floating. Note 1
SCLK1	15	Input	CLOCK1 frequency SELECT. Note 1
SCLK21	16	Input	CLOCK2 frequency SELECT 1. Note 1
AVDD	17	-	ANALOG POWER SUPPLY (+5V DC)
REFCLK2	18	Output	REFERENCE CLOCK output #2. Produces 14.318 MHz clock
NC	19	-	NO CONNECT
CLK22	20	Output	CLOCK2 output #2
DGND	21	-	DIGITAL GROUND
VDD	22	-	DIGITAL POWER SUPPLY (+5V)
CLK23	23	Output	CLOCK2 output #3
NC	24	-	NO CONNECT
NC	25	-	NO CONNECT
PDCLK1*	26	Input	POWER DOWN CLOCK#1. Shuts off CLK1 when low
PDCLK2*	27	Input	POWER DOWN CLOCK#2. Shuts off CLK2 when low
SCLK20	28	Input	CLOCK2 frequency SELECT 0

Note 1: These pins have internal pull-up resistors to maintain complete functionality when used in an AV9127 socket

Block Diagram for AV9129-08





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Decoding Tables for AV9129-08
(Using 14.318 MHz input. All frequencies in MHz)

REFCLK

PDCLK (1-4)*	REFCLK OUTPUT	REFCLK1 (Pin 6)	REFCLK2 (Pin 18)
0	OFF	LOW	LOW
1	ON	14.318	14.318

CLOCK#4

PDCLK4* (Pin 2)	CLK4 OUTPUTS	CLK41 (Pin 11)	CLK42 (Pin 10)
0	OFF	LOW	LOW
1	ON	32.00	16.00

CLOCK#1

PDCLK1* (Pin 26)	SCLK1 (Pin 15)	CLK1 OUTPUT	CLK1 (Pin 3)
0	X	OFF	LOW
1	0	ON	18.44
1	1	ON	1.844

CLOCK#3

PDCLK3* (Pin 1)	CLK3 OUTPUT	CLK3 (Pin 9)
0	OFF	LOW
1	ON	24.08

CLOCK#2

PDCLK2* (Pin 27)	SCLK21 (Pin 16)	SCLK20 (Pin 28)	CLK22, 23 (Pin 20,23)	CLK23 (Pin 23)	CLK 22 (Pin 20)
0	X	X	OFF	LOW	LOW
1	0	0	ON	80.05	40.03
1	0	1	ON	66.63	33.32
1	1	0	ON	50.11	25.06
1	1	1	ON	40.00	20.00

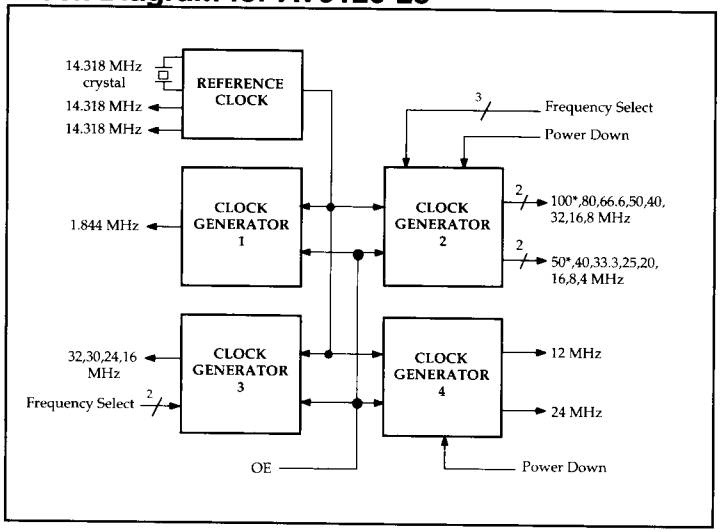
When PDCLK1*, PDCLK2*, PDCLK3*, and PDCLK4* all power down, the REFCLK automatically powers down.

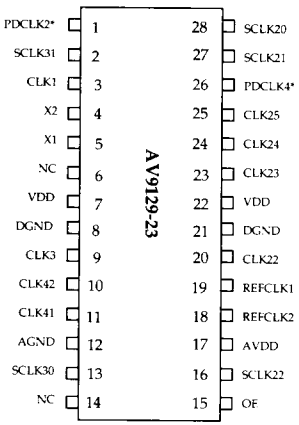
Pin Description for AV9129-23 (when using a 14.318MHz reference)

Pin Name	Pin #	Pin type	Description
PDCLK2*	1	Input	POWER DOWN. Powers down CLOCK2 when low. Note 1
SCLK31	2	Input	CLOCK3 frequency SELECT1. Note 1
CLK1	3	Output	CLOCK1 output (1.844 MHz)
X2	4	Output	CRYSTAL connection for 14.318 MHz crystal
X1	5	Input	CRYSTAL connection for 14.318 MHz crystal, or input clock
NC	6	-	NO CONNECT
VDD	7	-	DIGITAL POWER SUPPLY (+5V)
DGND	8	-	DIGITAL GROUND
CLK3	9	Output	CLOCK3 output
CLK42	10	Output	CLOCK4 output #2 (23.71 MHz)
CLK41	11	Output	CLOCK4 output #1 (11.86 MHz)
AGND	12	-	ANALOG GROUND
SCLK30	13	Input	CLOCK3 frequency SELECT0. Note 1
NC	14	-	TEST. Connect to VDD or can be left floating
OE	15	Input	OUTPUT ENABLE. All outputs are tri-stated when low. Note 1
SCLK22	16	Input	CLOCK2 frequency SELECT 2
AVDD	17	-	ANALOG POWER SUPPLY (+5V DC)
REFCLK2	18	Output	REFERENCE CLOCK output #2. Produces 14.318 MHz clock
REFCLK1	19	Output	REFERENCE CLOCK output #1. Produces 14.318 MHz clock
CLK22	20	Output	CLOCK2 output #2
DGND	21	-	DIGITAL GROUND
VDD	22	-	DIGITAL POWER SUPPLY (+5V)
CLK23	23	Output	CLOCK2 output #3
CLK24	24	Output	CLOCK2 output #4
CLK25	25	Output	CLOCK2 output #5
PDCLK4*	26	Input	POWER DOWN. Power down CLOCK4 when low. Note 1
SCLK21	27	Input	CLOCK2 frequency SELECT 1
SCLK20	28	Input	CLOCK2 frequency SELECT 0

Note 1: Has internal pull-up resistor on this pin

Block Diagram for AV9129-23





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Decoding Tables for AV9129-23
(using 14.318 MHz input. Actual frequencies shown, in MHz)

CLOCK#1

CLK1 (Pin 3)
1.844

CLOCK#2

SCLK22 (Pin 16)	SCLK21 (Pin 27)	SCLK20 (Pin 28)	CLK22,23 (Pins 20,23)	CLK24,25 (Pins 24,25)
0	0	0	7.50	3.75
0	0	1	15.51	7.75
0	1	0	32.22	16.11
0	1	1	40.09	20.04
1	0	0	50.11	25.05
1	0	1	66.54	33.27
1	1	0	80.18	40.09
1	1	1	100.23*	50.11*

CLOCK#3

SCLK31 (Pin 2)	SCLK30 (Pin 13)	CLK3 (Pin 9)
0	0	24.00
0	1	30.07
1	0	32.00
1	1	16.00

CLOCK#4

CLK41 (Pin 11)	CLK42 (Pin 10)
11.86	23.71

REFERENCE CLOCK

REFCLK1 (Pin 19)	REFCLK2 (Pin 18)
14.32	14.32

* The 1,1,1 selection does not guarantee a 100 MHz and 50 MHz output clock with the standard AV9129-23. If either of these clocks is desired, order the device as an AV9129-23Cx 28-100. The 100 MHz operation will be specially screened.

Absolute Maximum Ratings

AVDD, VDD referenced to GND..... 7V
Operating temperature under bias..... 0°C to +70°C
Storage temperature..... -40°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation..... 0.5 Watts

Note: Stresses above those listed under Absolute Maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect devices reliability.

Electrical Characteristics

(V_{DD} = +5V± 10%, T_A = 0°C to 70°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DC Characteristics						
V_{IL}	Input Low Voltage	-	-	0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0	-	-	V	V_{DD} = 5V
I_{IL}	Input Low Current	-	-	-5*	µA	V_{IN} = 0V
I_{IH}	Input High Current	-	-	5	µA	V_{IN} = V_{DD}
V_{OL}	Output Low Voltage	-	-	0.4	V	I_{OL} = 4mA
V_{OH}	Output High Voltage	V_{DD}-.4V	-	-	V	I_{OH} = -1mA,V_{DD}=5.0V
V_{OH}	Output High Voltage	V_{DD}-.8V	-	-	V	I_{OH} = -4mA,V_{DD}=5.0V
V_{OH}	Output High Voltage	2.4	-	-	V	1 I_{OH} = -8mA
I_{CC}	Supply Current	-	45		mA	No load, AV9129-06
F_D	Output Frequency Change over Supply and Temperature	-	0.005	0.05	%	With respect to typical frequency
I_{SC}	Short circuit current	25	40		mA	Each output clock
I_{CC}	Supply Current		30		mA	No load, AV9129-08
$I_{CCSTDBY}$	Standby Supply Current		50		µA	All Clocks off
R_{PU}	Pull-up resistor value		680		kΩ	Pins 13-16 AV9129
AC Characteristics						
t_{ICr}	Input Clock Rise Time	-	-	20	ns	
t_{ICf}	Input Clock Fall Time	-	-	20	ns	
t_r	Output Rise time, 0.8 to 2.0V	-	1	2	ns	25 pf load
t_r	Rise time, 20% to 80% V_{DD}	-	2	4	ns	25 pf load
t_f	Output Fall time, 2.0 to 0.8V	-	1	2	ns	25 pf load
t_f	Fall time, 80% to 20% V_{DD}	-	2	4	ns	25 pf load
d_t	Duty cycle	43/57	48/52	57/43	%	25 pf load
d_t	Duty cycle, reference clocks	40/60	43/57	60/40	%	25 pf load
t_{jls}	Jitter, one sigma		1	3	%	As compared with
t_{jab}	Jitter, absolute		2	5	%	clock period
f_i	Input Frequency	5	14.318	32	MHz	
T_{sk}	Clock skew between any Clock #2 outputs		1	1.5	ns	
t_{pu}	Power up time		5		ms	From off to 80 MHz

* Crystal input pin will be higher, typically -10µA

Notes:
1. All clocks on AV9129-06 running at highest possible frequencies. Power supply current can change substantially with different mask configurations (see Application Note AAN02).

Ordering Information

Part Number	Temperature Range	Package Type
AV9128-xxCN20	0°C to +70°C	20 lead Plastic DIP
AV9128-xxCW20	0°C to +70°C	20 lead SOIC
AV9129-xxCN28	0°C to +70°C	28 lead Plastic DIP (300 mils)
AV9129-xxCW28	0°C to +70°C	28 lead SOIC

Note: The dash number following AV9128/9, (denoted by xx above) must be included when ordering product, since it specifies the options being ordered. For 100 Mhz devices, add -100 MHz to part number.