Integrated Device Technology, Inc.

128KB SECONDARY CACHE MODULE FOR THE INTEL® i486™

IDT7MB6098A

FEATURES

- Pin compatible with the Intel 485TurboCache™ 82485MB
- 128KB direct mapped, write-through, non-sectored, zero-wait-state secondary cache module
- Ideal for use with i486-based systems with an Intel 485TurboCache socket
- Uses IDT71589 32K x 9 CacheRAM™ with burst counter and self-timed write IDT71B74 cache-tag RAM and cache control ASIC
- Operates with external i486 speeds of up to 33MHz
- Concurrent snooping is supported
- 485TurboCache write-protect strap feature is not supported
- 113 lead FR-4 QIP (Quad in-Line Package)
- Single 5V (±5%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL-compatible
- For SIMM package version refer to the IDT7MP6104
- For 256KB version refer to the IDT7MP6105

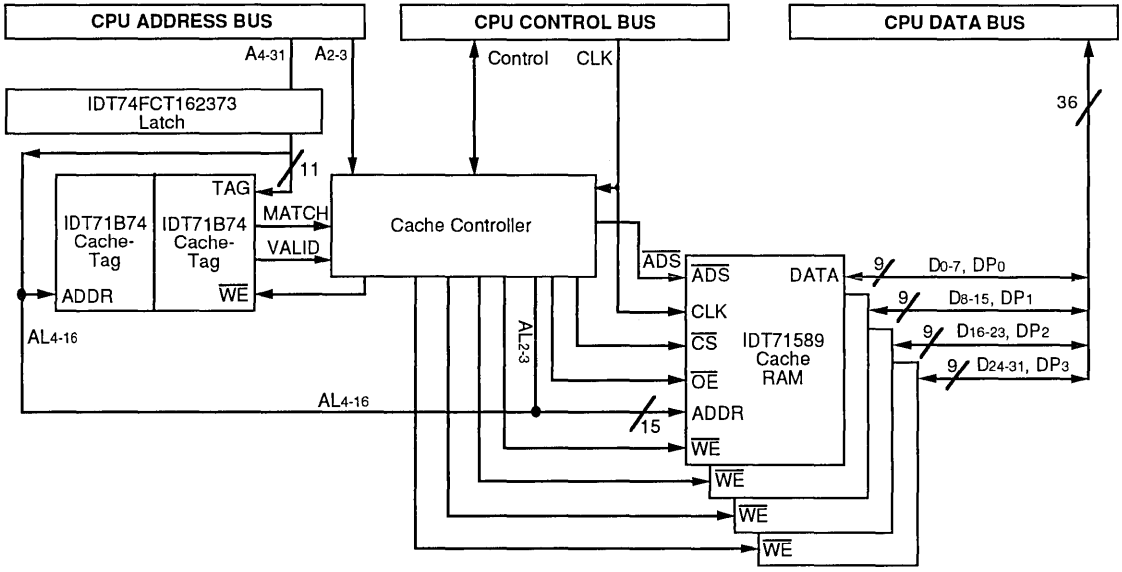
DESCRIPTION

The IDT7MB6098A is a pin-compatible replacement for the Intel 485TurboCache 82485MB. The module is a 128KB direct-mapped, write-through, non-sectored, zero-wait-state secondary cache and is ideal for use with many i486-based systems that have an Intel 485TurboCache socket. The IDT7MB6098A uses four IDT71589 32K x 9 CacheRAMs, two IDT71B74 8K x 8 cache-tag RAMs and two IDT74FCT162373 Double-Density™ 16-bit latches in plastic surface mount packages mounted on a multilayer epoxy laminate (FR-4) board along with an ASIC based cache controller. Extremely high speeds are achieved using IDT's high-performance, high-reliability BiCMOS and CMOS technologies.

The quad in-line package (QIP) package configuration allows 113 leads to be placed on a package 2.9" long by 2.0" wide and 0.280" tall. SIMM package versions are available, please refer to the IDT7MP6104 datasheet. For 256KB upgrade to the IDT7MP6104, refer to the IDT7MP6105.

Multiple GND pins and on-board decoupling capacitors provide maximum noise protection. All inputs and outputs of the IDT7MB6098A are TTL-compatible and operate from a single 5V power supply.

FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATION[1]

GND	A1	•	•	A2	RESET	$\overline{CS}$	A4	•	•	A5	GND
CLK	B1	•	•	B2	M/$\overline{IO}$	$\overline{CRDY}$	B4	•	•	B5	$\overline{CKEN}$
RESV	C1	•	•	C2	$\overline{FLUSH}$	$\overline{CBRDY}$	C4	•	•	C5	$\overline{BRDYO}$
$\overline{BLAST}$	D1	•	•	D2	$\overline{EADS}$	VCC	D4	•	•	D5	$\overline{SKEN}$
$\overline{BOFF}$	E1	•	•	E2	VCC	WP	E4	•	•	E5	$\overline{START}$
$\overline{ADS}$	F1	•	•	F2	W/$\overline{R}$	D0	F4	•	•	F5	GND
GND	G1	•	•	G2	NC[2]	D2	G4	•	•	G5	D1
$\overline{BE0}$	H1	•	•	H2	$\overline{BE1}$	GND	H4	•	•	H5	D3
$\overline{BE2}$	I1	•	•	I2	$\overline{BE3}$	D5	I4	•	•	I5	D4
A2	J1	•	•	J2	GND	D7	J4	•	•	J5	D6
VCC	K1	•	•	K2	A3	D8	K4	•	•	K5	GND
A4	L1	•	•	L2	A5	D10	L4	•	•	L5	D9
A6	M1	•	•	M2	A7	VCC	M4	•	•	M5	D11
A9	N1	•	•	N2	A8	D13	N4	•	•	N5	D12
A10	O1	•	•	O2	VCC	D15	O4	•	•	O5	D14
GND	P1	•	•	P2	A11	DP0	P4	•	•	P5	GND
A31	Q1	•	•	Q2	A12	D16	Q4	•	•	Q5	DP1
A14	R1	•	•	R2	A13	GND	R4	•	•	R5	D17
A15	S1	•	•	S2	GND	D19	S4	•	•	S5	D18
A17	T1	•	•	T2	A16	D21	T4	•	•	T5	D20
A19	U1	•	•	U2	A18	D22	U4	•	•	U5	VCC
VCC	V1	•	•	V2	A20	D24	V4	•	•	V5	D23
A22	W1	•	•	W2	A21	GND	W4	•	•	W5	D25
A23	X1	•	•	X2	VCC	D27	X4	•	•	X5	D26
A25	Y1	•	•	Y2	A24	D29	Y4	•	•	Y5	D28
A27	Z1	•	•	Z2	A26	D30	Z4	•	•	Z5	D31
A29	AA1	•	•	AA2	A28	DP2	AA4	•	•	AA5	DP3
GND	BB1	•	•	BB2	A30	$\overline{PRSN}$ BB3	•	VCC	BB4	•	•	BB5	GND

QIP
TOP VIEW

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NOTE:
1. Pin G2 is $\overline{WPSTRP}$ on the Intel 485Turbocache. This signal is not used by the IDT7MB6098A and is N.C. (No Connect).

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–10 to +85	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

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NOTE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 5%

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RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0.0	0.0	0.0	V
VIH	Input HIGH Votage	2.2	—	6.0	V
VIL	Input LOW Voltage	–0.5[1]	—	0.8	V

NOTE:
1. VIL = –3.0V for pulse width less than 5ns.

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CAPACITANCE[1]

(TA = +25°C, f = 1.0 MHz)

Symbol	Parameter[1]	Condition	Max.	Unit
CIN	Input Capacitance (Address, Control)	VIN = 0V	15	pF
CIN	Input Capacitance (Clock)	VIN = 0V	45	pF
COUT	Output Capacitance (Control)	VIN = 0V	15	pF
CI/O	Data I/O Capacitance	VOUT = 0V	10	pF

NOTE:
1. These parameters are guaranteed by design but not tested.

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PIN DESCRIPTION

Symbol	Parameter	Type	Active	Description
CLK	Clock	Input	N/A	This input is the timing reference for all of the IDT7MB6098A's functions. It is the same as the i486 CLK input.
RESET	Reset Cache	Input	HIGH	A synchronous positive-true reset input, which invalidates all cache locations and resets the cache control logic.
$\overline{ADS}$	Address Strobe	Input	LOW	$\overline{ADS}$ is connected to the ADS# pin of the i486 CPU. It is used by the IDT7MB6098A to start any read or write cycle. $\overline{CS}$ must be asserted for $\overline{ADS}$ to be recognized.
M/$\overline{IO}$	Memory/IO	Input	N/A	This pin is used by the i486 to indicate whether the current cycle is a memory or I/O cycle. I/O cycles are not cacheable by the IDT7MB6098A.
W/$\overline{R}$	Write/Read	Input	N/A	Write cycles are indicated by a HIGH level on this pin, and read cycles are indicated by a LOW level.
$\overline{START}$	Memory Start	Output	LOW	During a cache read miss cycle or a write cycle, the $\overline{START}$ pin signals that the main memory system should service the current access.
$\overline{BRDYO}$	Burst Ready Out	Output	LOW	This is the IDT7MB6098A's means of signaling to the i486 that cache data is ready to be sampled.
$\overline{CBRDY}$	Cache Burst Ready In	Input	LOW	This is the system input to the IDT7MB6098A to let the cache know that a main memory cache word is ready to be sampled by the CPU and the IDT7MB6098A during a burst access.
$\overline{CRDY}$	Cache Ready In	Input	LOW	This is the system input to the IDT7MB6098A to let the cache know that a main memory cache word is ready to be sampled by the CPU and the IDT7MB6098A during a non-burst access.
$\overline{BLAST}$	Burst Last	Input	LOW	This i486 output indicates to the IDT7MB6098A cache control logic that the current cycle is the last cycle of a burst access.
$\overline{BOFF}$	Backoff	Input	LOW	This signal is used to stall the IDT7MB6098A. The IDT7MB6098A will also put its data bus into a high-impedance state. The IDT7MB6098A will only recognize invalidation cycles when $\overline{BOFF}$ is asserted.
$\overline{PRSN}$	Presence	Output	LOW	This pin is hardwired to ground. It tells the system logic that the IDT7MB6098A is plugged into the system.
A_2-A_{31}	Processor Addresses	Input	N/A	These are the address inputs to the IDT7MB6098A.
$\overline{BE_0}$-$\overline{BE_3}$	Byte Enable	Input	LOW	The byte enable inputs are sampled only during CPU write cycles and are only used to control byte writes to valid cache lines during write hit cycles. The timing is the same as for the address input pins.
$\overline{CS}$	Chip Select	Input	LOW	Chip select can be used for depth expansion. $\overline{CS}$ must be asserted for $\overline{EADS}$ or $\overline{ADS}$ to be recognized by the IDT7MB6098A.
D_0-D_{31}	Processor Data Lines	I/O	N/A	These are the data inputs from either the i486 or the system memory. D_0-D_7 define the least significant byte while D_{24}-D_{31} define the most significant byte.
DP_0-DP_3	Data Parity	I/O	N/A	These are the parity bits from either the i486 or the system memory. The timing requirements are the same as the data lines.
$\overline{CKEN}$	Cache Enable To CPU	Output	LOW	This signal is the cache enable signal generated by the IDT7MB6098A. The IDT7MB6098A will always assert $\overline{CKEN}$ during T1 cycles and during read hit cycles before the last $\overline{BRDYO}$. The IDT7MB6098A will not assert $\overline{CKEN}$ during read miss cycles.
$\overline{SKEN}$	System Cache Enable	Input	LOW	This signal is generated by the system to indicate that a line is cacheable. The IDT7MB6098A will look for $\overline{SKEN}$ to be asserted at least one cycle before the first word transfer and the cycle before the last word transfer of a line fill.
$\overline{FLUSH}$	Flush Cache	Input	LOW	This signal causes the IDT7MB6098A to invalidate its entire cache contents.
WP	Write Protect	Input	HIGH	The write protect input is only sampled during the third transfer of a line fill. If a line is flagged as write protected during a line fill, it is considered non-cacheable.
$\overline{WPSTRP}$	Write Protect Strap	N/A	N/A	This signal is not used by the IDT7MB6098A.
$\overline{EADS}$	Valid External Address	Input	LOW	This signal indicates that an invalidation address is present on the IDT7MB6098A address bus. $\overline{CS}$ must be asserted for $\overline{EADS}$ to be recognized by the IDT7MB6098A.

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FUNCTIONAL DESCRIPTION

Basic Operation

The IDT7MB6098A is a complete secondary cache subsystem designed to replace the Intel TurboCache485. The IDT7MB6098A is designed to support zero-wait-state line reads, i.e. four words of data in five clocks. The IDT7MB6098A supports all of the following bus cycles: read hit, read miss, write hit, write miss, invalidation and backoff. The IDT7MB6098A also features single pin reset and cache flush capabilities.

The IDT7MB6098A latches the address on the input of the module at the beginning of any read, write or invalidation cycle. The address remains latched for one cycle after the initiation of a read or write, and the address remains latched for two cycles after the initiation of an invalidation.

Reset

The IDT7MB6098A is reset when RESET is asserted. Asserting RESET will invalidate the entire contents of the cache, and reset the control logic of the cache. The cache will be reset regardless of the state of other control signals when RESET is asserted.

Flush

The entire cache contents of the IDT7MB6098A is invalidated when the $\overline{FLUSH}$ input is asserted. The cache will be invalidated regardless of the state of other control signals when $\overline{FLUSH}$ is asserted. $\overline{FLUSH}$ will not reset the cache control logic.

Read

The IDT7MB6098A recognizes the initiation of a read cycle when both $\overline{ADS}$ and $\overline{CS}$ are sampled LOW with M/$\overline{IO}$ HIGH and W/$\overline{R}$ LOW. As soon as the address is valid at the input of the module, the IDT7MB6098A begins its tag look-up. If the input address is not contained in the cache, then a miss has occurred, and the IDT7MB6098A will wait for the main memory system to service the current access. If the input address is present in the cache, then a hit has occurred, and the IDT7MB6098A will burst back a line of data to the CPU.

The IDT7MB6098A will not accept data returned in zero wait states. The earliest the IDT7MB6098A can accept data is the cycle after $\overline{START}$ is asserted.

The IDT7MB6098A will consider the data returned from the memory system as cacheable if $\overline{SKEN}$ is sampled LOW at least one cycle before $\overline{CBRDY}$ or $\overline{CRDY}$ is first asserted. The IDT7MB6098A will load the data word returned from the memory system into the cache each time $\overline{CBRDY}$ or $\overline{CRDY}$ is sampled LOW. If WP is sampled HIGH during the third word transfer of a line fill, the line is considered write protected, and the line of data is not validated. If the line is not write protected, the IDT7MB6098A will only validate the line of data returned from the memory system if $\overline{SKEN}$ is sampled LOW the cycle before the last data word is transferred from the memory system, i.e. the fourth time that $\overline{CBRDY}$ or $\overline{CRDY}$ is sampled LOW. The line fill is aborted if $\overline{BLAST}$ is sampled LOW concurrent with $\overline{CBRDY}$ or $\overline{CRDY}$ being sampled LOW prior to the last data word transfer.

The IDT7MB6098A will consider the data returned as non-cacheable if $\overline{CBRDY}$ or $\overline{CRDY}$ is sampled LOW before, or concurrently, with $\overline{SKEN}$ prior to the first word transfer. Therefore, to avoid a potential performance penalty, $\overline{SKEN}$ should not be asserted prior to $\overline{CBRDY}$ or $\overline{CRDY}$ if the data is considered non-cacheable, since the IDT7MB6098A will invalidate a line of data if $\overline{SKEN}$ is sampled LOW before $\overline{CBRDY}$ or $\overline{CRDY}$ is sampled LOW during a read miss.

The IDT7MB6098A requires that the read miss address (i.e. the address that was valid at the beginning of the read cycle) is present when $\overline{SKEN}$ is sampled LOW at the beginning of a line fill and again when $\overline{SKEN}$ is sampled at the end of a line fill. The address must be valid because it is latched at these times to invalidate a line at the beginning of the fill and then to validate the line at the end of the line fill. When the address is latched at the end of the line fill, it will remain latched until the last data word of the line is written to the cache.

If the IDT7MB6098A detects that the input address is contained in the cache, the IDT7MB6098A will supply data to the CPU. The IDT7MB6098A starts bursting data back to the CPU in the first T2 cycle. The IDT7MB6098A then transfers a new data word in each subsequent T2 cycle until $\overline{BLAST}$ is asserted to the cache. The IDT7MB6098A also forces $\overline{START}$ HIGH and $\overline{BRDYO}$ LOW in the first T2 cycle. $\overline{CKEN}$ is asserted during the T1 cycle and again in the second, and subsequent, T2 cycles during a read hit.

Write

The IDT7MB6098A recognizes the initiation of a write cycle when both $\overline{ADS}$ and $\overline{CS}$ are sampled LOW with M/$\overline{IO}$ HIGH and W/$\overline{R}$ HIGH. As soon as the address is valid at the input of the module, the IDT7MB6098A begins its tag look-up. If the input address is contained in the cache, then a write hit has occurred, and the cache contents are updated when $\overline{CRDY}$ or $\overline{CBRDY}$ is returned from the system. The IDT7MB6098A requires the address to be valid in the cycle that the data is written to the cache, i.e. when $\overline{CRDY}$ or $\overline{CBRDY}$ is returned from the system; this requirement should have no impact at the system level since the i486 will maintain both the address and data on its outputs until the write cycle is completed. If the input address is not contained in the cache, then a write miss has occurred, the IDT7MB6098A ignores the write, and the cache contents are not updated. For both write hits and write misses the IDT7MB6098A will assert $\overline{START}$ until $\overline{CRDY}$ or $\overline{CBRDY}$ is returned from the system.

Invalidation

An invalidation is initiated by the simultaneous assertion of $\overline{EADS}$ and $\overline{CS}$. If $\overline{EADS}$ and $\overline{ADS}$ are asserted simultaneously, $\overline{ADS}$ is ignored since invalidations have priority. At the initiation of an invalidation, the IDT7MB6098A begins its tag look-up. If the line is found in the cache, the line will be invalidated. The IDT7MB6098A requires two cycles after the assertion of $\overline{EADS}$ to invalidate a line; therefore, invalidations can only occur every third cycle. The IDT7MB6098A ignores invalidations only if an address is currently latched in the address latch. Therefore, the IDT7MB6098A ignores invalidations at the following times: the cycle after the initiation of a read or write cycle, the cycle after $\overline{SKEN}$ is first sampled LOW

during a line fill, the cycle(s) after sampling $\overline{SKEN}$ LOW concurrent with (or after) the third word transfer and prior to the fourth word transfer of a line fill, and the two cycles following a previous invalidation.

Backoff

A cache backoff is initiated by the assertion of $\overline{BOFF}$. $\overline{BOFF}$ interrupts any other cache cycle that the IDT7MB6098A is servicing. The cycle after $\overline{BOFF}$ is sampled LOW, the IDT7MB6098A will float its data bus, and the output control signals are driven to their idle levels, i.e. $\overline{CKEN}$ LOW, $\overline{START}$ HIGH and $\overline{BRDYO}$ HIGH. When $\overline{BOFF}$ is asserted, the IDT7MB6098A ignores all cache cycles except for invalidations; however, the IDT7MB6098A will still recognize the assertion of RESET or $\overline{FLUSH}$ when $\overline{BOFF}$ is asserted.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (Address, Data, Control)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LI}\|$	Input Leakage Current (Clock)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	50	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	10	µA
V_{OLD}	Output LOW Voltage (Data)	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OLC}	Output LOW Voltage (Control)	I_{OL} = 12mA, V_{CC} = Min.	—	0.5	V
V_{OHD}	Output HIGH Voltage (Data)	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V
V_{OHC}	Output HIGH Voltage (Control)	I_{OH} = –2mA, V_{CC} = Min.	2.4	—	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max., $\overline{CS} \le V_{IL}$, f = f_{MAX}, Outputs Open	—	1350	mA

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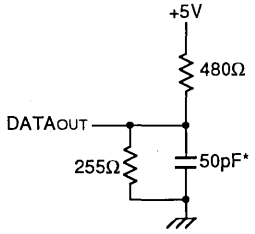
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2897 tbl 07



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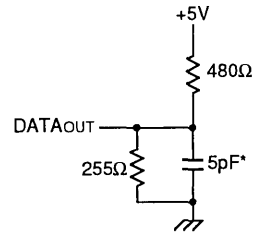
*including scope and jig

Figure 1. Output Load



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*including scope and jig

Figure 2. Output Load (for t_{OHZ}, t_{CHZ}, t_{OLZ} and t_{CLZ})

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 0° to +70°C)

Symbol	Parameter	7MB6098SA33K		Unit
		Min.	Max.	
t_1	Clock Period	30	—	ns
t_2	Clock HIGH Time	11	—	ns
t_3	Clock LOW Time	11	—	ns
t_4	A_2-A_{31}, $\overline{BE_0}$-$\overline{BE_3}$ Set-up Time	13	—	ns
t_5	A_2-A_{31}, $\overline{BE_0}$-$\overline{BE_3}$ Hold Time	10	—	ns
t_6	A_4-A_{31} Line Fill Set-up Time	5	—	ns
t_7	$\overline{ADS}$, M/$\overline{IO}$, W/$\overline{R}$ Set-up Time	13	—	ns
t_8	$\overline{ADS}$, M/$\overline{IO}$, W/$\overline{R}$ Hold Time	3	—	ns
t_9	$\overline{BLAST}$, $\overline{CS}$ Set-up Time	9	—	ns
t_{10}	$\overline{BLAST}$, $\overline{CS}$ Hold Time	3	—	ns
t_{11}	$\overline{CRDY}$, $\overline{CBRDY}$ Set-up Time	11	—	ns
t_{12}	$\overline{CRDY}$, $\overline{CBRDY}$ Hold Time	3	—	ns
t_{13}	$\overline{SKEN}$ Set-up Time	9	—	ns
t_{14}	$\overline{SKEN}$ Hold Time	3	—	ns
t_{15}	D_0-D_{31}, DP_0-DP_3 Set-up Time	5	—	ns
t_{16}	D_0-D_{31}, DP_0-DP_3 Hold Time	3	—	ns
t_{17}	$\overline{EADS}$ Set-up Time	9	—	ns
t_{18}	$\overline{EADS}$ Hold Time	3	—	ns
t_{19}	A_4-A_{31} Set-up Time (Snoop)	6	—	ns
t_{20}	A_4-A_{31} Hold Time (Snoop)	10	—	ns
t_{21}	RESET, $\overline{FLUSH}$ Set-up Time	9	—	ns
t_{22}	RESET, $\overline{FLUSH}$ Hold Time	3	—	ns
t_{23}	RESET, $\overline{FLUSH}$ Pulse Width	80	—	ns
t_{24}	$\overline{BRDYO}$ Valid	—	16	ns
t_{25}	$\overline{CKEN}$ Valid	—	15	ns
t_{26}	$\overline{START}$ Valid	—	16	ns
t_{27}	D_0-D_{31}, DP_0-DP_3 Valid (Read Hit)	—	24	ns
t_{28}	WP Set-up Time	9	—	ns
t_{29}	WP Hold Time	3	—	ns
t_{30}	$\overline{BOFF}$ Set-up Time	9	—	ns
t_{31}	$\overline{BOFF}$ Hold Time	3	—	ns

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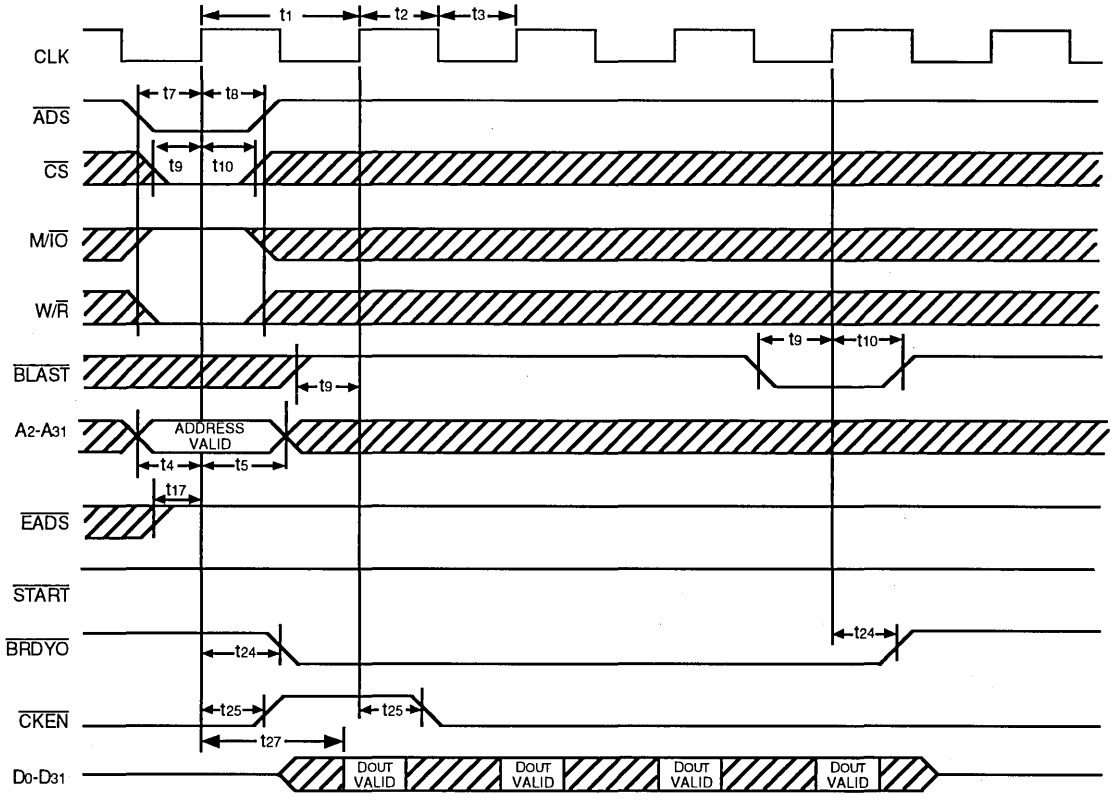
TIMING WAVEFORM OF A READ HIT CYCLE (READ LINE)(1)



NOTE:
1. RESET is held LOW, FLUSH is held HIGH, BOFF is held HIGH.

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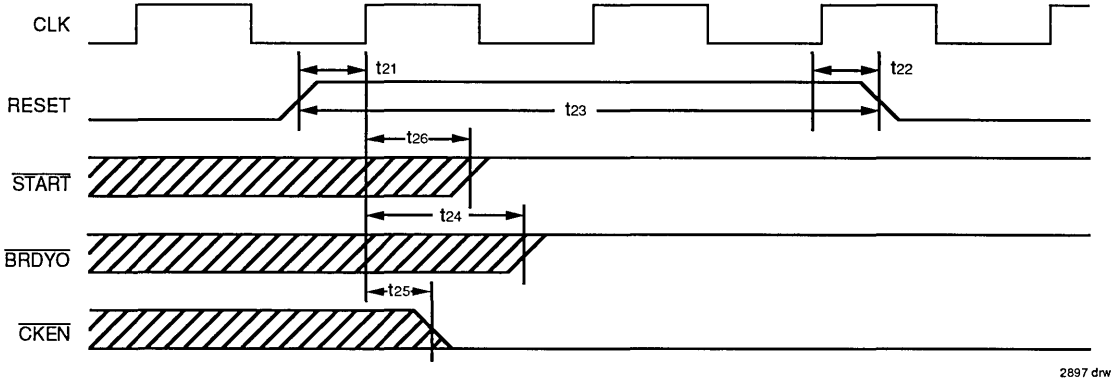
TIMING WAVEFORM OF A RESET OPERATION



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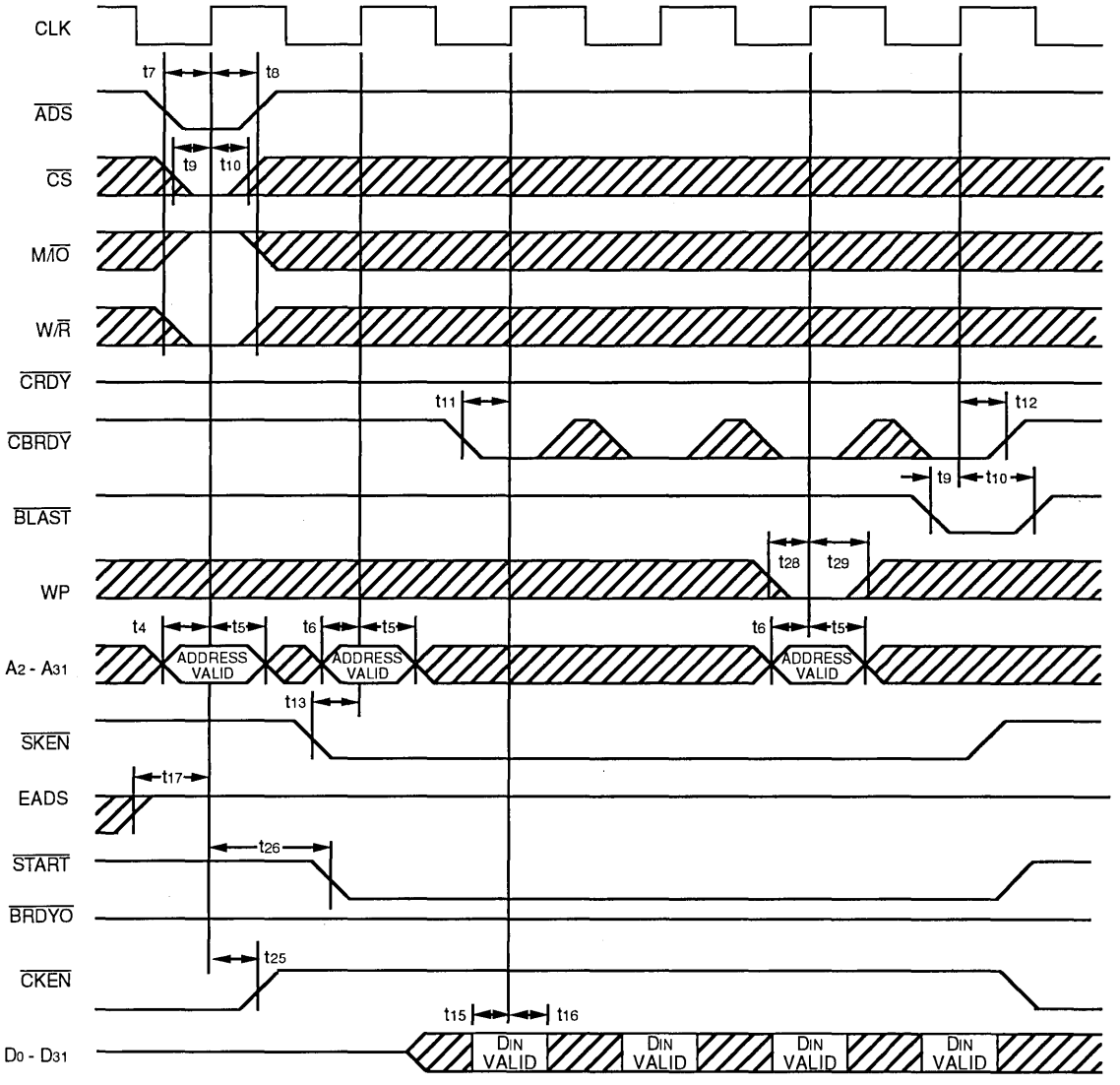
TIMING WAVEFORM OF A CACHEABLE BURST READ MISS CYCLE (WRITE LINE)(1)

(NON-WRITE PROTECTED)



NOTE:
1. RESET is held LOW, $\overline{FLUSH}$ is held HIGH, $\overline{BOFF}$ is held HIGH.

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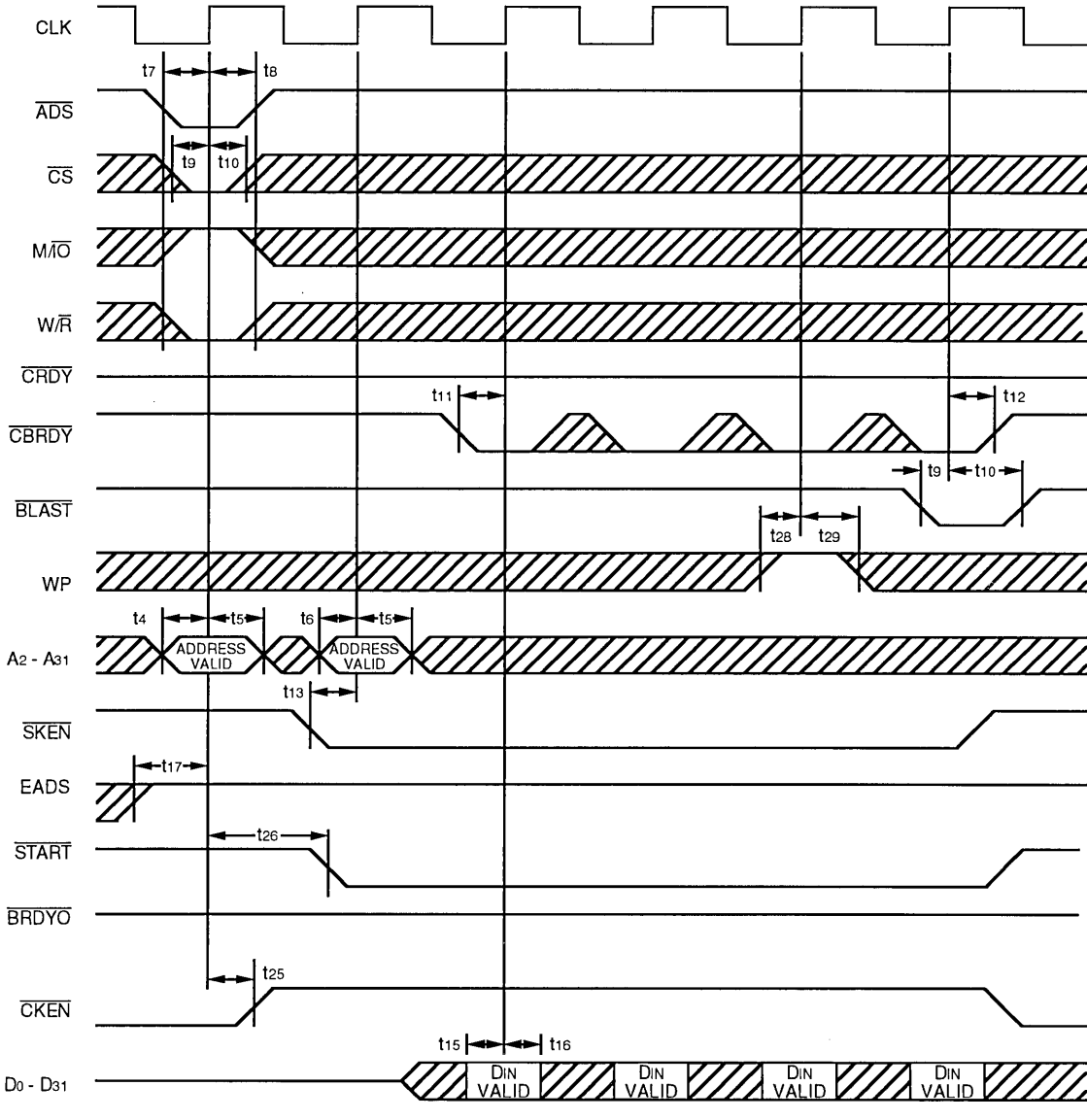
TIMING WAVEFORM OF A CACHEABLE BURST READ MISS CYCLE (WRITE LINE)[1]

(WRITE PROTECTED)

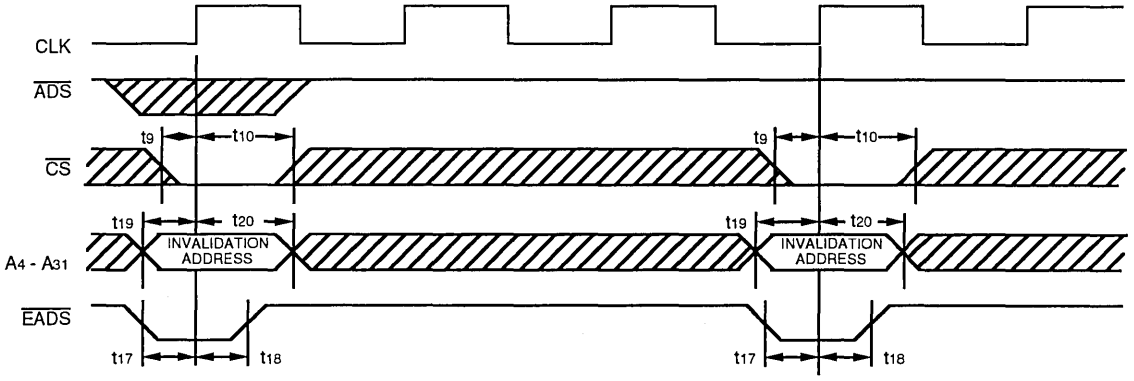


NOTE:

1. RESET is held LOW, $\overline{FLUSH}$ is held HIGH, $\overline{BOFF}$ is held HIGH.

2897 drw 08

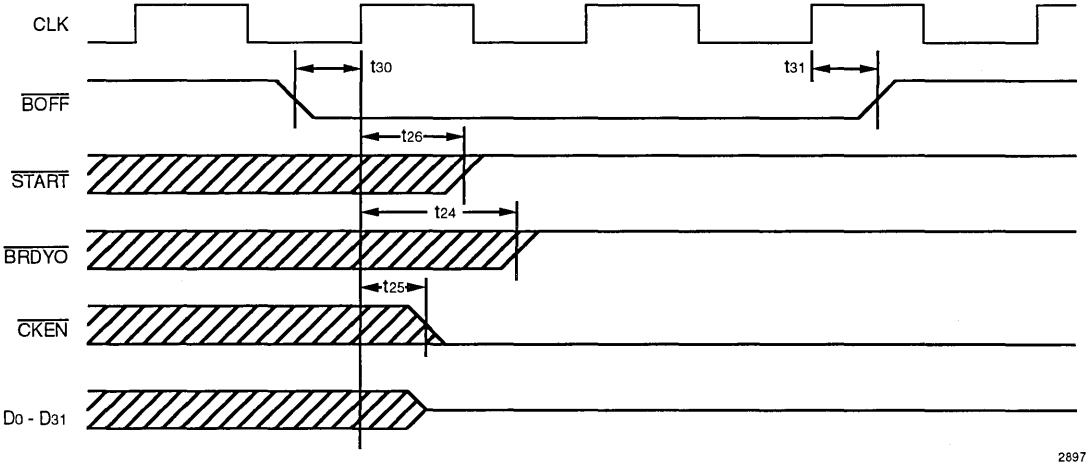
TIMING WAVEFORM OF A CACHE INVALIDATION(1)



2897 drw 09

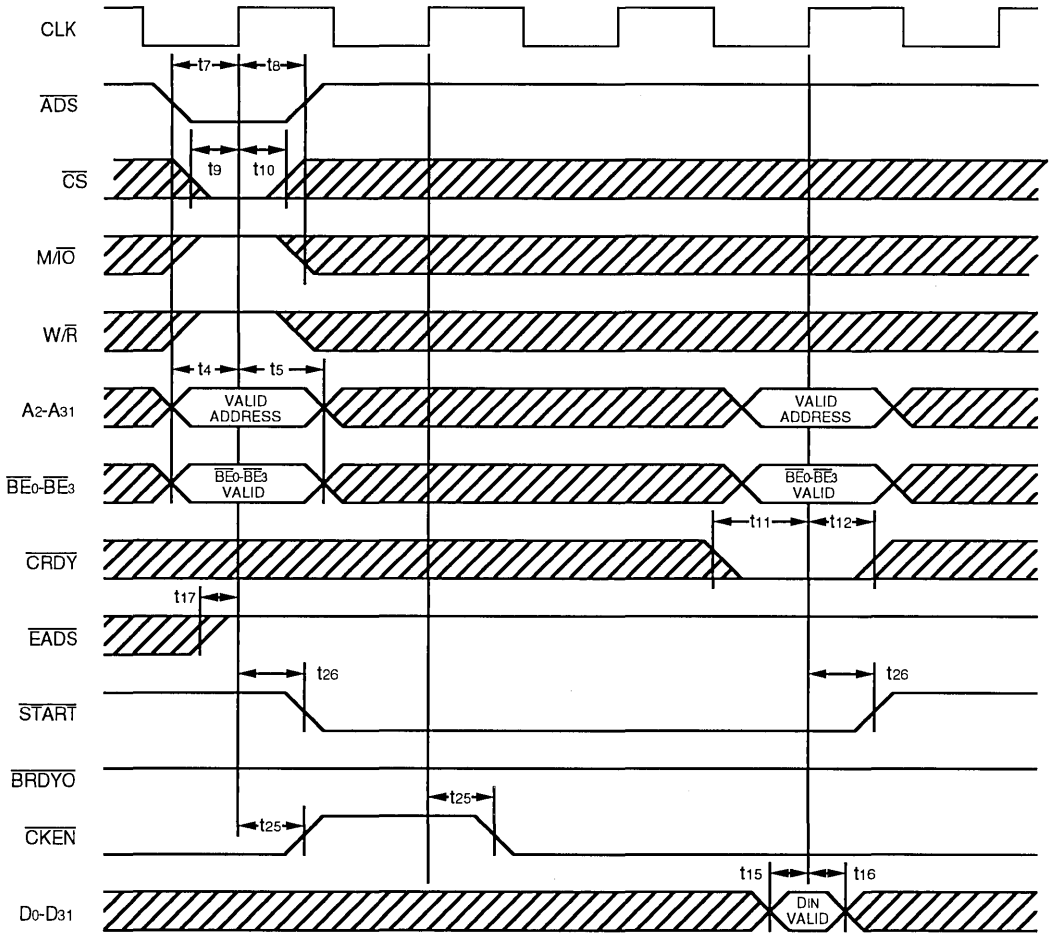
NOTE:
1. If EADS and ADS are asserted simultaneously, ADS is ignored.

TIMING WAVEFORM OF A BACKOFF OPERATION



2897 drw 10

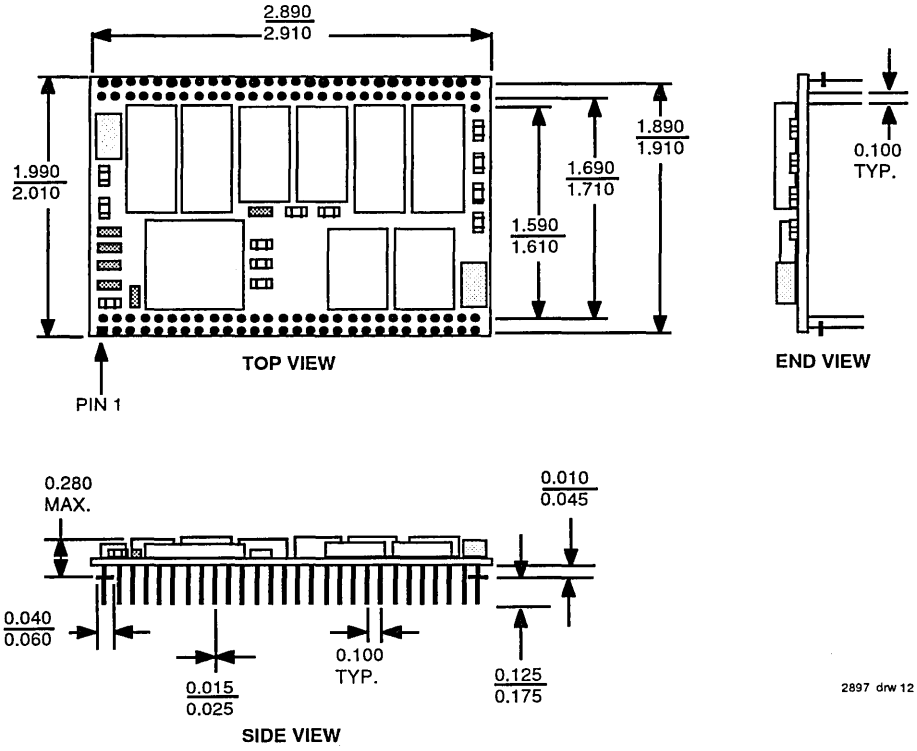
TIMING WAVEFORM OF A WRITE CYCLE(1, 2)



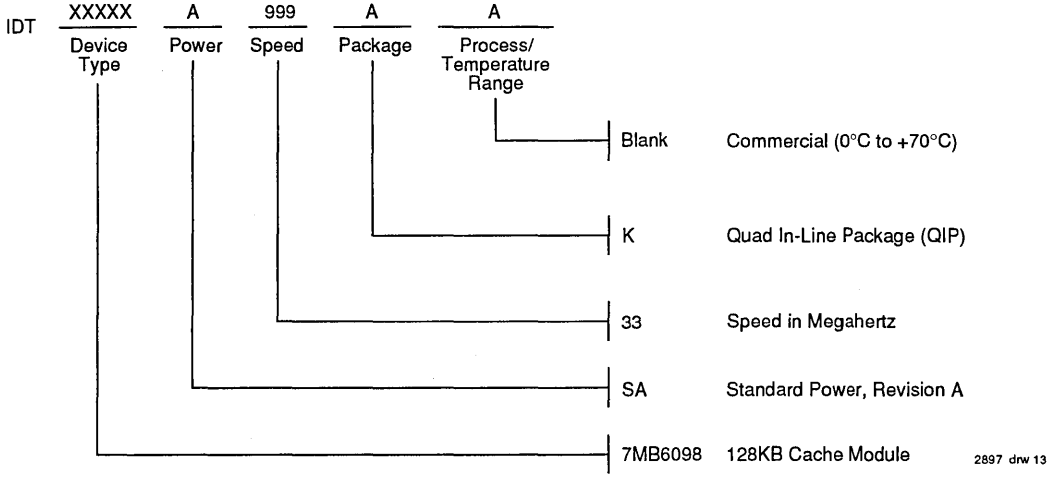
NOTES:
1. RESET is held LOW, $\overline{FLUSH}$ is held HIGH, $\overline{BOFF}$ is held HIGH.
2. For a write hit, data in the IDT7MB6098A is updated.

2897 drw 11

PACKAGE DIMENSIONS



ORDERING INFORMATION



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