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82750LH
Technical Specifications

September 1992

Order Number: 241344-001

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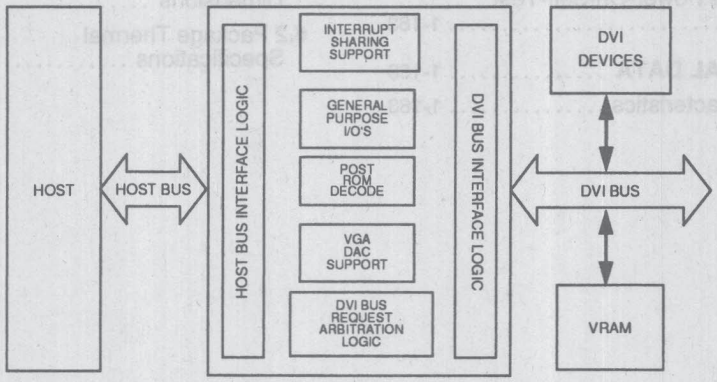
82750LH HOST INTERFACE GATE ARRAY

The 82750LH or HIGA is the Host Interface Gate Array for use in DVI® Systems. Its primary function is to interface the host bus (MicroChannel for PS/2-based systems, ISA for AT-based systems) to the DVI bus. The HIGA also serves five secondary functions. It performs Power-On-Self-Test (POST) ROM Decode, DVI Bus Request Arbitration, VGA DAC Support, Interrupt Sharing Hardware Support and provides General Purpose Inputs and Outputs.

The 82750LH is fabricated on a 1.2μ double metal layer CMOS* technology and is packaged in a 160-lead PQFP. The 82750LH is designed to run at a maximum frequency of 25 MHz.

82750LH - HIGA



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Manufactured and tested for Intel by Texas Instruments in accordance with Texas Instruments internal standards.

1.0 PIN DESCRIPTIONS

1.1 Pinout

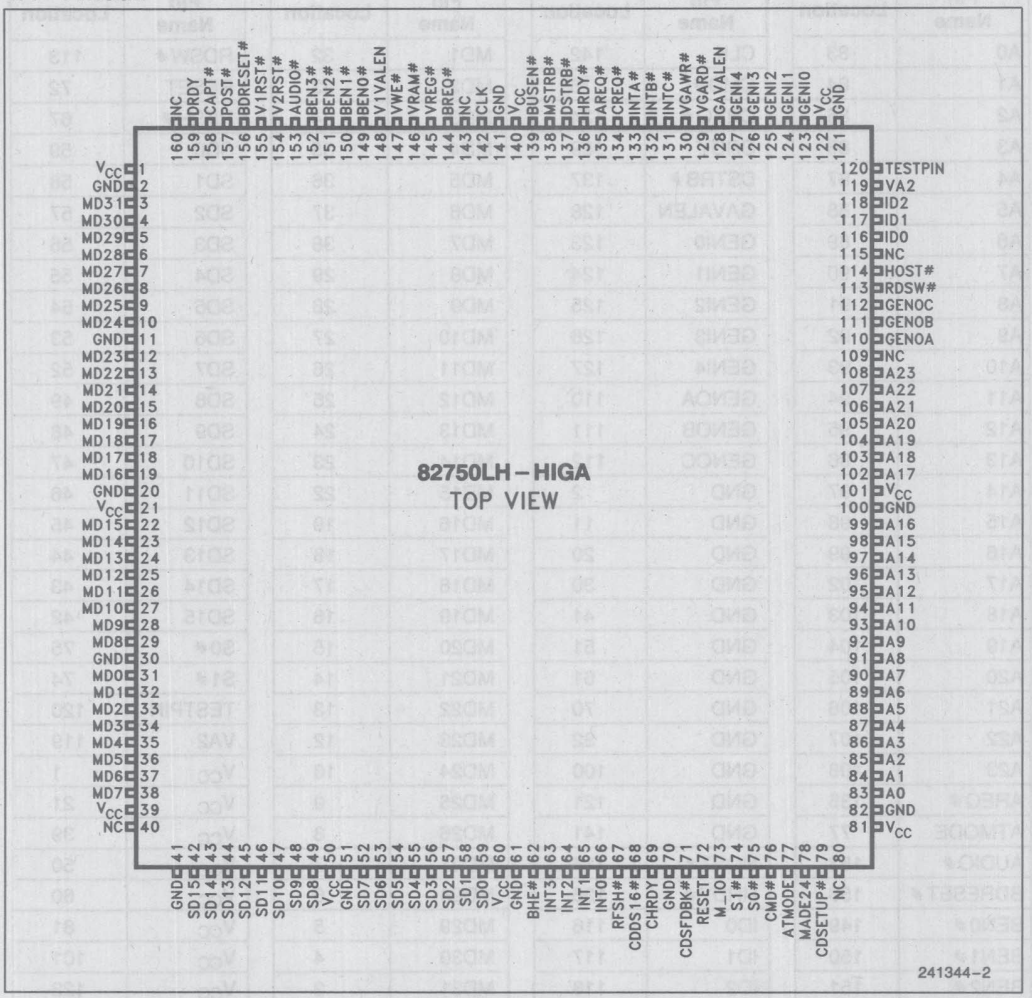


Figure 1-1. 82750LH Pinout

A10	93	GENI4	127	MD11	26	SD7	52
A11	94	GENOA	110	MD12	25	SD8	49
A12	95	GENOB	111	MD13	24	SD9	48
A13	96	GENOC	112	MD14	23	SD10	47
A14	97	GND	2	MD15	22	SD11	46
A15	98	GND	11	MD16	19	SD12	45
A16	99	GND	20	MD17	18	SD13	44
A17	102	GND	30	MD18	17	SD14	43
A18	103	GND	41	MD19	16	SD15	42
A19	104	GND	51	MD20	15	S0#	75
A20	105	GND	61	MD21	14	S1#	74
A21	106	GND	70	MD22	13	TESTPIN	120
A22	107	GND	82	MD23	12	VA2	119
A23	108	GND	100	MD24	10	V_{CC}	1
AREQ#	135	GND	121	MD25	9	V_{CC}	21
ATMODE	77	GND	141	MD26	8	V_{CC}	39
AUDIO#	153	HOST#	114	MD27	7	V_{CC}	50
BDRESET#	156	HRDY#	136	MD28	6	V_{CC}	60
BEN0#	149	ID0	116	MD29	5	V_{CC}	81
BEN1#	150	ID1	117	MD30	4	V_{CC}	101
BEN2#	151	ID2	118	MD31	3	V_{CC}	122
BEN3#	152	INTA#	133	MSTRB#	138	V_{CC}	140
BHE#	62	INTB#	132	M_IO	73	VGARD#	129
BREQ#	144	INTC#	131	NC	40	VGAWR#	130
BUSEN#	139	INT0	66	NC	80	VRAM#	146
CAPT#	158	INT1	65	NC	109	VREG#	145
CDDS16#	68	INT2	64	NC	115	VWE#	147
CDSETUP#	79	INT3	63	NC	143	V1RST#	155
CDSFDBK#	71	MADE24	78	NC	160	V2RST#	154
CHRDY	69	MD0	31	POST#	157	V1VALEN	148

Table 1-2. Pin Cross Reference by Pin Number

Location	Pin Name	Location	Pin Name	Location	Pin Name	Location	Pin Name
1	V_{CC}	41	GND	81	V_{CC}	121	GND
2	GND	42	SD15	82	GND	122	V_{CC}
3	MD31	43	SD14	83	A0	123	GENI0
4	MD30	44	SD13	84	A1	124	GENI1
5	MD29	45	SD12	85	A2	125	GENI2
6	MD28	46	SD11	86	A3	126	GEBI3
7	MD27	47	SD10	87	A4	127	GENI4
8	MD26	48	SD9	88	A5	128	GAVALEN
9	MD25	49	SD8	89	A6	129	VGARD#
10	MD24	50	V_{CC}	90	A7	130	VGAWR#
11	GND	51	GND	91	A8	131	INTC#
12	MD23	52	SD7	92	A9	132	INTB#
13	MD22	53	SD6	93	A10	133	INTA#
14	MD21	54	SD5	94	A11	134	CREQ#
15	MD20	55	SD4	95	A12	135	AREQ#
16	MD19	56	SD3	96	A13	136	HRDY#
17	MD18	57	SD2	97	A14	137	DSTRB#
18	MD17	58	SD1	98	A15	138	MSTRB#
19	MD16	59	SD0	99	A16	139	BUSEN#
20	GND	60	V_{CC}	100	GND	140	V_{CC}
21	V_{CC}	61	GND	101	V_{CC}	141	GND
22	MD15	62	BHE#	102	A17	142	CLK
23	MD14	63	INT3	103	A18	143	NC
24	MD13	64	INT2	104	A19	144	BREQ#
25	MD12	65	INT1	105	A20	145	VREG#
26	MD11	66	INT0	106	A21	146	VRAM#
27	MD10	67	RFSH#	107	A22	147	VWE#
28	MD9	68	CDDS16#	108	A23	148	V1VALEN
29	MD8	69	CHRDY	109	NC	149	BEN0#
30	GND	70	GND	110	GENOA	150	BEN1#
31	MD0	71	CDSFDBK#	111	GENOB	151	BEN2#
32	MD1	72	RESET	112	GENOC	152	BEN3#
33	MD2	73	M_IO	113	RDSW#	153	AUDIO#
34	MD3	74	S1#	114	HOST#	154	V2RST#
35	MD4	75	S0#	115	NC	155	V1RST#
36	MD5	76	CMD#	116	ID0	156	BDRESET#
37	MD6	77	ATMODE	117	ID1	157	POST#
38	MD7	78	MADE24	118	ID2	158	CAPT#
39	V_{CC}	79	CDSETUP#	119	VA2	159	DRDY
40	NC	80	NC	120	TESTPIN	160	NC

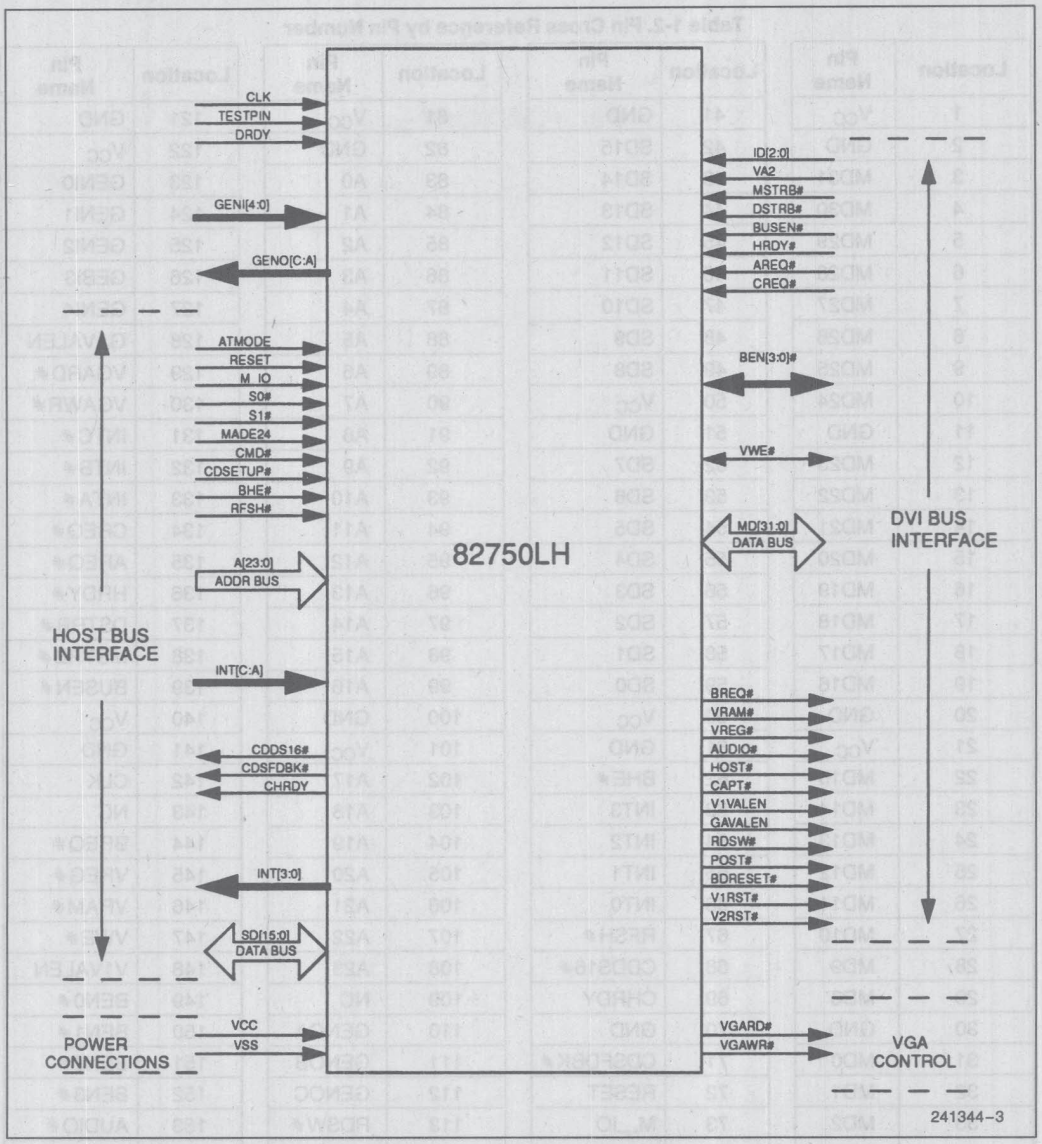


Figure 1-2. 82750LH Functional Signal Groupings

GENI0	I	GENI0 is a generic input pin whose state can be read through General Status Register bit 4. GENI0 has an internal pull up resistor of approximately 70 KΩ.
GENI1	I	GENI1 is a generic input pin whose state can be read through the General Status Register bit 5. GENI1 has an internal pull up resistor of approximately 70 KΩ.
GENI2	I	GENI2 is a generic input pin whose state can be read through General Status Register bit 6. GENI2 has an internal pull up resistor of approximately 70 KΩ.
GENI3	I	GENI3 is a generic input pin whose state can be read through the General Status Register bit 7. GENI3 has an internal pull up resistor of approximately 70 KΩ.
GENI4	I	GENI4 is a generic input pin whose state can be read through the General Status Register bit 0. GENI4 has an internal pull up resistor of approximately 70 KΩ.
GENOA	O	GENOA is a generic output from the HIGA that is controlled by the General Control Register bit 4.
GENOB	O	GENOB is a generic output from the HIGA that is controlled by the General Control Register bit 5.
GENOC	O	GENOC is a generic output from the HIGA that is controlled by the General Control Register bit 2.

Table 1-4. DVI Bus Signal Pin Descriptions

Symbol	Type	Name and Function
ID[2:0]	I	ID0, ID1 and ID2 are the DVI Device ID input pins used by the HIGA to decode the DVI Devices internal to the HIGA. The HIGA uses DVI Device 3 and DVI Device 2 (POST ROM). ID0, ID1 and ID2 have internal pull up resistors of approximately 70 KΩ.
VA2	I	VA2 is used to decode DVI Device 3 into two 32-bit registers.
MSTRB#	I	MSTRB# is the Memory Strobe signal used to indicate the end of a memory cycle. MSTRB# is also used to indicate when data can be read from the DVI Data Bus. The HIGA samples the DVI Data Bus on the rising edge of CLK during MSTRB#. This signal has an internal pull up resistor of approximately 70 KΩ.
DSTRB#	I	DSTRB# is the DVI Device Strobe signal used to indicate a DVI Device cycle on the DVI Bus. MSTRB# is still used to indicate when data can be read from the DVI Data Bus, even though the bus cycle is a DVI Device Bus cycle. The HIGA samples DVI Bus data on the rising edge of CLK during MSTRB#. This signal has an internal pull up resistor of approximately 70 KΩ.
BUSEN#	I	BUSEN# is the Bus Enable signal on the DVI Bus. The HIGA uses BUSEN# as an indicator to know when the DVI Bus has been given up by the 82750PB. This signal has an internal pull up resistor of approximately 70 KΩ.

Table 1-4. DVI Bus Signal Pin Descriptions (Continued)

Symbol	Type	Name and Function
BREQ#	O	BREQ# is a Bus Cycle Request signal to the 82750PB. The 82750PB responds with a BUSEN# to indicate that the request is being serviced.
HRDY#	I	HRDY# is the Host Ready signal from the 82750PB. The HIGA uses HRDY# to drop the BREQ# signal to the 82750PB. This signal has an internal pull up resistor of approximatley 70 KΩ.
VRAM#	O	VRAM# is the Bus Cycle Type Indicator signal for the 82750PB. When VRAM# is active with a bus request (BREQ#) then the DVI Bus cycle will be a VRAM access or a DVI Device Access (as opposed to an 82750PB register access).
VREG#	O	VREG# is a bus cycle type indicator for the 82750PB. When VREG# is active with a bus request (BREQ#) then the DVI Bus cycle will be an 82750PB register access. The VREG# signal is always the opposite of VRAM#.
AREQ#	I	AREQ# is the Audio Bus Request signal on the DVI Bus. The HIGA arbitrates the external requests and the internal requests and presents the BREQ# signal to the 82750PB. This signal has an internal pull up resistor of approximately 70 KΩ.
CREQ#	I	CREQ# is the Capture/SCSI Bus Request signal on the DVI Bus. The HIGA arbitrates the external requests and the internal requests and presents the BREQ# signal to the 82750PB. This signal has an intemal pull up resistor of approximately 70 KΩ.
AUDIO#	O	AUDIO# is the arbitrated output from the HIGA's internal arbitration logic. The HIGA arbitrates the Audio request, Capture/SCSI request and the HIGA internal requests and decides who should respond to the next DVI Bus cycle with BUSEN# active. AUDIO# active indicates that AREQ# is currently being serviced or will be serviced with the next BUSEN#.
HOST#	O	HOST# active indicates that an internal request is currently being serviced or will be serviced with the next BUSEN#.
CAPT#	O	CAPT# active indicates that CREQ# is currently being serviced or will be serviced with the next BUSEN#.
CLK	I	CLK is a CMOS compatible clock signal for the HIGA. The HIGA uses CLK to synchronize events on the host bus to events on the DVI Bus. All synchronous events occur on the rising edge of CLK.
MD[31:0]	B	MD[31:0] are the DVI Bus Data Bus signals used to transfer data between the HIGA and VRAM or other DVI Devices. At the beginning of DVI Bus cycles, the MD[31:0] lines carry the address information. These signals have internal pull up resistors of approximately 70 KΩ.
V1VALEN	O	V1VALEN is the VRAM Latch Enable signal input to the 82750PB. While V1VALEN is high and BUSEN# is low, address information is presented on the MD[31:0] data lines.
GAVALEN	O	GAVALEN is the VRAM Address Latch Enable signal input to devices on the DVI Bus. GAVALEN's high to low transition lags V1VALEN by one clock period.
BEN[3:0]#	B	BEN0# through BEN3# are the Byte Enable signals on the DVI Bus. They define which byte or bytes are involved in the DVI Bus cycle. BEN0# signals the use of the least significant byte, or data lines MD[7:0]. These signals have internal pull up resistors of approximately 70 KΩ.
VWE#	B	VWE# is the read/write direction control for the DVI Bus. When VWE# is low, the bus cycle is a write. This signal has an internal pull up resistor of approximately 70 KΩ.

Table 1-4. DVI Bus Signal Pin Descriptions (Continued)

Symbol	Type	Name and Function
RDSW#	O	RDSW# is used to gate the switch information onto the DVI Bus data bus lines MD[31:0]. The trailing edge of RDSW# (low to high) latches the information into the HIGA. MD[7:0] lines are latched into the I/O Port Switch Register while the MD[15:8] lines are latched into the POST Address Switch Register. The HIGA uses this information to configure the I/O Port Address and POST ROM Address while in the ATMODE of operation.
POST#	O	POST# is the chip select output for the POST ROM on the DVI Bus. POST# is a decode of DVI Device 2, DSTRB# and not VWE#. Since POST is an eight bit device, the HIGA does not return the CDDS16# (or MEMCS16#) signal during POST accesses. Additionally, special steering logic inside the HIGA logically connects the MD[7:0] lines to the SD[7:0] lines regardless of the byte address. Therefore, consecutive byte accesses do not progress from MD[7:0] to MD[15:8] to MD[23:16], etc. when accessing the POST ROM.
BDRESET#	O	BDRESET# is the Board Reset signal controlled by the General Control Register bit 0. BDRESET# is also applied when the RESET input is active. Besides driving the output pin low, BDRESET# also resets the HIGA internal registers, state machine and FIFO logic. The POS and PAR registers are not affected by Board Reset. BDRESET# should be held low for at least 10 μs to guarantee a full board reset.
V1RST#	O	V1RST# is the 82750PB Reset signal controlled by the General Control Register bit 1. V1RST is also applied when the RESET input is active.
V2RST#	O	V2RST# is the 82750DB Reset signal controlled by the General Control Register bit 7.

Table 1-5. Host Bus Signal Pin Descriptions

Symbol	Type	Name and Function
ATMODE	I	ATMODE configures the HIGA for an AT or ISA type interface for the host bus when high. When low, ATMODE configures the host interface for the MicroChannel type interface. This signal has an internal pull up resistor of approximately 70 KΩ.
RESET	I	RESET is the main reset signal for the HIGA. This signal has an internal pull up resistor of approximately 70 KΩ.
SD[15:0]	B	SD[15:0] are the host data bus signals used to transfer data between the host and the HIGA. These signals have internal pull up resistors of approximately 70 KΩ.
A[23:0]	I	A[23:0] are the host address pins. The address signals are used to access the registers internal to the HIGA as well as the VRAM and DVI Devices on the DVI Bus. These signals have intemal pull up resistors of approximately 70 KΩ.
M__IO (IOWRC#)	I	M__IO is the memory or I/O cycle indicator signal on the MicroChannel Bus when the HIGA is in the non-ATMODE. M__IO is the ISA IOWRC# signal when the HIGA is in the ATMODE of operation.
S0# (MRDC#)	I	SO# is the Status 0 signal on the MicroChannel Bus when the HIGA is in the non-ATMODE. S0# is the ISA MRDC# signal when the HIGA is in the ATMODE of operation.
S1# (MWRC#)	I	S1# is the Status 1 signal on the MicroChannel Bus when the HIGA is in the non-ATMODE. S0# is the ISA MWRC# signal when the HIGA is in the ATMODE of operation.
MADE24 (IORDC#)	I	MADE24 is the below 16M memory cycle indicator signal on the MicroChannel Bus when the HIGA is in the non-ATMODE. MADE24 is the ISA IORDC# signal when the HIGA is in the ATMODE of operation.

		the POS4 register in the HIGA. This signal has an internal pull up resistor of approximately 70 KΩ.
INTB#	I	INTB# is the Audio Interrupt signal on the DVI Bus. The INTB# signal can be steered to one of the INT1 or INT2 outputs through programming of the POS4 register in the HIGA. This signal has an internal pull up resistor of approximately 70 KΩ.
INTC#	I	INTC# is the Capture/SCSI Interrupt signal on the DVI Bus. INTC# can be steered to one of the INT1 or INT2 outputs through programming of the POS4 register in the HIGA. This signal has an internal pull up resistor of approximately 70 KΩ.
CDDS16# (IOCS16#)	O	CDDS16# is the Card Data Size16 signal on the MicroChannel Bus when the HIGA is in the non-ATMODE of operation. CDDS16# is the ISA IOCS16# signal when the HIGA is in the ATMODE.
CDSFDBK# (MEMCS16#)	O	CDSFDBK# is the Card Select Feedback signal on the MicroChannel Bus when the HIGA is in the non-ATMODE of operation. CDSFDBK# is the ISA MEMCS16# signal when the HIGA is in the ATMODE.
CHRDY (IOCHRDY)	O	CHRDY is the Channel Ready signal on the MicroChannel Bus when the HIGA is in the non-ATMODE of operation. CHRDY is the ISA IOCHRDY signal when the HIGA is in the ATMODE.
INT[3:0]	O	INT0 through INT3 are the four interrupt output pins on the HIGA. In the non-ATMODE of operation the INT outputs are active low, open collector type outputs. In the ATMODE of operation the INT outputs are active high, totem pole type outputs.

Table 1-6. VGA Support Signal Pin Descriptions

Symbol	Type	Name and Function
VGARD#	O	VGARD# is the VGA DAC Read signal. VGARD# is active during host reads of the VGA DAC Test Registers. Note that the HIGA does not drive the SD[15:0] lines during VGARD# cycles, but does provide the other host timing necessary for the cycle.
VGAWR#	O	VGAWR# is the VGA DAC Write signal. VGAWR# is active during host writes of the VGA DAC Registers. Note that the HIGA does not accept any data from the SD[15:0] lines during VGAWR# cycles.

Table 1-7. Output Pins**

Name	Active Level
INT[3:0]	*
CDDS16#	Low
CHRDY	High
CDSFDBK#	Low
GENO[C:A]	High
RDSW#	Low
HOST#	Low
GAVALEN	High
VGARD#	Low
VGAWR#	Low
BREQ#	Low
VREG#	Low
VRAM#	Low
V1VALEN	High
AUDIO#	Low
V2RST#	Low
V1RST#	Low
BDRESET#	Low
POST#	Low
CAPT#	Low

NOTE:
*Active high in ATMODE.
Active low in non-ATMODE.

Table 1-8. Input Pins

Name	Active Level	Sync/Async
BHE#	Low	Async
RFSH#	Low	Async
RESET	High	Async
M_IO	High	Async
S1#	Low	Async
S0#	Low	Async
CMD#	Low	Async
ATMODE	High	Async
MADE24	High	Async
CDSETUP#	Low	Async
A[23:0]	High	Async
ID[2:0]	High	Async
VA2	High	Sync
GENI[4:0]	High	Async
INT[C:A]	Low	Async
CREQ#	Low	Async
AREQ#	Low	Async
HRDY#	Low	Sync
DSTRB#	Low	Sync
MSTRB#	Low	Sync
BUSEN#	Low	Sync
CLK	High	Sync
DRDY#	Low	Async

Table 1-9. Bidirectional Pins

Name	Active Level	When Floated**	Sync/Async
MD[31:0]	High	VRAM Read, DVI Device Read	Sync
SD[15:0]	High	Host Reads	Async
VWE#	Low		Sync
BEN[3:0]#	Low		Sync

NOTE:
**All output and bidirectional pins are floated when TESTPIN and RESET are asserted together.

2.0 INTERNAL ARCHITECTURE

2.1 DVI/Host Bus Interface

2.1.1 DVI BUS OVERVIEW

The primary function of the HIGA is to interface the host bus (MicroChannel for PS/2-based systems, ISA for AT-based systems) to the DVI Bus. The DVI Bus connects VRAM, the 82750PB, Audio and host together through one common address and data path. The 82750PB normally owns the DVI Bus. The HIGA is designed to run at the same frequency as the 82750PB.

The data bus from the host passes through the HIGA before reaching the DVI Bus and also creates an intermediate path for passing around the HIGA. This allows for two types of accesses to components in the DVI system: accesses that require the use of the DVI Bus and those that do not. The two types of accesses are classified into a Slow Access Group and a Fast Access Group respectively. When the HIGA is running at 25 MHz a Fast Access takes about 400 ns (10 cycles) to complete while a Slow Access can take up to 3000 ns (75 cycles) to complete.

The DVI Bus supports up to 16 Mbytes of address space. The first 15 Mbytes of address space is reserved for RAM while the last 1 Mbyte of address space is reserved for communication between devices on the DVI Bus. The last 1 Mbyte of address space is divided into eight 128 Kbyte areas with each device assigned to one of the eight areas as a DVI Device ID. DVI Device ID 0 is the first 128K area above 15 Mbytes and DVI Device ID 7 is the last 128 Kbyte area. The following DVI Device ID assignments have been made:

Device ID 7 —82750PB Registers via the Host Bus

Device ID 6 — Capture Subsystem Registers

Device ID 5 — Audio Subsystem, Genlock and Keying Registers

Device ID 4 — CDROM Subsystem Registers

Device ID 3 — Reserved

Device ID 2 — Power-On-Self-Test (POST) ROM

Device ID 1 — Reserved

Device ID 0 — Reserved

2.1.2 EXPANDED MEMORY SPACE HOST/ VRAM CONNECTION

VRAM is seen by the host in memory space by a method known as EMS or Expanded Memory Space. The EMS method of expanding memory uses a technique in which memory is paged mapped through a "window" of the host's address space.

The HIGA supports 13 EMS window options ranging in size from 0 bytes to 16 Mbytes. The EMS window options that are supported are 0 bytes, 8 Kbytes, 16 Kbytes, 32 Kbytes, 64 Kbytes, 128 Kbytes, 256 Kbytes, 512 Kbytes, 1 Mbytes, 2 Mbytes, 4 Mbytes, 8 Mbytes, and 16 Mbytes. The EMS window size and starting window location are established by setting bits in the Configuration Registers.

A window's starting address must be a multiple of its size. As an example, a 128 Kbyte window must start on a 128 Kbyte boundary in the host's memory address space. Each EMS window is divided into four equally sized pages which have corresponding Page Address Registers (PARs). The PARs are used to map the logical (window) address space of the host independently into four pages of physical addresses in VRAM (with page aligned starting addresses).

2.1.3 HOST/VRAM FIFO CONNECTION

There are four FIFOs connecting the host to VRAM in addition to the EMS connection. The FIFOs are in the host's I/O address space whereas the EMS window is in the host's memory address space. The FIFOs are divided into four types and there is one of each type available: a 16-Bit-Read FIFO, a 16-Bit-Write FIFO, a 32-Bit-Read FIFO and a 32-Bit-Write FIFO. A 16-bit FIFO will only access 16-bit words in the VRAM address space and is useful for accessing 82750PB registers. A 32-bit FIFO can access 32-bit words in the VRAM address space and is useful for accessing VRAM in high-performance modes or through Host DMA channels. All FIFOs can be operated in an Auto-increment Mode in which the VRAM address is incremented after each access through the FIFO.

2.1.4 DVI DEVICE ACCESS

In order to allow accesses to DVI Devices (which are memory mapped) or to setup a FIFO without having to change the Page Address Registers, a Quick Access method is provided. The Quick Access method is selected by writing the DVI Device ID to a control register via an I/O operation. In this mode, the next memory access through the PARs (not FIFOs) will have the physical address modified to point to the selected DVI Device. The DVI Device ID must be rewritten for the next access through this path, even if the previous access was to the same DVI Device. This method reduces the overhead for accessing a DVI Device to one Fast Access and one Slow Access operation, without disturbing the PARs. Note that the Quick Access is armed for the next memory access through any of the PARs, regardless of the source of the access (Host or DMA).

2.2 Power-On-Self-Test ROM

The HIGA provides support for configuring and enabling/disabling a Power-On-Self-Test ROM. The POST ROM, when installed and enabled, will be executed after the host's POST but before the system boots and may contain a self-test program and any special configuration programs.

2.3 DVI Bus Request Arbitration

The HIGA arbitrates all of the requests for the DVI Bus and asserts the acknowledge for the highest priority request. The possible requests are: EMS from the HIGA's EMS logic, FIFO from the HIGA's internal FIFO logic, CAPT from the external CREQ# pin, AUDIO from the external AREQ# pin and V1REQ from DVI Device 3. The FIFO request is an arbitrated request from the FIFO logic which ranks the requests as follows: 32-Bit-Write FIFO, 16-Bit-Write FIFO, 32-Bit-Read FIFO, 16-Bit-Read FIFO. Table 2-1 summarizes the request priorities.

Table 2-1. Bus Request Priority

Priority	Request
1	EMS
2	32-Bit-Write FIFO
3	16-Bit-Write FIFO
4	32-Bit-Read FIFO
5	16-Bit-Read FIFO
6	CAPT
7	AUDIO
8	V1REQ

The arbitration algorithm is such that once requests have been stacked up, the arbitration logic services the stacked up requests before any other requests will be considered. This behavior keeps a high-priority request from monopolizing the DVI Bus. For example, consider a situation where HREQ is asserted. While HREQ is being serviced AREQ is asserted, followed by CREQ. Even though AREQ was asserted first, CREQ will be the next to get attention. This is because when one request is already in the process of being serviced no other requests are considered and they stack up. Then when arbitration continues (after the service is completed) all stacked up requests enter at the same time and the one with the highest priority will be the next to be serviced. Only stacked up requests and requests that become active on the same CLK edge are arbitrated against each other. Otherwise, requests are honored in the order in which they are received.

Another example of the arbitration algorithm is one in which all of the possible requests become active in the opposite order of priority, all separated by one clock period. The first request to be serviced is the lowest priority one since it came in first, followed by the rest of the requests in order of priority or the opposite order in which they arrived. This is because they all stacked up behind the lowest priority request.

2.4 VGA DAC Support

The DVI Board may have a VGA type DAC onboard which can be used along with the Video Feature Connector to "copy" the video stream from the system's VGA. The onboard VGA video can then be keyed with 82750DB's output. The final RGB video information is output to a standard VGA monitor and connector. The monitor ID supplied to the monitor connector by the connected monitor can be read by the host.

All I/O writes on the system bus are monitored by the HIGA. When an I/O write falls into the range of 03C6-03C9, hex for the PS/2-based system or X3C6-X3C9 hex for the AT-based system, a VGA write to the onboard VGA DAC is generated, duplicating the data in the system's VGA DAC. I/O reads to 03C6-03C9 are ignored by the DVI Board to prevent two I/O devices from driving data at the same time. Using this eavesdropping programming technique together with the system's Video Feature Bus allows the DVI Board to maintain an RGB video stream identical to the system's VGA RGB creating a VGA compatible mode that is transparent to the programmer or user.

The General Control Register contains the DINT (Disable Interrupt) bit that can be used to reassert

the host's I/O space at BASE-BASE+3F hex plus the POS registers through the POS setup mechanism in PS/2-based machines. A register map of the HIGA registers is shown in Table 2-2.

Table 2-2. HIGA Register Map

B1 ..... B8	B7 ..... B0	
PAR0 HIGH	PAR0 LOW	BASE+0
PAR1 HIGH	PAR1 LOW	BASE+2
PAR2 HIGH	PAR2 LOW	BASE+4
PAR3 HIGH	PAR3 LOW	BASE+6
ROM 8K SELECT REGISTER	DVI DEVICE QUICK ACCESS	BASE+8
32-BIT-WRITE FIFO DATA HIGH	32-BIT-WRITE FIFO DATA LOW	BASE+20
32-BIT-WRITE FIFO ADDR CNTR BYTE	32-BIT-WRITE FIFO CONTROL	BASE+22
16-BIT-WRITE FIFO DATA HIGH	16-BIT-WRITE FIFO DATA LOW	BASE+24
16-BIT-WRITE FIFO ADDR CNTR BYTE	16-BIT-WRITE FIFO CONTROL	BASE+26
32-BIT-READ FIFO DATA HIGH	32-BIT-READ FIFO DATA LOW	BASE+28
32-BIT-READ FIFO ADDR CNTR BYTE	32-BIT-READ FIFO CONTROL	BASE+2A
16-BIT-READ FIFO DATA HIGH	16-BIT-READ FIFO DATA LOW	BASE+2C
16-BIT-READ FIFO ADDR CNTR BYTE	16-BIT-READ FIFO CONTROL	BASE+2E
GENERAL STATUS REGISTER	POS0	BASE+30
GENERAL CONTROL REGISTER	POS1	BASE+32
I/O PORT SWITCH REGISTER	POS2	BASE+34
POST ADDRESS SWITCH REGISTER	POS3	BASE+36
RESERVED	POS4	BASE+38
RESERVED	POS5	BASE+3A
VGA TEST REGISTER 3C9	VGA TEST REGISTER 3C8	BASE+3C
VGA TEST REGISTER 3C7	VGA TEST REGISTER 3C6	BASE+3E

The fast access registers for the FIFO data ports can become slow access registers if the access must cause a DVI Bus cycle in order for it to complete. Reading an empty read FIFO or writing a full write FIFO are the only examples of this condition. All other system registers and VRAM are in the Slow Access Group.

2.7.1 PAGE ADDRESS REGISTERS

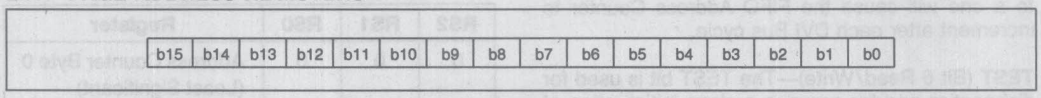


Figure 2-1. PARn

Page Address Registers 0–3 are read/write registers located at BASE+0 hex, BASE+2 hex, BASE+4 hex and BASE+6 hex respectively. The PARs are used to map the logical (window) address space of the host independently into four pages of physical addresses in VRAM. The PARs are 16-bit registers, although only the necessary top PAR bits are used in each EMS Window Mode.

2.7.2 DVI DEVICE QUICK ACCESS REGISTER

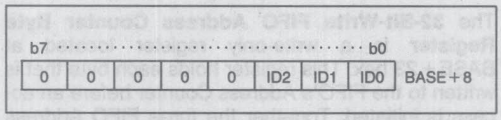


Figure 2-2. DVI Device Quick Access Register

The DVI Device Quick Access Register is a write-only register located at BASE+8 hex. This is an 8-bit register with only the lowest three bits defined. The value of the ID2, ID1 and ID0 taken as a three bit field define a DVI Device ID which is used in conjuction with the Quick Access Method of bypassing the PARs to access a DVI Device Register. The Quick Access Register will be used to force the access to the DVI Device ID contained in this register. The Quick Access is enabled by the writing of the Quick Access Register and lasts for just one access through the EMS Window.

The user is cautioned to keep in mind that the host CPU will turn one 16-bit access at an odd address into two 8-bit accesses and the Quick Access would be enabled for only the first 8-bit access. The user is also cautioned to keep in mind that the HIGA does not distinguish between host cycles performed by the CPU and those that are performed via DMA.

2.7.3 ROM 8K SELECT REGISTER

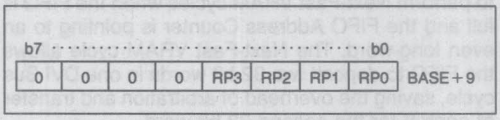


Figure 2-3. ROM 8K Select Register

The ROM 8K Select Register is an 8-bit write-only register located at BASE+9 hex. Only the lowest 4 bits are defined. This register is used to select the 8K page of POST ROM. On RESET the contents of this register is initialized to zero.

2.7.4 FIFO CONTROL, ADDRESS AND DATA REGISTERS

There are five registers associated with each of the FIFOs.

2.7.4.1 32-Bit-Write FIFO Registers

The **32-Bit-Write FIFO Control Register** is a read/write register located at BASE+22 hex. Each of the bits in this register is described below.

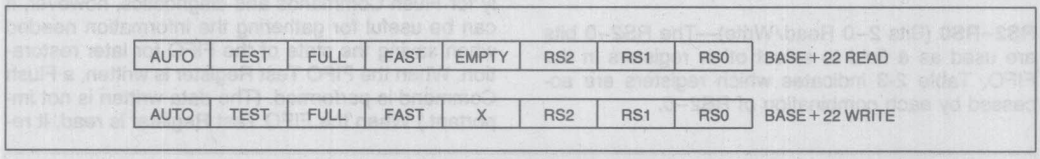


Figure 2-4. 32-Bit-Write FIFO Control Register

AUTO (Bit 7 Read/Write)—The AUTO bit when set to a one will cause the FIFO Address Counter to increment after each DVI Bus cycle.

TEST (Bit 6 Read/Write)—The TEST bit is used for diagnostics and for ensuring a clean initialization of the FIFO. When initializing the FIFO, the first write to the control register should have this bit set to a one.

FULL (Bit 5 Read)—The FULL bit reflects the status of the data holding registers in the FIFO. If the FULL bit is on and data is written to the data ports then the access becomes a Slow Access.

FAST (Bit 4 Read)—The FAST bit allows the FIFO to perform Next-Fast VRAM cycles when the FIFO is full and the FIFO Address Counter is pointing to an even long-word. The Next-Fast VRAM cycle allows the FIFO to deposit two 32-bit words in one DVI Bus cycle, saving the overhead of arbitration and transfer of control for the second 32-bit word.

EMPTY (Bit 3 Read)—The EMPTY bit reflects the status of the data holding registers in the FIFO. A write FIFO should always be empty before any change is made to its FIFO Control Register that may cause a pending data operation to fail. Such operations include a change from AUTO to not AUTO (or the reverse), any change to the FIFO Address Counter and setting the TEST or TCLK bits. The 32-Bit-Write FIFO will try to empty the data registers whenever the most significant byte of a 32-bit word is received from the host. If a transfer from the host ends on the first, second or third byte then the FIFO will not go empty until the host performs a Flush Command. Sending a Flush Command to a FIFO that would have normally gone empty or was already empty does no harm whatsoever.

TCLK (Bit 5 Write)—The TCLK bit should be left as a zero for proper FIFO operation.

RS2–RS0 (Bits 2–0 Read/Write)—The RS2–0 bits are used as a field to select other registers in the FIFO. Table 2-3 indicates which registers are accessed by each combination of RS2–0.

Table 2-3. RS2–0 Register Selection

RS2	RS1	RS0	Register
0	0	0	Address Counter Byte 0 (Least Significant)
0	0	1	Address Counter Byte 1
0	1	0	Address Counter Byte 2 (Most Significant)
0	1	1	Test Register
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

The **32-Bit-Write FIFO Address Counter Byte Register** is a write-only register located at BASE + 23 hex. This register holds each byte that is written to the FIFO's Address Counter before an access is initiated. Together the three FIFO Address Counter Bytes hold the 24-bit byte address of the destination of the FIFO data. The FIFO Control Register and the FIFO Address Counter Byte Register can be written with the same 16-bit I/O operation.

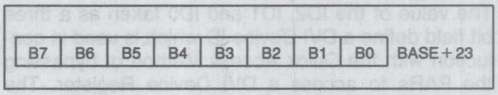


Figure 2-5. 32-Bit-Write FIFO Address Counter Byte Register (RS = 0,1,2)
32-Bit-Write FIFO Test Register (RS = 3)

The **32-Bit-Write FIFO Test Register** is an 8-bit read/write register located at BASE + 23 hex that is accessed when bits RS[2:0] in the corresponding control register = 3(010). This register is used mainly for Flush Commands and diagnostics, however, it can be useful for gathering the information needed when saving the state of the FIFO for later restoration. When the FIFO Test Register is written, a Flush Command is performed. (The data written is not important.) When the FIFO Test Register is read, it re-

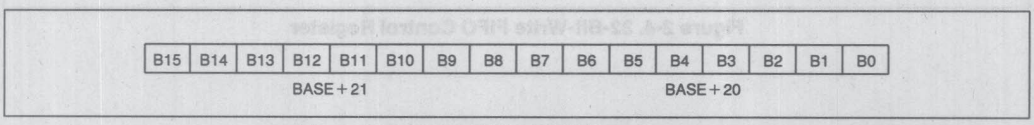


Figure 2-6. 32-Bit-Write FIFO Data Registers

turns some information. B0 will be zero when the first byte has been written to the FIFO Data Register, B1 will be zero when the second byte has been written and so on.

The **32-Bit-Write FIFO Data High and Low Registers** are two 8-bit write-only registers located at BASE+20 hex and BASE+21 hex. The FIFO data registers can be written 8 or 16 bits at a time. However, when writing with byte operations, address BASE+21 hex must be written between any writes to BASE+20 hex.

2.7.4.2 16-Bit-Write FIFO Registers

The 16-Bit-Write FIFO registers are identical to that of the 32-Bit-Write FIFO described above except that the FAST bit in the 16-Bit-Write FIFO Control Register has no meaning. Locations for the 16-Bit-Write FIFO Registers are listed below.

16-Bit-Write FIFO Control Register = BASE+26 hex

16-Bit-Write FIFO Address Counter Byte Register = BASE+27 hex

16-Bit-Write FIFO Test Register = BASE+27 hex

16-Bit-Write FIFO Data High Register = BASE+25 hex

16-Bit-Write FIFO Data Low Register = BASE+24 hex

2.7.4.3 32-Bit-Read FIFO Registers

The **32-Bit-Read FIFO Control Register** is an 8-bit read/write register located at BASE+2A hex. Each of the bits in this register is described below.

AUTO	TEST	TCLK	FAST	EMPTY	RS2	RS1	RS0	BASE+2A READ
AUTO	TEST	TCLK	FAST	X	RS2	RS1	RS0	BASE+2A WRITE

Figure 2-7. 32-Bit-Read FIFO Control Register

most significant byte of a 32-bit word is read from the host. If a transfer from the host ends on the first, second or third byte then the FIFO will contain some residual data. When in the AUTO mode the FIFO will always contain some residual data after the transfer is finished. This unwanted data is a by-product of reading ahead and trying to keep the FIFO full.

FAST (Bit 4 Read)—The FAST bit allows the FIFO to perform Next-Fast VRAM cycles when the FIFO is empty and the FIFO Address Counter is pointing to an even long-word. The Next-Fast VRAM cycle allows the FIFO to fetch two 32-bit words in one DVI Bus cycle, saving the overhead of arbitration and transfer of control for the second 32-bit word.

EMPTY (Bit 3 Read)—The EMPTY bit reflects the status of the data holding registers in the FIFO. If the EMPTY bit is on and data is read from the data ports then the access becomes a Slow Access.

TCLK (Bit 5 Write)—The TCLK bit should be left as a zero for proper FIFO operation.

RS2–RS0 (Bits 2–0 Read/Write)—The RS2-0 bits are used as a field to select other registers in the FIFO.

The **32-Bit-Read FIFO Address Counter Byte Register** is a write-only register located at BASE + 2B hex. This register holds each byte that is written to the FIFO's Address Counter before an access is initiated. Together the three FIFO Address Counter Bytes hold the 24-bit byte address of the source of the FIFO data. The FIFO Control Register and the FIFO Address Counter Byte Register can be written with the same 16-bit I/O operation.

The **32-Bit-Read FIFO Test Register** is an 8-bit read/write register located at BASE + 2B hex that is accessed when RS[2:0] in the corresponding control register = 3 (011). This register is used for diagnostic purposes only.

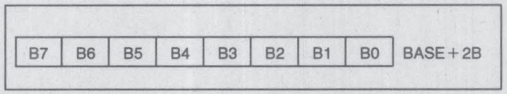


Figure 2-8. 32-Bit-Read FIFO Address Counter Byte Register (RS = 0,1,2) 32-Bit-Read FIFO Test Register (RS3)

The **32-Bit-Read FIFO Data High and Low Registers** are two 8-bit read-only data registers located at BASE + 28 hex and BASE + 29 hex. The FIFO data registers can be written 8 or 16 bits at a time. However, when writing with byte operations, address BASE + 29 hex must be written between any writes to BASE + 28 hex.

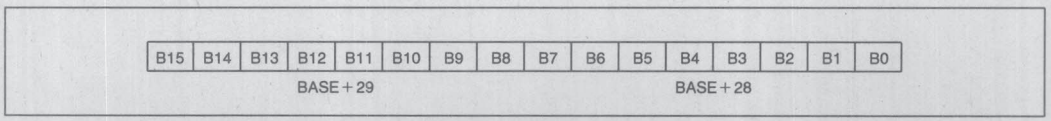


Figure 2-9. 32-Bit-Read FIFO Data Registers

2.7.4.4 16-Bit-Read FIFO Registers

The Registers for the 16-Bit-Read FIFO are identical to those of the 32-Bit-Read FIFO described above except that the FAST bit in the 16-Bit-Read FIFO Control Register has no meaning. Locations for the 16-Bit-Read FIFO Registers are listed below.

16-Bit-Read FIFO Control Register = BASE+2E hex

16-Bit-Read FIFO Address Counter Byte Register = BASE+2F hex

16-Bit-Read FIFO Test Register = BASE+2F hex

16-Bit-Read FIFO Data High Register = BASE+2D hex

16-Bit-Read FIFO Data Low Register = BASE+2C hex

2.7.5 GENERAL STATUS REGISTER

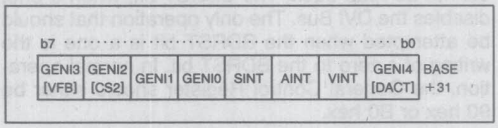


Figure 2-10. General Status Register

The General Status Register is an 8-bit read-only register located at BASE+31 hex. This register contains three dedicated bits that are used to identify interrupt sources and five general purpose input bits (GENI0-4) which correspond directly to the input pins of the same names. In the bit definitions below, the bit names and descriptions shown in brackets ([ ]) are examples of some useful functions that these pins can serve in a typical DVI environment. These bits may, of course, be assigned to any compatible input at the user's discretion.

GENI3 (Bit 7)—General Purpose Input 3.

[**VFB** (Bit 7)—VFB will be a zero if the DVI Board is connected to a Video Feature Bus.]

GENI2 (Bit 6)—General Purpose Input 2.

[**CS2** (Bit 6)—CS2 will be a zero if the DVI Board is hosting a Capture Board.]

GENI1 (Bit 5)—General Purpose Input 1.

GENI0 (Bit 4)—General Purpose Input 0.

SINT (Bit 3)—SINT (SCSI Interrupt) is a read-only bit that reflects the status of the interrupt signal from the SCSI/Capture Subsystem. The SINT bit will be a one whenever the interrupt signal is active.

AINT (Bit 2)—AINT (Audio Interrupt) is a read-only bit that reflects the status of the interrupt signal from the Audio Subsystem. The AINT bit will be a one whenever the interrupt signal is active.

VINT (Bit 1)—VINT (Video Interrupt) is a read-only bit that reflects the status of the interrupt signal from the Video Subsystem (82750PB). The VINT bit will be a one whenever the interrupt signal is active.

GENI4 (Bit 0)—General Purpose Input 4.

[**DACT** (Bit 0)—DACT (DAC Test) bit is a read-only bit that reflects the status of the RGB signals on the Video Output Connector. The DACT bit will be a zero whenever one of the RGB levels is above the 50% of full scale point.]

2.7.6 GENERAL CONTROL REGISTER

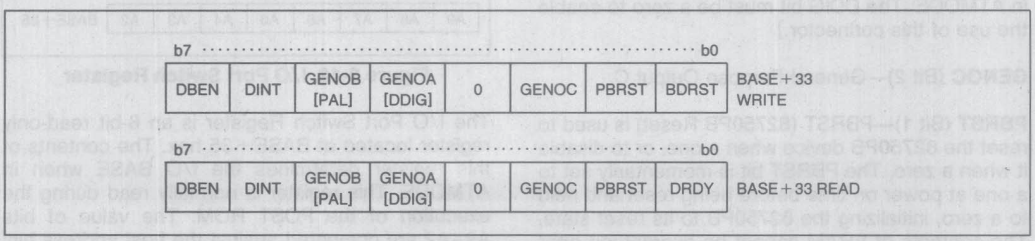


Figure 2-11. General Control Register

The General Control Register is an 8-bit read/write register located at BASE+33 hex. Bit 0 changes definition depending on whether the register is being read or written. This register is reset to 0 by system reset. Four of the bits in this register are dedicated and three of the bits are General Purpose Output bits which correspond to the output pins of the same names. In the bit definitions shown below the bit names and descriptions show in brackets ([ ]) are examples of some useful functions that these bits can serve in a typical DVI environment. They may, of course, be assigned to any compatible output at the user's discretion.

DBEN (Bit 7)—DBEN (82750DB Enable) is used to reset the 82750DB device when it is a zero or to allow the 82750DB to run when it is a one.

DINT (Bit 6)—DINT (Disable Interrupt) is used to re-assert interrupts at the end of an interrupt routine or to disable all of the interrupts from the DVI Board.

GENOB (Bit 5)—General Purpose Output B.

[**PAL** (Bit 5)—PAL (PAL/NTSC) selects the PAL Mode when a one, or NTSC Mode when a zero for the Y-C output circuit.]

GENOA (Bit 4)—General Purpose Output A.

[**DDIG** (Bit 4)—DDIG (Disable 82750DB Digital Outputs) is used to disable the digital video data outputs on the 82750DB device. If the DVI Board uses the analog video data outputs from the 82750DB device, the DDIG bit should be set to a one. The power dissipation of the 82750DB will increase significantly if the DDIG bit is a zero, especially at frequencies above 30 MHz. The 82750DB digital outputs are wired directly to the Ditgital Display Connector when in ATMODE. The DDIG bit must be a zero to enable the use of this connector.]

GENOC (Bit 2)—General Purpose Output C.

PBRST (Bit 1)—PBRST (82750PB Reset) is used to reset the 82750PB device when a one, or to disable it when a zero. The PBRST bit is momentarily set to a one at power on time before being reset and held to a zero, initializing the 82750PB to its reset state. The contents of VRAM cannot be guaranteed after the PBRST bit has been toggled to a one. The PBRST bit, when a one, disables arbitration for the DVI Bus in the 82750PB device. The only operation that should be attempted when the PBRST bit is a one is the writing of a zero to the PBRST bit.

BDRST (Bit 0 Write)—BDRST (Board Reset) is used to reset the entire DVI Board. This reset is so complete that this bit should only be used for debugging purposes. The contents of VRAM cannot be guaranteed after the BDRST bit has been toggled to a one. Setting this bit to a one is the same as a power on reset except that the POS Registers, PAR Registers, 82750PB and the General Control Register itself are not affected. Writing a 03 followed by a 00 to the General Control Register is as complete a reset attainable without powering down. The BDRST bit should be held as a one for at least 10 μs to guarantee a full board reset. Note also that the BDRST bit cannot be read back. The BDRST bit, when a one, disables the DVI Bus. The only operation that should be attempted when the BDRST bit is a one is the writing of a zero to the BDRST bit. In normal operation, the General Control Register should either be 90 hex or B0 hex.

DRDY (Bit 0 Read)—DRDY (Capture Data Ready) is a read-only bit that reflects the status of the Data Ready bit from the capture board.

NOTE:
When trying to set or reset a bit in the General Control Register, do not forget to reset the DRDY bit before writing the data back out, or the system will get stuck in external wait state forcing you to use the main reset switch of the host!

2.7.7 I/O PORT SWITCH REGISTER

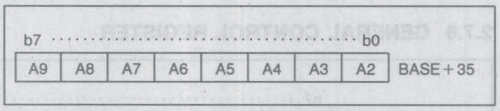


Figure 2-12. I/O Port Switch Register

The I/O Port Switch Register is an 8-bit read-only register located at BASE+35 hex. The contents of this register determines the I/O BASE when in ATMODE. This register is normally read during the execution of the POST ROM. The value of bits A9–A2 are compared against the host address bits A9–A2 by hardware. This register has no meaning when operating in non-ATMODE.

2.7.8 POST ADDRESS SWITCH REGISTER

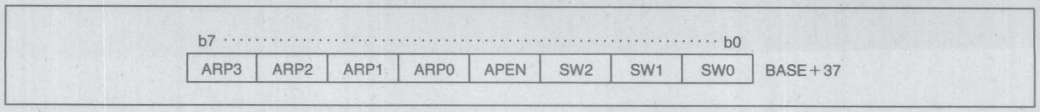


Figure 2-13. POST Address Switch Control Register

RESET VALUE	b7							b0	
80	1	EMS10	EMS9	EMS8	EMS7	EMS6	EMS5	EMS4	POS5 - BASE + 3A
00	EMS3	EMS2	EMS1	EMS0	VIS1	VIS0	AIS0	CIS0	POS4 - BASED + 38
01	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	EW3	PEN	POS3 - BASED + 36
30	RP3	RP2	RP1	RP0	EW2	EW1	EW0	CDEN	POS2 - BASE + 34
EF	MOST SIGNIFICANT ID BYTE								POS1 - BASE + 32
DC	LEAST SIGNIFICANT ID BYTE								POS0 - BASE + 30

Figure 2-14. HIGA Configuration Registers

The POST Address Switch Register is an 8-bit read-only register located at BASE + 37 hex. ARP3-ARP0 reflect the status of the POST Address Switches when in ATMODE. The APEN bit reflects the status of the POST ROM Enable Switch when in ATMODE. SW2–SW0 are definable switches also when in ATMODE. This register has no meaning when in non-ATMODE.

2.7.9 CONFIGURATION REGISTERS

Figure 2-14 shows the HIGA Configuration Registers for both the PS/2 and PC/AT implementations. The Configuration Registers are used to set the I/O port addresses (in non-ATMODE), the POST ROM address, the interrupt levels for the Audio Subsystem and the 82750PB and the EMS Window configuration. Additionally, the configuration registers contain one control bit (CDEN) used to enable and disable the entire board.

When in non-ATMODE the configuration registers are accessed as outlined in the respective PS/2 Technical Reference Manual. The registers can also be accessed via the I/O port path. The non-ATMODE mode prevents the writing of these registers through the I/O port path but not the reading of the registers.

When operating in ATMODE the configuration registers are accessed only through the I/O port addresses. The I/O port is contained in the I/O Port Switch Register. The configuration register POS3 has no meaning when in ATMODE, except for the EW3 and PEN bits. In addition, the RP0–3 bits in the configuration register POS2 have no meaning when in ATMODE. Instead, these parameters are set via switches on the board.

NOTE:
The POS registers on PS/2-based implementations should not be written by any of the software drivers or application code. The writing of POS registers is reserved exclusively for the IBM power-on configuration program. A possible exception to this would be the POST program that may disable the POST ROM after execution in order to create space for the EMS Window.

2.7.9.1 I/O Port BASE Address Determination

The I/O port BASEs in non-ATMODE differ slightly from the I/O port BASEs in ATMODE. Figure 2-15 illustrates the differences between the two systems. On the PS/2 (MicroChannel Bus), the host I/O address is mapped directly into the I/O BASE. Bits A10 through A15 are compared against POS3 register bits to select the I/O address range for the entire DVI Board. Bits A6 through A9 must be zeroes, while bits A0 through A5 select specific functions within the BASE.

A15	A14	A13	A12	A11	A10	A9 0	A8 0	A7 0	A6 0	A5	A4	A3	A2	A1	A0	non-ATMODE
A9	A8	A7	A6	A5	A4	A3	A2	A15 0	A14 0	A13	A12	A11	A10	A1	A0	ATMODE

Figure 2-15. DVI Board I/O Port Mapping

SET would be 36 hex for the POS3 register.

2.7.9.2 POS0

POS0 is an eight bit read/write register located at BASE+30 hex. When read, the eight bits in this register return the least significant byte of the DVI Board Identification during the PS/2 power on sequence. The value returned by this register is hard-wired in the HIGA. This register can be read in ATMODE through the appropriate I/O port.

POS0 is also used to enable and disable the EMS Window. Writing 55 hex to this register will enable the EMS Window, and writing 54 hex to this register will disable the EMS Window.

2.7.9.3 POS1

POS1 is an eight bit read-only register located at BASE+32 hex. The eight bits in this register return the most significant byte of the DVI Board Indentification during the PS/2 power on sequence. The value returned by this register is hard-wired in the HIGA. This register can be read in ATMODE through the appropriate I/O port.

2.7.9.4 POS2

POS2 is an eight bit read/write register located at BASE+34 hex. Each of the bits in this register is described below. POS2 is reset to 30 hex by system reset.

CDEN (Bit 0)—When the CDEN bit is a zero, the entire DVI Board is disabled. In non-ATMODE, the HIGA will not respond to I/O or memory addresses and will not drive the interrupt lines. In ATMODE the HIGA will not respond to memory addresses and will not drive the interrupt lines.

POS3 is an eight bit read/write register located at BASE+36 hex. POS3 is the I/O Port Address Configuration Register. In non-ATMODE, this register is used to set the I/O addresses for the BASE functions. Each of the bits in this register is described below. POS3 is reset to 01 hex by system reset.

PEN (Bit 0)—The PEN bit is used to open and close the POST ROM in the host's address space. When set to a 0, the space that was being used by the POST ROM can be reused for EMS Window space for VRAM.

EW3 (Bit 1)—The EW3 bit (along with EW0–2 in POS2) set the EMS Window mode. The EMS Window size can be one of 13 sizes ranging from 0 Mbytes to 16 Mbytes in size.

I/O2–7 (Bits 2–7)—The I/O7–I/O2 field is used to compare against the host's address bus bits A15–A10 respectively during I/O read or write operations when in non-ATMODE. If POS3 was initialized to C0 then the I/O port BASE would be set to C000. The I/O7–I/O2 bits have no meaning when operating in ATMODE.

2.7.9.6 POS4

POS4 is an eight bit read/write register located at BASE+38 hex. Each of the bits in this register is described below. POS4 is reset to zero by system reset.

CIS0 (Bit 0)—CIS0 is the Interrupt Level Select bit for the CDROM Subsystem interrupts. When CIS0 = 0, then the interrupt will be presented on the INT[1] pin. When CIS0 = 1, then the interrupt will be presented on the INT[2] pin.

AIS0 (Bit 1)—AIS0 is the Interrupt Level Select bit for the Audio Subsystem interrupts. When AIS0 = 0, then the interrupt will be presented on the INT[1] pin. When AIS0 = 1, then the interrupt will be presented on the INT[2] pin.

VIS0–1 (Bits 2–3)—VIS0 and VIS1 are the Interrupt Level Select bits for the 82750PB interrupts. Table 2-5 indicates where the interrupt will be presented for each combination of VIS0 and VIS1.

Table 2-5. 82750PB Interrupt Level Selection

VIS1	VIS0	Pin
0	0	IN[0]
0	1	IN[1]
1	0	IN[2]
1	1	IN[3]

EMS0–3 (Bits 4–7)—EMS0–3 (along with EMS4–10 in POS5) are used by the board to set the address of the EMS Window. The memory space is divided into 2048 8 Kbyte segments by the HIGA. The desired starting address (divided by 8192) of the EMS window would be written in POS5 and POS4 by the initialization software.

2.7.10 VGA TEST REGISTERS

VGA Test Register	3C7	(C03F) [3EE7]	VGA Test Register	3C6	(C03E) [3EE6]	BASE+3C
VGA Test Register	3C9	(C03D) [3EE4]	VGA Test Register	3C8	(C03C) [3EE4]	BASE+3E

Figure 2-16. VGA Test Registers

The VGA Test Registers are four 8-bit read/write registers located at BASE+3C hex, BASE+3D hex, BASE+3E hex and BASE+3F hex. These registers provide an alternate programming path for testing the DVI Board's VGA DAC. Port BASE+3C is the same register found at 03C7, Port BASE+3D is the same register found at 03C9, Port BASE+3E is the same register found at 03C6 and Port BASE+3F is the same register found at 03C8. The VGA Test Registers can be written or read at any time but should only be accessed with byte I/O operations. The (C03C)[33E4] type numbers in Figure 2-16 represent examples of I/O port addresses for (non-ATMODE) and [ATMODE] if the BASE was set to C000 or 02E4 respectively.

2.7.9.7 POS5

POS5 is an eight bit read/write register located at BASE+3A hex. Each of the bits in this register is described below. POS5 is reset to 80 hex by system reset.

EMS4–10 (Bits 0–6)—EMS4–10 (along with EMS0–3 in POS4) are used by the board to set the address of the EMS Window. The memory space is divided into 2048 8 Kbyte segments by the HIGA. The desired starting address (divided by 8192) of the EMS window would be written in POS5 and POS4 by the initialization software.

D7 (Bit 7)—D7 is used by the PS/2 error recovery system and is set by hardware to indicate "no error information available on this board". This bit should always be set to a one whenever POS5 is written.

3.0 HARDWARE INTERFACE

3.1 MicroChannel Interface Operation and Timing

MicroChannel host cycles consist of four types of cycles: Memory Read, Memory Write, I/O Read and I/O Write. Each of the four cycle types is explained in Figure 3-1. The HIGA meets all of the timing requirements for the MicroChannel Bus as published by IBM. Refer to any IBM PS/2 Technical Reference Manual for detailed explanations.

3.1.1 I/O READ

In the I/O Read cycle timing diagram pictured in Figure 3-1, CLK is the main timing source for the HIGA. The signals sources from the MicroChannel Bus are assumed to be completely asynchronous to the HIGA, therefore, CLK is used to synchronize the events on the MicroChannel Bus with internal HIGA operations.

The cycle is not considered valid until CMD# is active. At that time, the internal synchronizer starts to sample the cycle and turn the CMD# into a synchronous internal request for an operation. Also at that time, the internal host interface sequencer moves into state T1.

The internal operation starts at the beginning of the third CLK (T1) since CMD#, address, status, etc. were valid before the rising edge of that CLK period. During T2 and T3 the internal read operation takes place. At the end of T3 the internal read operation is completed, CHRDY is asserted and the internal host interface sequencer moves into state T4. The internal host interface sequencer repeats state T4 until the host negates CMD#.

The HIGA drives the data bus with valid data from the end of T3 (CHRDY) until CMD# is negated by the host (all T4's). If the operation required the use of the DVI Bus, additional T3's would have been inserted until the operation was completed. Examples of I/O operations that require the use of the DVI Bus are reading an empty read FIFO and writing a full write FIFO.

3.1.2 I/O WRITE

The I/O Write cycle timing diagram pictured in Figure 3-2 is basically the same as the I/O Read operation except the data bus is driven by the host. The data should be valid a minimum of 25 ns before T3 and should remain valid until CMD# is negated.

3.1.3 Memory Read

The Memory Read cycle in Figure 3-3 requires the use of the DVI Bus before it can be completed and therefore must be extended. The cycle is extended by inserting additional T3 states until MSTRB# is received, indicating valid data on the DVI Bus.

The number of CLK periods from BUSEN# active to CHRDY inactive is fixed by the programming of the memory timing in the VSCGA device. The number of CLK periods from BREQ# active to BUSEN# active is variable and depends on the activity of the 82750PB. This time is known as the DVI Bus latency and can be as long as one 82750PB Next-Fast cycle (NXTFST) plus one regular 82750PB memory cycle. This latency time is the main reason for the FIFOs in the HIGA. The FIFOs allow fast I/O Read or Write cycles on the host side while independently executing DVI Bus cycles on the DVI Bus side. The FIFOs can also stack host data into 32-bit and 64-bit DVI Bus cycles.

The operation and timing of a memory read to the POST ROM (an eight bit device) is different than the one shown in Figure 3-3 in two ways. First, the HIGA will not return the CDDS16# signal during POST ROM accesses. Second, special steering logic inside the HIGA logically connects the MD[7:0] lines to the SD[7:0] lines regardless of the byte address. Therefore, consecutive byte accesses do not progress from MD[7:0] to MD[15:8] to MD[23:16] when accessing the POST ROM.

Note that the MREQ# (82750PB) and RAS# (VSCGA) signals are not connected to the HIGA but nonetheless were thought to be useful signals to include in the timing diagrams.

3.1.4 MEMORY WRITE

The Memory Write cycle timing diagram pictured in Figure 3-4 is basically the same as the Memory Read operation except the SD(15:0) data bus is driven by the host.

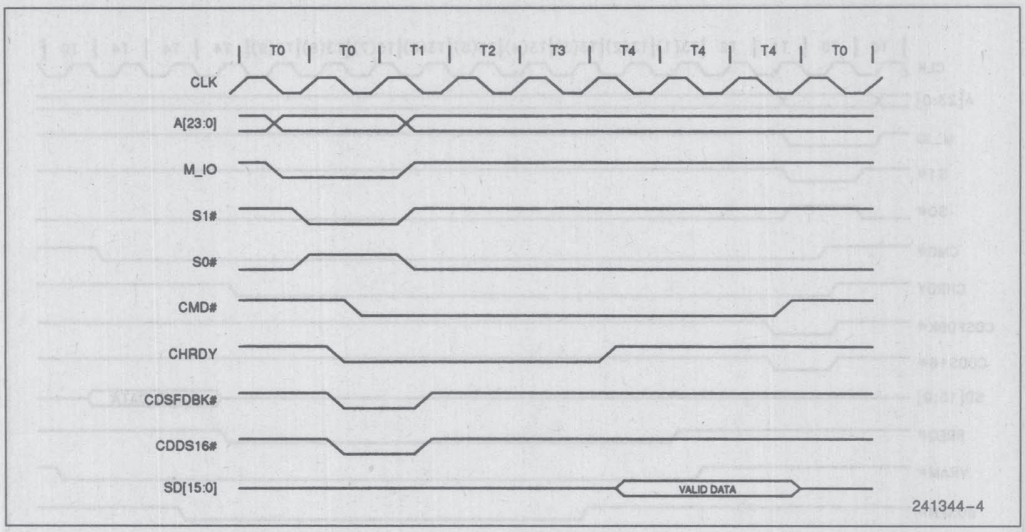


Figure 3-1. MicroChannel I/O Read Timing

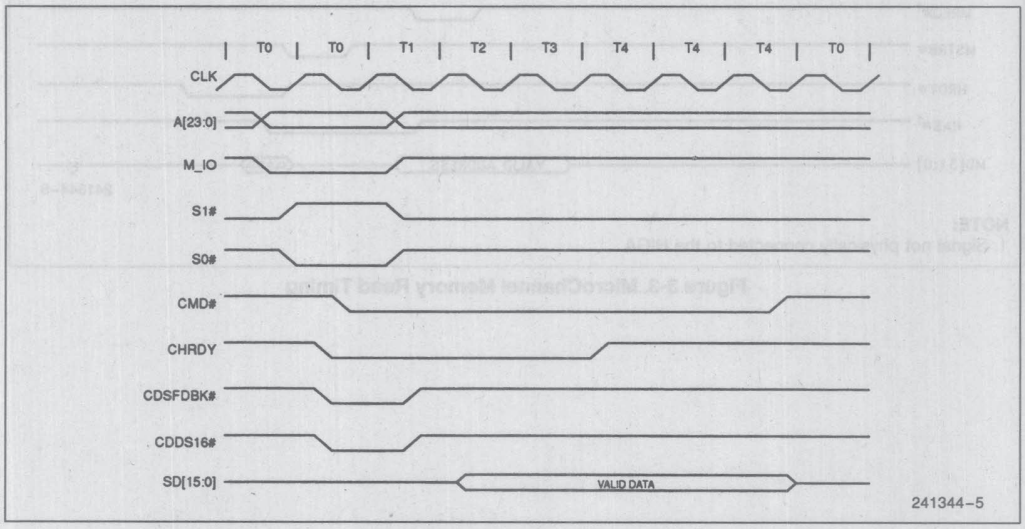
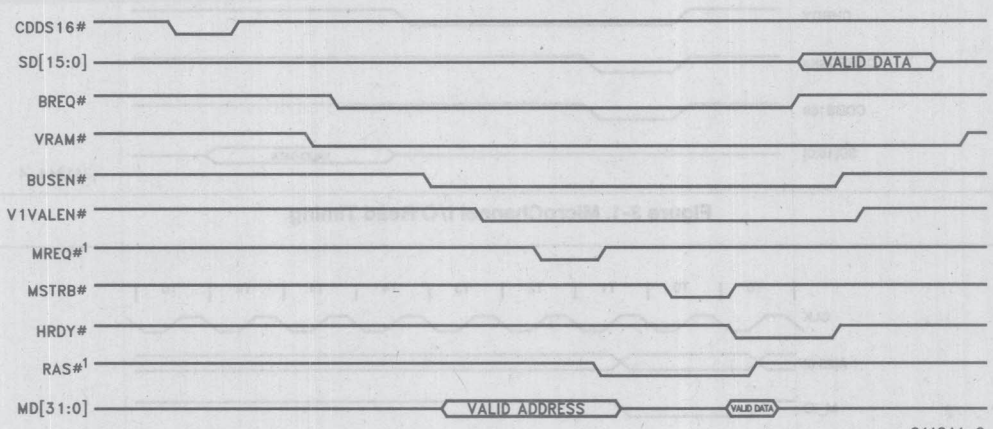
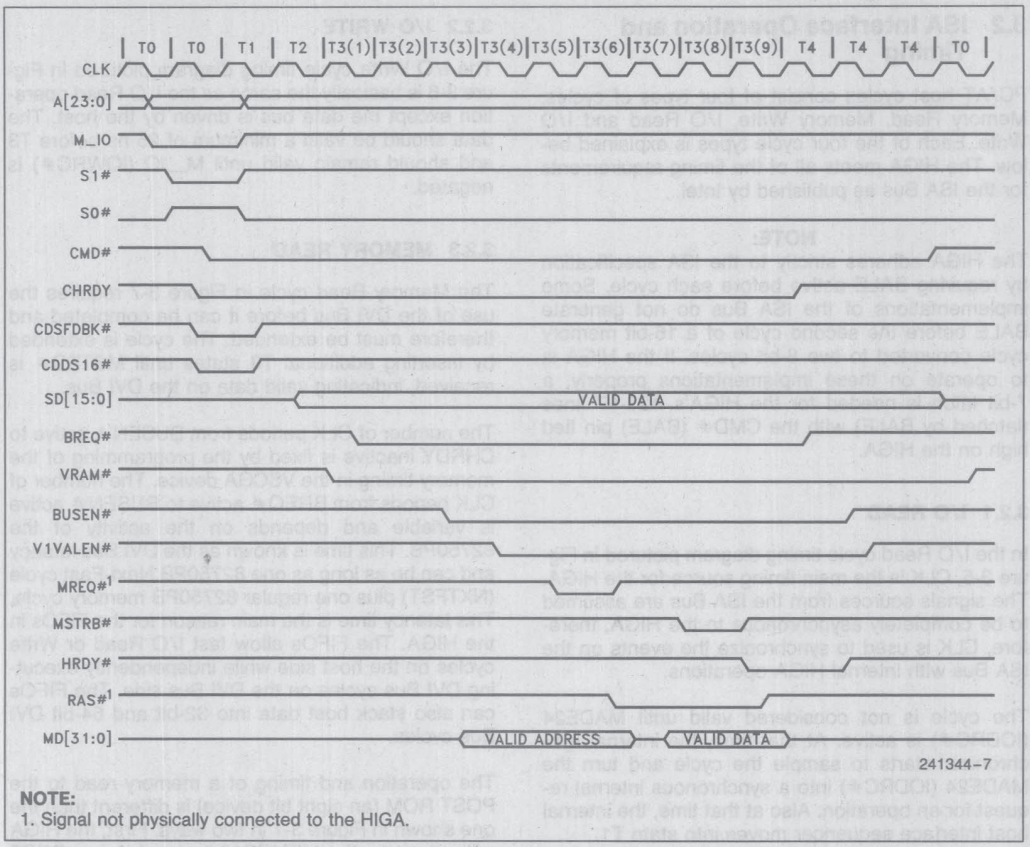


Figure 3-2. MicroChannel I/O Write Timing



NOTE:
1. Signal not physically connected to the HIGA.

Figure 3-3. MicroChannel Memory Read Timing



NOTE:
1. Signal not physically connected to the HIGA.

Figure 3-4. MicroChannel Memory Write Timing

3.2 ISA Interface Operation and Timing

PC/AT host cycles consist of four types of cycles: Memory Read, Memory Write, I/O Read and I/O Write. Each of the four cycle types is explained below. The HIGA meets all of the timing requirements for the ISA Bus as published by Intel.

NOTE:
The HIGA adheres strictly to the ISA specification by requiring BALE active before each cycle. Some implementations of the ISA Bus do not generate BALE before the second cycle of a 16-bit memory cycle converted to two 8-bit cycles. If the HIGA is to operate on these implementations properly, a 7-bit latch is needed for the HIGA's A23-17 lines (latched by BALE) with the CMD# (BALE) pin tied high on the HIGA.

3.2.1 I/O READ

In the I/O Read cycle timing diagram pictured in Figure 3-5, CLK is the main timing source for the HIGA. The signals sources from the ISA Bus are assumed to be completely asynchronous to the HIGA, therefore, CLK is used to synchronize the events on the ISA Bus with internal HIGA operations.

The cycle is not considered valid until MADE24 (IODRC#) is active. At that time, the internal synchronizer starts to sample the cycle and turn the MADE24 (IODRC#) into a synchronous internal request for an operation. Also at that time, the internal host interface sequencer moves into state T1.

The internal operation starts at the beginning of the third CLK (T1) since MADE24 (IODRC#), address, status, etc. were valid before the rising edge of that CLK period. During T2 and T3 the internal read operation takes place. At the end of T3 the internal read operation is completed, CHRDY is asserted and the internal host interface sequencer moves into state T4. The internal host interface sequencer repeats state T4 until the host negates MADE24 (IODRC#).

The HIGA drives the data bus with valid data from the end of T3 (CHRDY) until MADE24 (IODRC#) is negated by the host (all T4's). If the operation required the use of the DVI Bus, additional T3's would have been inserted until the operation was completed. Examples of I/O operations that require the use of the DVI Bus are reading an empty read FIFO—and wriiting a full write FIFO.

3.2.2 I/O WRITE

The I/O Write cycle timing diagram pictured in Figure 3-6 is basically the same as the I/O Read operation except the data bus is driven by the host. The data should be valid a minimum of 25 ns before T3 and should remain valid until M__IO (IOWRC#) is negated.

3.2.3 MEMORY READ

The Memory Read cycle in Figure 3-7 requires the use of the DVI Bus before it can be completed and therefore must be extended. The cycle is extended by inserting additional T3 states until MSTRB# is received, indicating valid data on the DVI Bus.

The number of CLK periods from BUSEN# active to CHRDY inactive is fixed by the programming of the memory timing in the VSCGA device. The number of CLK periods from BREQ# active to BUSEN# active is variable and depends on the activity of the 82750PB. This time is known as the DVI Bus latency and can be as long as one 82750PB Next-Fast cycle (NXTFST) plus one regular 82750PB memory cycle, This latency time is the main reason for the FIFOs in the HIGA. The FIFOs allow fast I/O Read or Write cycles on the host side while independently executing DVI Bus cycles on the DVI Bus side. The FIFOs can also stack host data into 32-bit and 64-bit DVI Bus cycles.

The operation and timing of a memory read to the POST ROM (an eight bit device) is different than the one shown in Figure 3-7 in two ways. First, the HIGA will not return the MEMCS16# signal during POST ROM accesses. Second, special steering logic inside the HIGA logically connects the MD[7:0] lines to the SD[7:0] lines regardless of the byte address. Therefor, consecutive byte accesses do not progress from MD[7:0] to MD[15:8] to MD[23:16] when accessing the POST ROM.

Note that the MREQ# (82750PB) and RAS# (VSCGA) signals are not connected to the HIGA but nonetheless were thought to be useful signals to include in the timing diagrams.

3.2.4 MEMORY WRITE

The Memory Write cycle timing diagram pictured in Figure 3-8 is basically the same as the Memory Read operation except the SD[15:0] data bus is driven by the host.

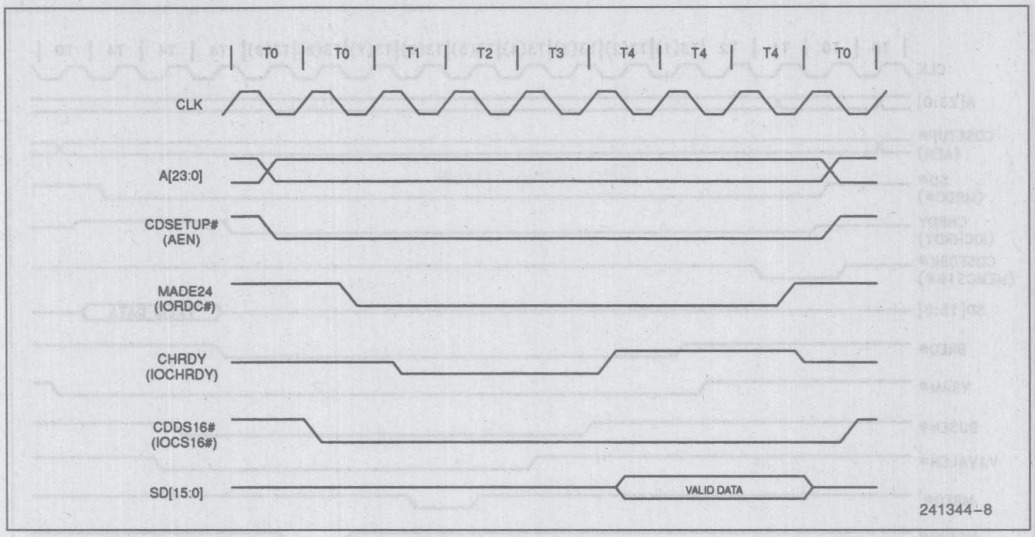


Figure 3-5. ISA I/O Read Timing

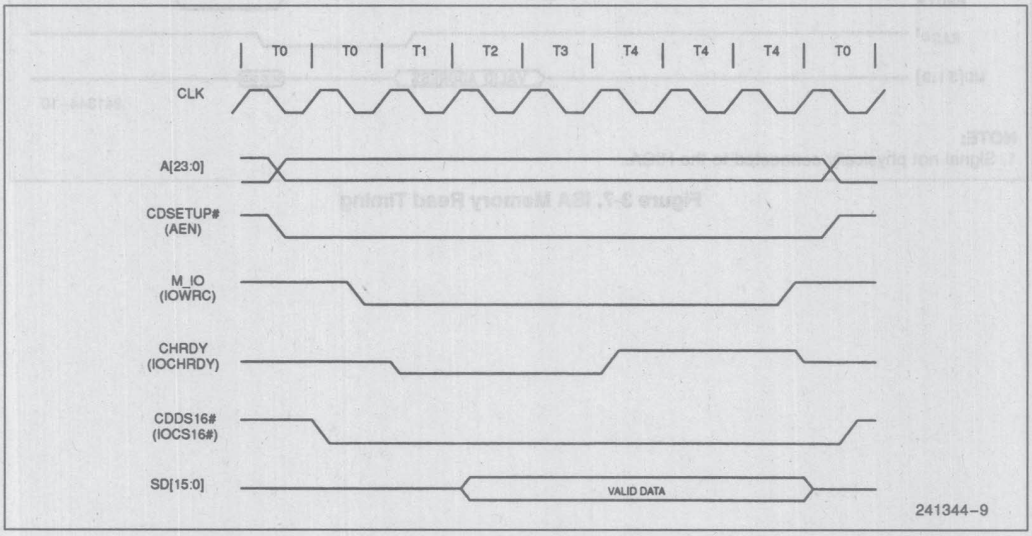
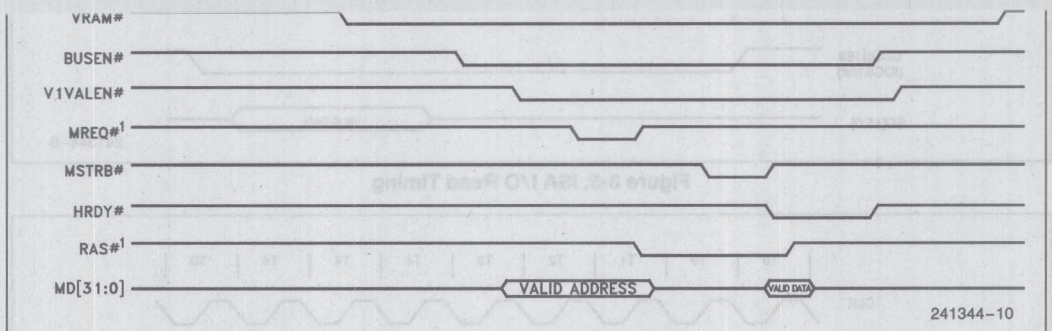
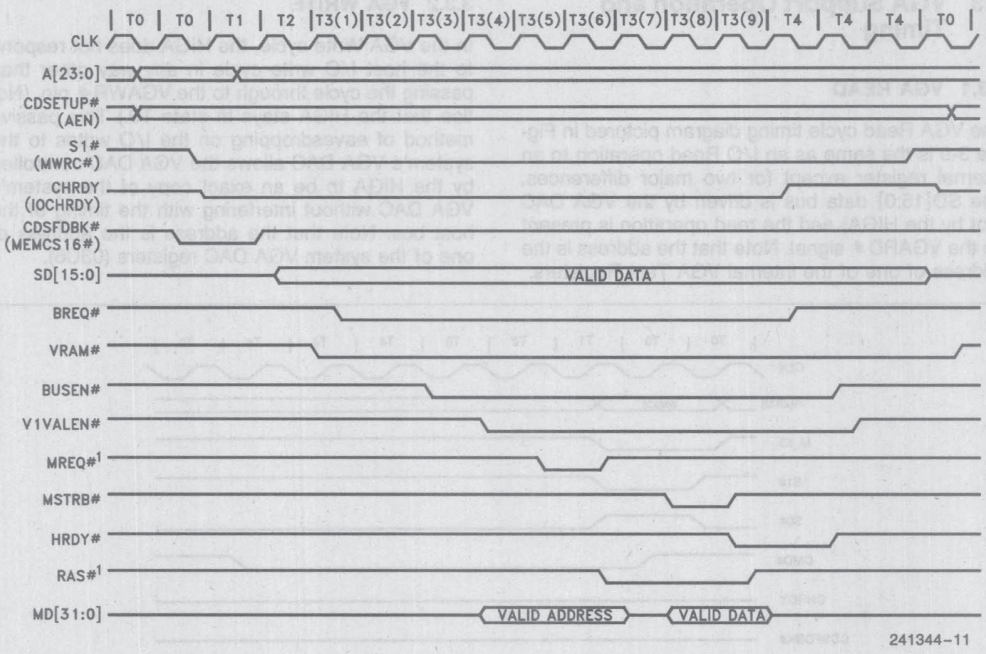


Figure 3-6. ISA I/O Write Timing



NOTE:
1. Signal not physically connected to the HIGA.

Figure 3-7. ISA Memory Read Timing



NOTE:
1. Signal not physically connected to the HIGA.

Figure 3-8. ISA Memory Write Timing

3.3 VGA Support Operation and Timing

3.3.1 VGA READ

The VGA Read cycle timing diagram pictured in Figure 3-9 is the same as an I/O Read operation to an internal register except for two major differences. The SD[15:0] data bus is driven by the VGA DAC (not by the HIGA) and the read operation is present on the VGARD# signal. Note that the address is the address of one of the internal VGA Test Registers.

3.3.2 VGA WRITE

In the VGA Write cycle, the HIGA does not respond to the host I/O write cycle in any way other than passing the cycle through to the VGAWR# pin. (Notice that the HIGA stays in state T0.) This passive method of eavesdropping on the I/O writes to the system's VGA DAC allows the VGA DAC controlled by the HIGA to be an exact copy of the system's VGA DAC without interfering with the timing of the host bus. Note that the address is the address of one of the system VGA DAC registers (03C6).

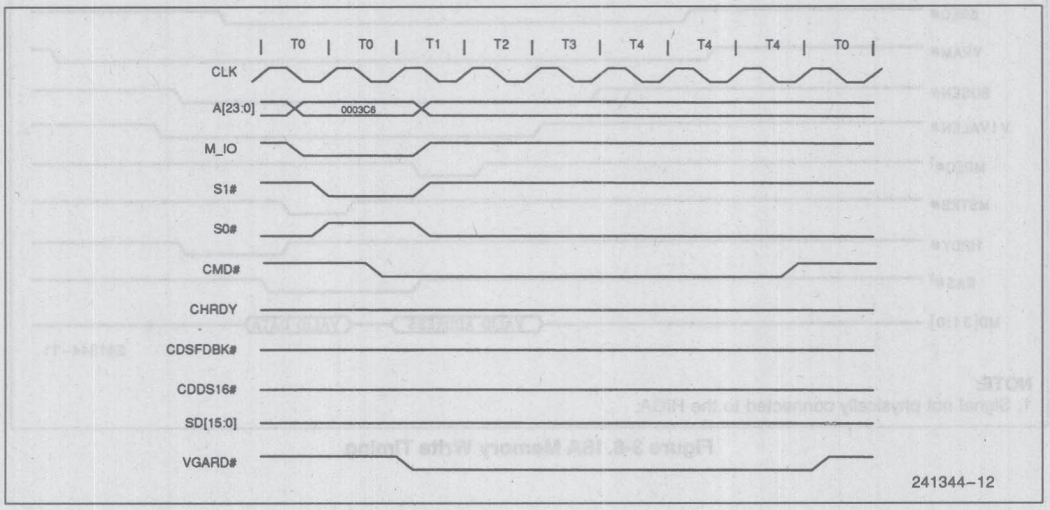


Figure 3-9. MicroChannel VGA Read Timing

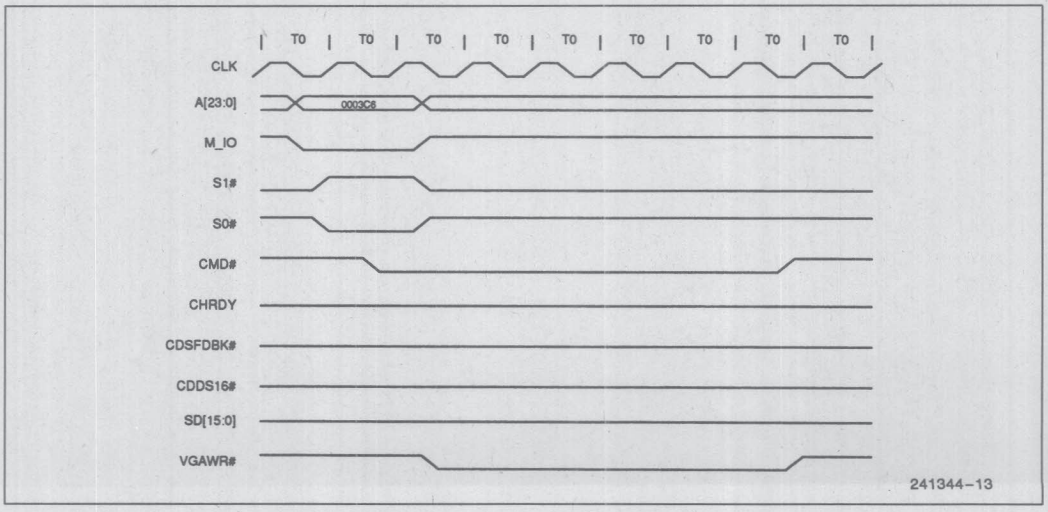


Figure 3-10. MicroChannel VGA Write Timing

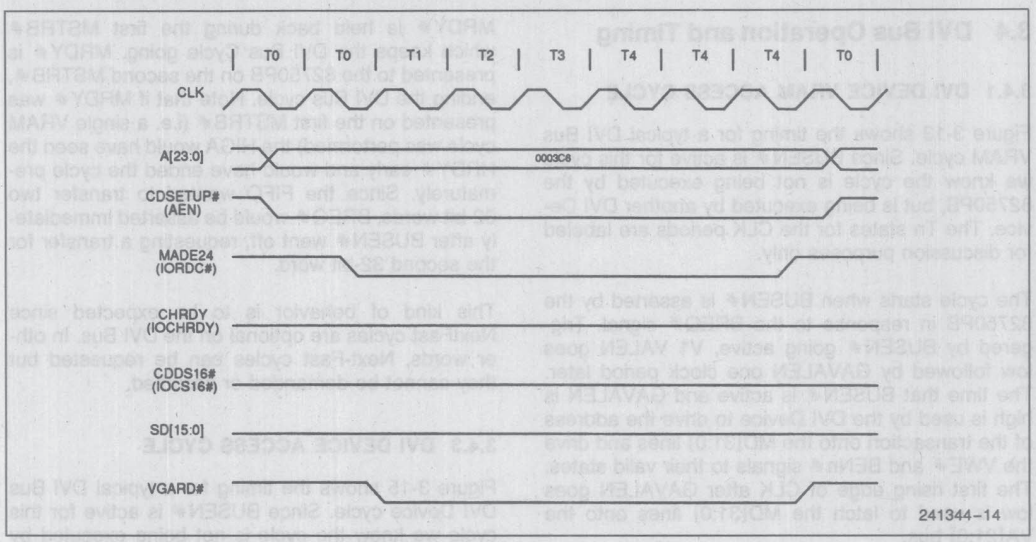


Figure 3-11. ISA VGA Read Timing

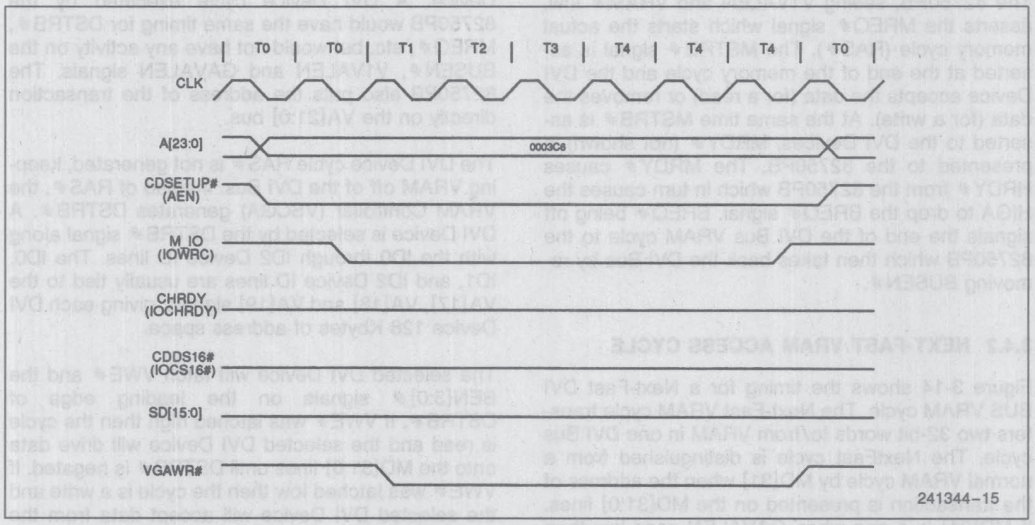


Figure 3-12. ISA VGA Write Timing

gered by BUSEN# going active, V1 VALEN goes low followed by GAVALEN one clock period later. The time that BUSEN# is active and GAVALEN is high is used by the DVI Device to drive the address of the transaction onto the MD[31:0] lines and drive the VWE# and BENn# signals to their valid states. The first rising edge of CLK after GAVALEN goes low is used to latch the MD[31:0] lines onto the VA[21:0] bus.

The 82750PB, seeing V1VALEN and VRAM# low, asserts the MREQ# signal which starts the actual memory cycle (RAS#). The MSTRB# signal is asserted at the end of the memory cycle and the DVI Device accepts the data (for a read) or removes the data (for a write). At the same time MSTRB# is asserted to the DVI Devices, MRDY# (not shown) is presented to the 82750PB. The MRDY# causes HRDY# from the 82750PB which in turn causes the HIGA to drop the BREQ# signal. BREQ# being off signals the end of the DVI Bus VRAM cycle to the 82750PB which then takes back the DVI Bus by removing BUSEN#.

3.4.2 NEXT-FAST VRAM ACCESS CYCLE

Figure 3-14 shows the timing for a Next-Fast DVI BUS VRAM cycle. The Next-Fast VRAM cycle transfers two 32-bit words to/from VRAM in one DVI Bus cycle. The NextFast cycle is distinguished from a normal VRAM cycle by MD[31] when the address of the transaction is presented on the MD[31:0] lines. If MD[31] is a one when GAVALEN goes low then the cycle will be a Next-Fast cycle. The FIFOs in the HIGA use the Next-Fast cycle to transfer 64 bits of information when possible.

The Next-Fast cycle is very similar to the single transfer VRAM cycle. When the Next-Fast cycle is executed the VRAM Controller (VSCGA) performs a two CAS page mode memory cycle instead of the single GAS memory cycle. The VRAM Controller also ORs on the VA[2] address line to increment the Column Address during the second CAS cycle. For this reason, all Next-Fast cycles must start on even 32-bit boundaries.

er words, Next-Fast cycles can be requested but they cannot be demanded or assumed.

3.4.3 DVI DEVICE ACCESS CYCLE

Figure 3-15 shows the timing for a typical DVI Bus DVI Device cycle. Since BUSEN# is active for this cycle we know the cycle is not being executed by the 82750PB, but is being executed by another DVI Device. A DVI Device cycle executed by the 82750PB would have the same timing for DSTRB#, MREQ#, etc. but would not have any activity on the BUSEN#, V1VALEN and GAVALEN signals. The 82750PB also puts the address of the transaction directly on the VA[21:0] bus.

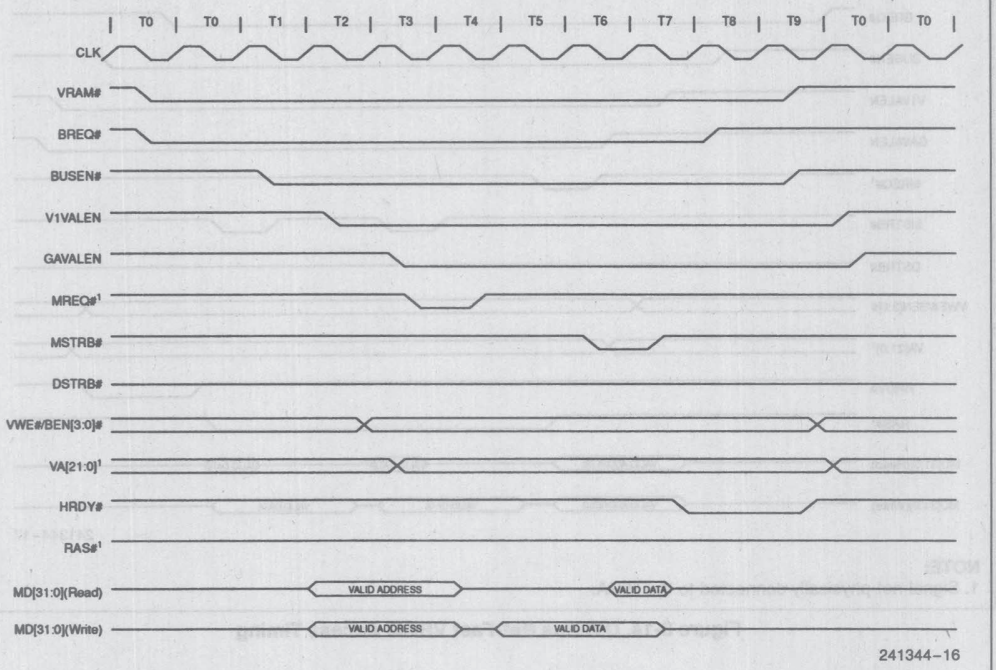
The DVI Device cycle RAS# is not generated, keeping VRAM off of the DVI Bus. Instead of RAS#, the VRAM Controller (VSCGA) generates DSTRB#. A DVI Device is selected by the DSTRB# signal along with the ID0 through ID2 Device ID lines. The ID0, ID1, and ID2 Device ID lines are usually tied to the VA[17], VA[18] and VA[19] signals, giving each DVI Device 128 Kbytes of address space.

The selected DVI Device will latch VWE# and the BEN[3:0]# signals on the leading edge of DSTRB#. If VWE# was latched high then the cycle is read and the selected DVI Device will drive data onto the MD[31:0] lines until DSTRB# is negated. If VWE# was latched low then the cycle is a write and the selected DVI Device will accept data from the MD[31:0] lines on the rising edge of CLK during MSTRB#. The length of DSTRB# (programmable in VSCGA) should be long enough to allow for the slowest DVI Device access time.

3.4.4 82750PB REGISTER ACCESS CYCLE

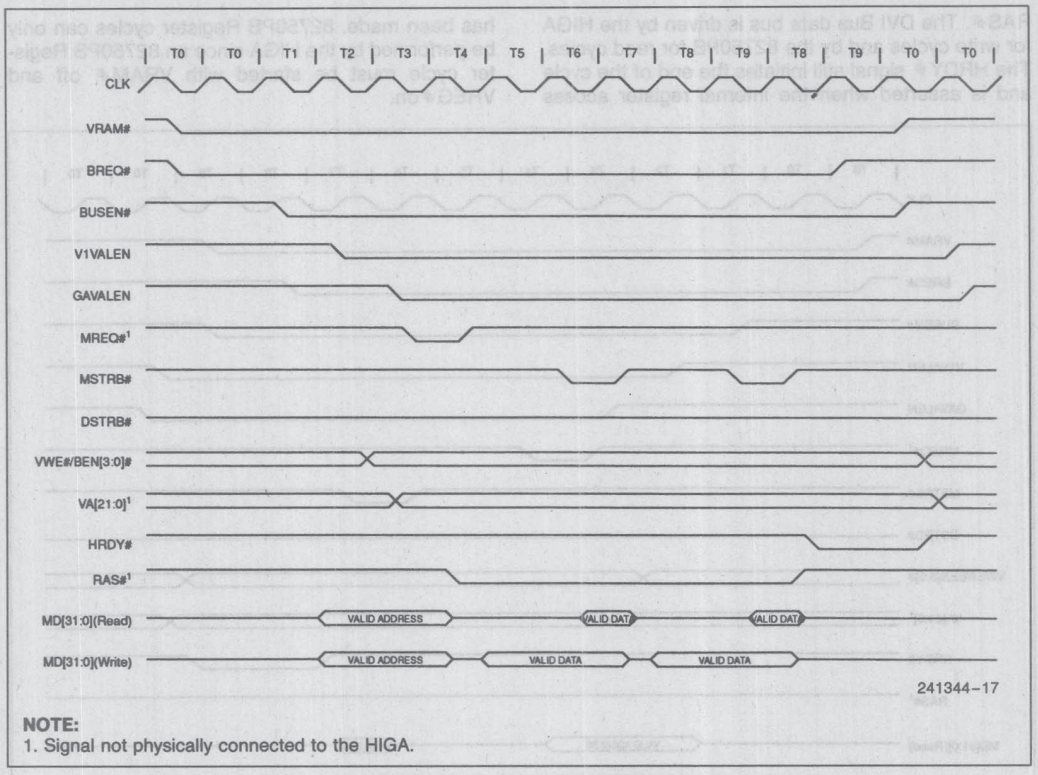
Figure 3-16 shows the timing for a typical DVI Bus 82750PB Register cycle. The 82750PB Register cycle is used to access internal registers in the 82750PB. The major differences in this type of cycle is the absence of MREQ#, MSTRB#, DSTRB# and

RAS#. The DVI Bus data bus is driven by the HIGA for write cycles and by the 82750PB for read cycles. The HRDY# signal still initiates the end of the cycle and is asserted when the internal register access has been made. 82750PB Register cycles can only be performed by the HIGA since an 82750PB Register cycle must be started with VRAM# off and VREG#on.



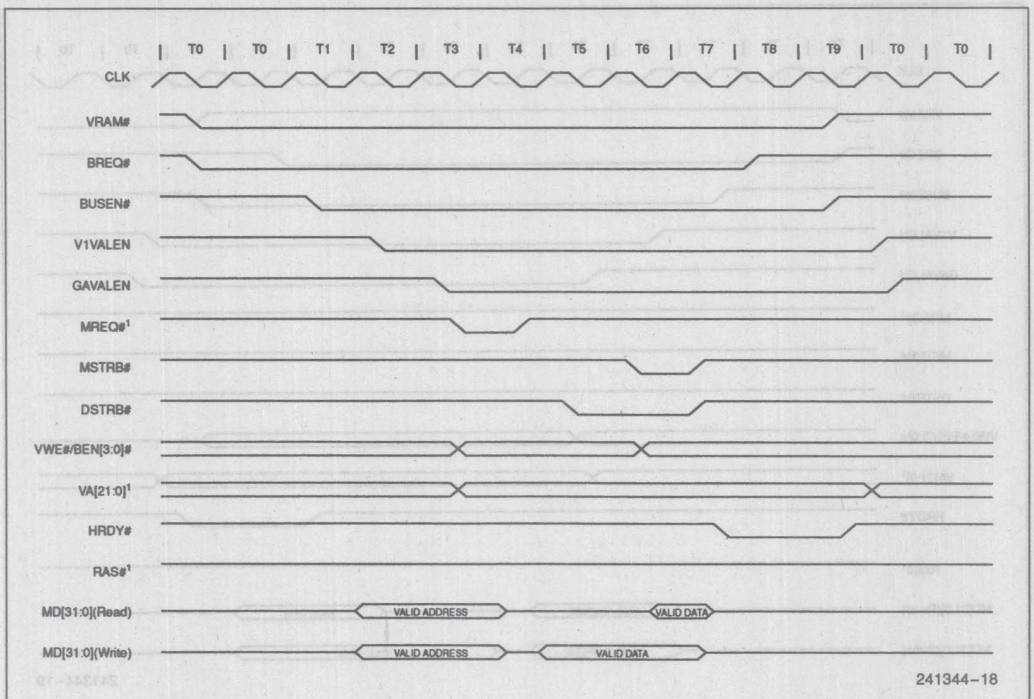
NOTE:
1. Signal not physically connected to the HIGA.

Figure 3-13. DVI Bus DVI Device VRAM Access Timing



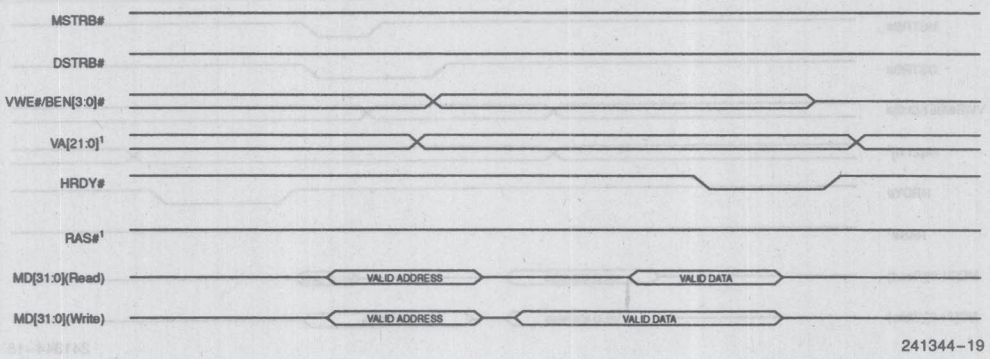
NOTE:
1. Signal not physically connected to the HIGA.

Figure 3-14. DVI Bus Net-Fast VRAM Access Timing



NOTE:
1. Signal not physically connected to the HIGA.

Figure 3-15. DVI Bus DVI Device Access Timing



NOTE:
1. Signal not physically connected to the HIGA.

Figure 3-16. DVI Bus 82750PB Register Access Timing

while the FIFO is trying to gain access to the DVI Bus the host can be writing additional bytes to the FIFO. If the FIFO becomes full before the first access is granted and the VRAM address is an even long-word address, then the access will turn into a Next-Fast VRAM cycle. The Next-Fast VRAM cycle will allow the FIFO to write both long-words in the same DVI Bus cycle. This action forces the FIFO to become more efficient as the DVI Bus gets busier.

The operation of the 32-Bit-Write FIFO can be modified and controlled through the programming of the 32-Bit-Write FIFO Control Register. To initialize the FIFO, the first write to the FIFO's control register should have the TEST bit set to a one. All subsequent writes to the control register should have the TEST bit reset to a 0. The FIFO's address counter is written or read with three I/O operations to the FIFO's Control Register and three I/O operations to the FIFO's Address Counter Byte Register. The FIFO Address Counter Bytes must be written in the order of low followed by middle followed by high. The low byte of the FIFO address counter is at RS=0, with the middle byte at RS=1 and the high byte at RS=2. The FIFO Control Register and the FIFO Address Counter Byte Register can be written with the same 16-bit I/O operation. The three FIFO Address Counter Bytes hold the 24-bit byte address of the destination of the FIFO data. The transfer of data can start and end on any byte boundary. The FIFO data high and low registers hold the data and can be written 8 bits or 16 bits at a time. However, when writing with byte operations, data high register must be written between any writes to the data low register.

The 16-Bit-Write FIFO is a low performance path from the host to all of the devices on the DVI Bus, including VRAM. The 16-Bit-Write FIFO has just one 16-bit buffer which is used to hold data while the FIFO waits for access to the DVI Bus.The 16-Bit-Write FIFO will dump its data registers into VRAM whenever the most significant byte of the data register is written. The operation of the 16-Bit-Write FIFO is very similar to that of the 32-Bit-Write FIFO de-

empty the updated bytes in the FIFO into VRAM. The programmer should wait until the FIFO is empty before accessing the FIFO after executing the Flush Command.

4.1.2 USING THE READ FIFOs

The 32-Bit-Read FIFO is a high performance path from VRAM to the host. The FIFO contains two long-word buffers designed to maximize the throughput of the host's bus and the DVI Bus. The FIFO will try to read the first two long-words of data as soon as the FIFO Address Counter is written. Assuming the FIFO is empty and the FIFO Address Counter is pointing to an even long-word address, the access will be a Next-Fast VRAM cycle. The Next-Fast VRAM cycle will allow the FIFO to read both long-words in the same DVI Bus cycle. (If a Next-Fast VRAM cycle is not possible, then the FIFO would require two DVI Bus cycles to fill the data buffers.) The host could now read all eight bytes from the FIFO without having additional wait states inserted.

While the host is reading bytes or words from the FIFO with I/O reads, the FIFO is busy trying to read long-words from VRAM in an effort to keep the FIFO full. The operation of the 32-Bit-Read FIFO can be modified and controlled through the programming of the 32-Bit-Read FIFO Control Register. To initialize the FIFO, the first write to the FIFO's control register should have the TEST bit set to a one. All subsequent writes to the conrol register should have the TEST bit reset to a 0. The FIFO's address counter is written or read with three I/O operations to the FIFO's Control Register and three I/O operations to the FIFO's Address Counter Byte Register. The FIFO Address Counter Bytes must be written in the order of low followed by middle followed by high. The low byte of the FIFO address counter is at RS=0, with the middle byte at RS=1 and the high byte at RS=2. The FIFO will fetch data immediately after the high Address Counter Byte is written. The FIFO Control Register and the FIFO Address Counter Byte Register can be written with the same 16-bit I/O operation. The three FIFO Address Counter

Bytes hold the 24-bit byte address of the destination of the FIFO data. The FIFO data registers hold the read data.

The 16-Bit-Read FIFO is a low-performance path from all of the devices on the DVI Bus, including VRAM to the host. The 16-Bit-Read FIFO has just one 16-bit buffer which is used to hold data while the FIFO waits for the host to read the data. Operation of the 16-Bit-Read FIFO is very similar to that of the 32-Bit-Read FIFO described above except that the data is now processed in 16-bit pieces.

Both read FIFOs can be put into an Auto-increment Mode by setting the AUTO bit in the corresponding FIFO Control Register. When in Auto-increment Mode the VRAM address pointer is incremented after each access through the FIFO. The Read FIFOs will not prefetch data unless they are in the Auto-increment Mode. When not in the Auto-increment Mode, the FIFO's VRAM pointer will remain unchanged following the access. Accessing the Read FIFOs when empty will cause inserted wait states until the FIFO has data.

4.2 Programming the VRAM Modes

The EMS10–0 bits in the POS4 and POS5 registers set the location of the EMS Window while the EW3–0 bits in POS2 and POS3 set the EMS Window size. After power-on or Board Reset the EMS Window is disabled. To enable the EMS Window, 55 hex must be written to POS2 (BASE+30). The EMS Window can be disabled either by writing 54 hex to POS0, or by selecting EMS Mode F, or by executing a Board Reset. The remainder of this section explains the operating modes of the EMS logic and in some cases gives examples of POS register settings.

Figure 4-1 shows the 0K byte EMS Window Mode or Mode F. Mode F is selected by writing an F value to the four EW3–0 bits in POS2 and POS3. The location of the EMS Window will not affect the operation of the board in the mode since the host address bus is logically disconnected from the VRAM address bus. It is impossible for the host to access VRAM through its memory address space if the board is in this mode.

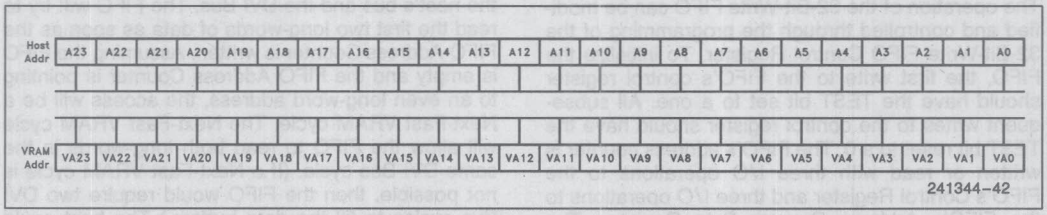


Figure 4-1. OK Byte EMS Window Mode—Mode F

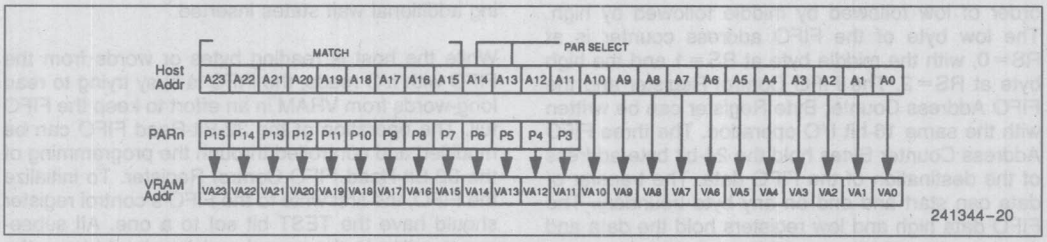


Figure 4-2. 8K Byte EMS Window Mode—Mode 0

Figure 4-2 shows the 8 Kbyte EMS Window Mode or Mode 0. Mode 0 is selected by writing a 0 value to the four EW3–0 bits (as a four bit field) in POS2 and POS3. The location of the EMS Window is determined by the EMS10–0 bits in POS4 and POS5. Since the EMS10–0 bits select on which 8K boundary the EMS Window begins and an 8K Window size must start on an 8K boundary, any value in the EMS10–0 bits would be logically correct. If the EMS10–0 bits are written with a 68 hex value (as an 11-bit field), then the EMS Window would start at host location D0000, because 68 hex x 2000 hex (i.e. 8K) is D0000.

In EMS Window Mode 0 the EMS Window is divided into four 2K byte pages controlled by four different Page Address Registers or PARs. The decode of host address bits A11 and A12 determines the PAR used during the access. The PARs are actually 16-bit registers although only bits P3 through P15 are used in the 8K Mode. The VRAM address generated by the host access is determined by the contents of the selected PAR as well as the state of the host's address bus, as is shown in the figure above. The Match Field in the same figure defines the bits of the host's address bus that must match the EMS10–0 bits.

The Page Address Registers (PARs) are used in combination with the host's address bus to generate the VRAM address bus. In each EMS Mode only the necessary top bits of the PARs are used. The remaining bits in the PARs can be written with any value without affecting the operation of the board.

As an example, in order to access the registers in DVI Device 5 which begin at FA0000, a PAR is written with FA00. The particular PAR used is dependent on the desired host address because the PARs are always selected by bits on the host's address bus. The FA00 value will work in any EMS Mode since in each EMS Mode only the necessary top bits of the PARs are used. The PARs can be written and read with either byte I/O or word I/O operations.

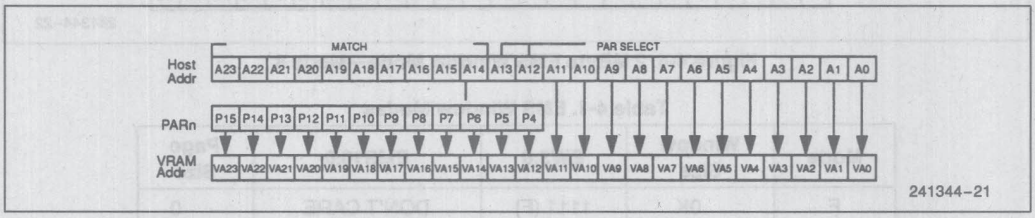


Figure 4-3. 16 KByte EMS Window Mode—Mode 1

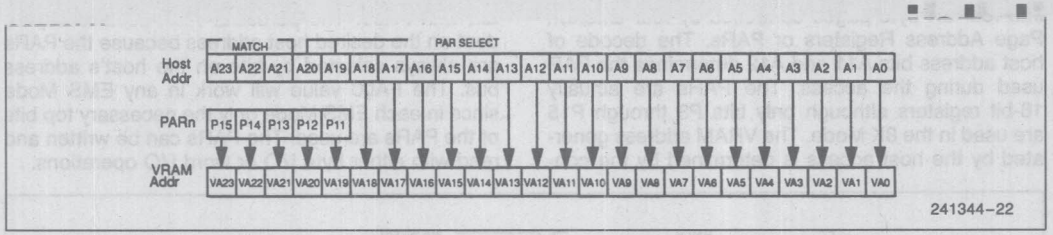


Figure 4-4. 2 MByte EMS Window Mode—Mode 8

Table 4-1. EMS Window Modes

Mode	Window Size	EW3:0	EMS10:0	Page Size
F	0K	1111 (F)	DON'T CARE	0
0	8K	0000 (0)	NNNNNNNNNN	2K
1	16K	0001 (1)	NNNNNNNNN0	4K
2	32K	0010 (2)	NNNNNNNNN00	8K
3	64K	0011 (3)	NNNNNNNN000	16K
4	128K	0100 (4)	NNNNNNN0000	32K
5	256K	0101 (5)	NNNNNN00000	64K
6	512K	0110 (6)	NNNNN000000	128K
7	1M	0111 (7)	NNNN0000000	256K
8	2M	1000 (8)	NNN00000000	512K
9	4M	1001 (9)	NN000000000	1M
A	8M	1010 (A)	N0000000000	2M
B	16M	1011 (B)	00000000000	4M

4.3 Using the Power-On-Self-Test ROM

The Power-On-Self-Test ROM or POST ROM is a single 64 Kbyte ROM that is page mapped through a fixed size EMS Window in the memory address space between 0C0000 hex and ODFFFF hex. On 8 Kbyte boundaries, any single ROM can appear in any one of the sixteen 8 Kbyte pages from 0C0000 hex to ODE000 hex. In non-ATMODE, the POST ROM's address space is determined by the ROM Page Select bits in the HIGA's POS2 register (RP0–RP3). In ATMODE, the POST ROM's address space is determined by the ROM Page Select Register. For both types of systems, the 1 of 8 POST ROM selection is done with the ROM Select bits in the ROM 8K Select Register and is set to select ROM 0 by RESET. A POST ROM Enable bit in the POS3 register can be used to disable the POST ROM. When disabled, the DVI Board will not respond to memory accesses in the POST ROM address space. The POST ROM is enabled by RESET, but can be disabled by writing the POS3 register in non-ATMODE. In ATMODE, the ROM Enable Switch or the POS3 register can be used to disable the POST ROM.

5.0 ELECTRICAL DATA

5.1 D.C. Characteristics

Maximum Ratings

Table 5-1 contains stress ratings only, and functional operation at the maximums is not guaranteed. Exposure to Maximum Ratings may affect device reliability. Furthermore, although the 82750LH contains protective circuitry to resist damage from static electrical discharge, this device is sensitive to ESD levels above 1000V. Always take precautions to avoid high static voltages or electric fields.

Table 5-1. Maximum Ratings

Condition	Maximum Requirement
Maximum Operating Junction Temperature	100°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin with Respect to Ground	−0.5V to +7V
Supply Voltage with Respect to V_{SS}	−0.5V to +7V
Input Current Clamp ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output Current Clamp ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous Output Current Low	20 mA
Continuous Output Current High	20 mA

Table 5-2. Recommended Operating Conditions

Parameter	Recommended Condition		
	Min	Nom	Max
Supply Voltage (V_{CC})	4.50V	5.0V	5.50V
Operating Temperature Range	0°C		70°C

Table 5-3. D.C. Characteristics V_{CC} = 5V, T_{CASE} = 25°C

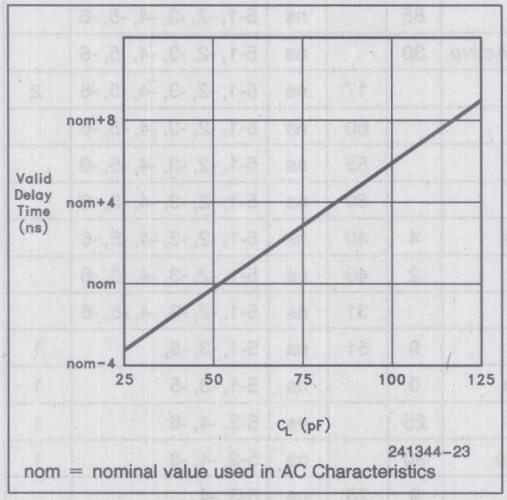
Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IL}	Input LOW Voltage			0.8	V	V_{CC} = 4.5V
V_{IH}	Input HIGH Voltage	2.0			V	V_{CC} = 5.5V
V_{OL}(1)	Output LOW Voltage			0.5	V	V_I = 0.1 V_{CC}, I_{OL} = 4 mA
V_{OL}(2)	Output LOW Voltage			0.5	V	V_I = 0.1 V_{CC}, I_{OL} = 16 mA
V_{OL}(3)	Output LOW Voltage			0.5	V	V_I = 0.1 V_{CC}, I_{OL} = 20 mA
V_{OH}(1)	Output HIGH Voltage	3.7			V	V_I = 0.9 V_{CC}, I_{OH} = 4 mA
V_{OH}(2, 3)	Output HIGH Voltage	3.7			V	V_I = 0.9 V_{CC}, I_{OH} = 12 mA
I_{IL}(4)	Input Leakage Current		−70		μA	V_{IL} = 0V
I_{IL}(5)	Input Leakage Current		±1		μA	V_{IL} = 0V
I_{OZ}(6)	Output Leakage Current		−70		μA	V_O = 0V
I_{OH}(1)	Output HIGH Current			4	mA	
I_{OH}(2, 3)	Output HIGH Current			12	mA	
I_{OL}(1)	Output LOW Current			4	mA	
I_{OL}(2)	Output LOW Current			16	mA	
I_{OL}(3)	Output LOW Current			20	mA	
I_{CC}	Power Supply Current		15		mA	
C_{IN}	Input Capacitance			7	pF	
C_{OUT}	Output Capacitance			34	pF	
V_T(7)	Input Threshold Voltage		1.3		V	

NOTES:
1. All output and bidirectional pins except INT[3:0]#, CDDS16#, CHRDY, CDSFDBK#, SD[15:0].
2. INT[3:0], CDDS16#, CHRDY, CDSFDBK# only.
3. SD[15:0] only.
4. All input pins except RESET, M_IO, S1#, S0#, MADE24, TESTPIN.
5. RESET M_IO, S1#, S0#, MADE24, TESTPIN.
6. Specified for MD[31:0], VWE#, BEN[3:0]# only.
7. Specified for all input pins except RESET, M_IO, S1#, S0#, MADE24.

Table 5-4. CLK D.C. Characteristics V_{CC} = 5V, T_{CASE} = 25°C

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IL}	Input LOW Voltage			0.9	V	V_{CC} = 4.5V
V_{IH}	Input HIGH Voltage	3.85			V	V_{CC} = 5.5V
I_{IL}	Input LOW Leakage			±1	μA	V_{IH} = V_{CC}
I_{IH}	Input HIGH Leakage			±1	μA	V_{IL} = 0V
V_T	Input Threshold Voltage		2.5		V	
C_{IN}	Input Capacitance			7	pF	

Output Delay and Rise Time Versus Load Capacitance



nom = nominal value used in AC Characteristics

Figure 5-1. Typical Output Valid Delay versus Load Capacitance

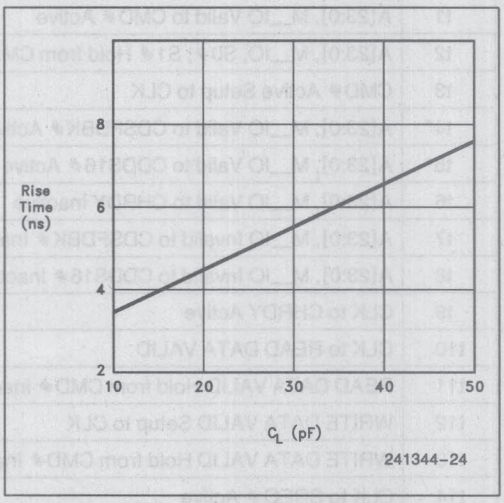


Figure 5-2. Typical Output Rise Time versus Load Capacitance

t3	CMD# Active Setup to CLK		17	ns	5-1, -2, -3, -4, -5, -6	2
t4*	A[23:0], M__IO Valid to CDSFDBK# Active		60	ns	5-1, -2, -3, -4, -5, -6	
t5*	A[23:0], M__IO Valid to CDDS16# Active		55	ns	5-1, -2, -3, -4, -5, -6	
t6	A[23:0], M__IO Valid to CHRDY Inactive		60	ns	5-1, -2, -3, -4, -5, -6	
t7	A[23:0], M__IO Invalid to CDSFDBK# Inactive	4	40	ns	5-1, -2, -3, -4, -5, -6	
t8	A[23:0], M__IO Invalid to CDDS16# Inactive	2	40	ns	5-1, -2, -3, -4, -5, -6	
t9	CLK to CHRDY Active		31	ns	5-1, -2, -3, -4, -5, -6	
t10	CLK to READ DATA VALID	9	51	ns	5-1, -3, -5,	1
t11	READ DATA VALID Hold from CMD# Inactive	0		ns	5-1, -3, -5	1
t12	WRITE DATA VALID Setup to CLK	25		ns	5-2, -4, -6	1
t13	WRITE DATA VALID Hold from CMD# Inactive	30		ns	5-2, -4, -6	1
t14	CLK to BREO# Active	9	28	ns	5-3, -4	
t15	CMD# Active to VRAM# Active	4	40	ns	5-3, -4	
t16	CMD# Active to VGARD# Active		35	ns	5-5	
t17	CMD# Inactive to VGARD# Inactive	7		ns	5-5	
t18	CMD# Active to VGAWR# Active		34	ns	5-6	
t19	CMD# Inactive to VGAWR# Inactive	7		ns	5-6	

NOTES:
1. Measured with C_L = 100 pF on SD[15:0].
2. CMD# is asynchronous. CMD# setup time is specified only to guarantee timing shown.

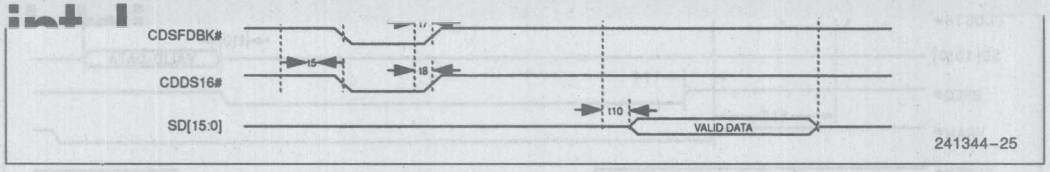


Figure 5-1. MicroChannel I/O Read AC Timing

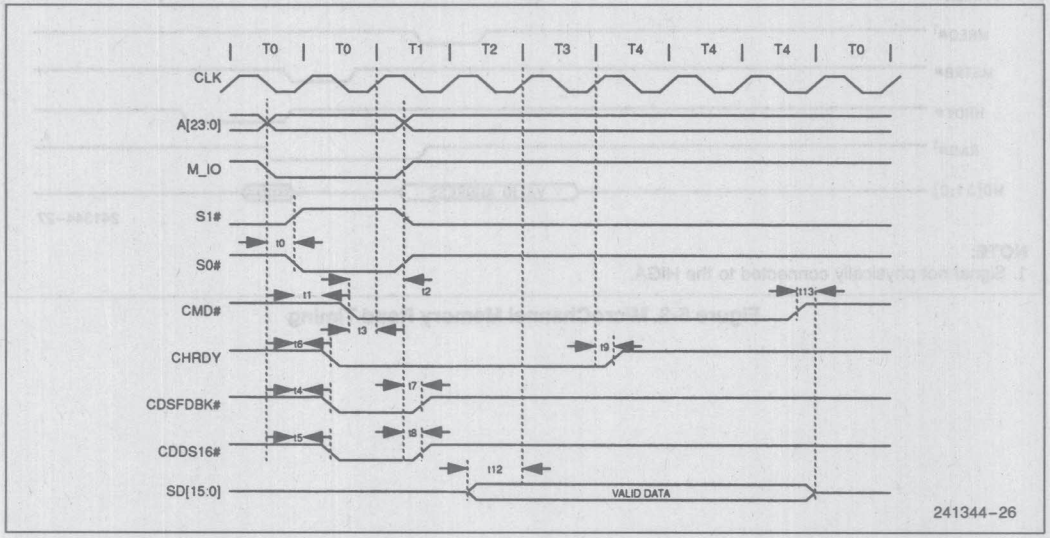
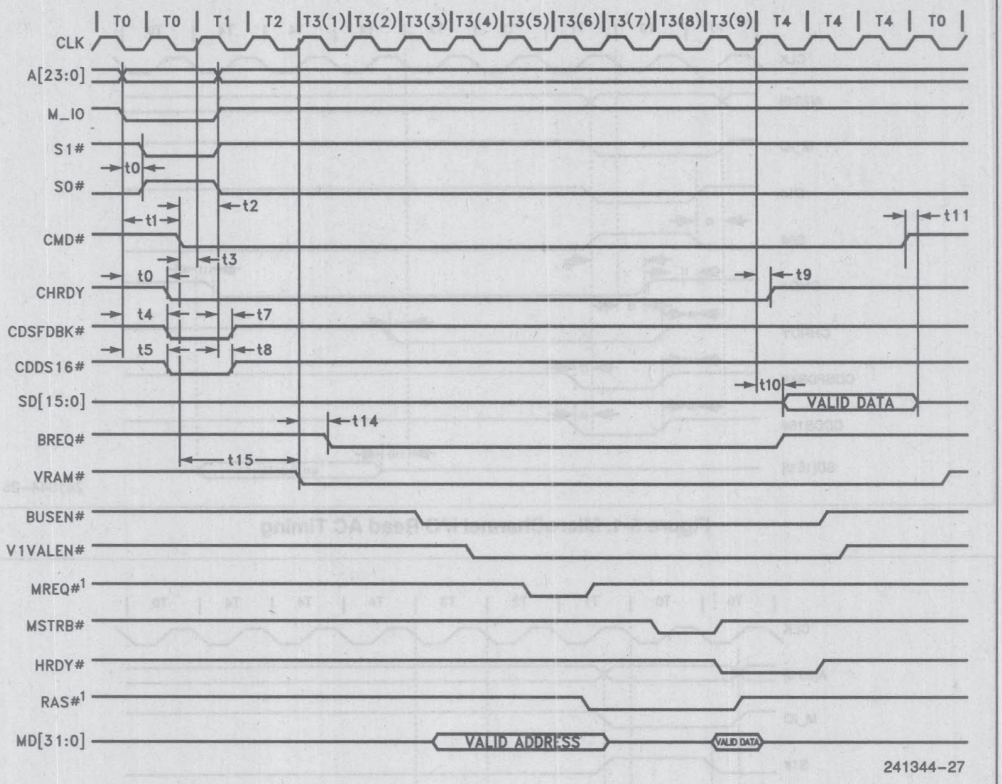
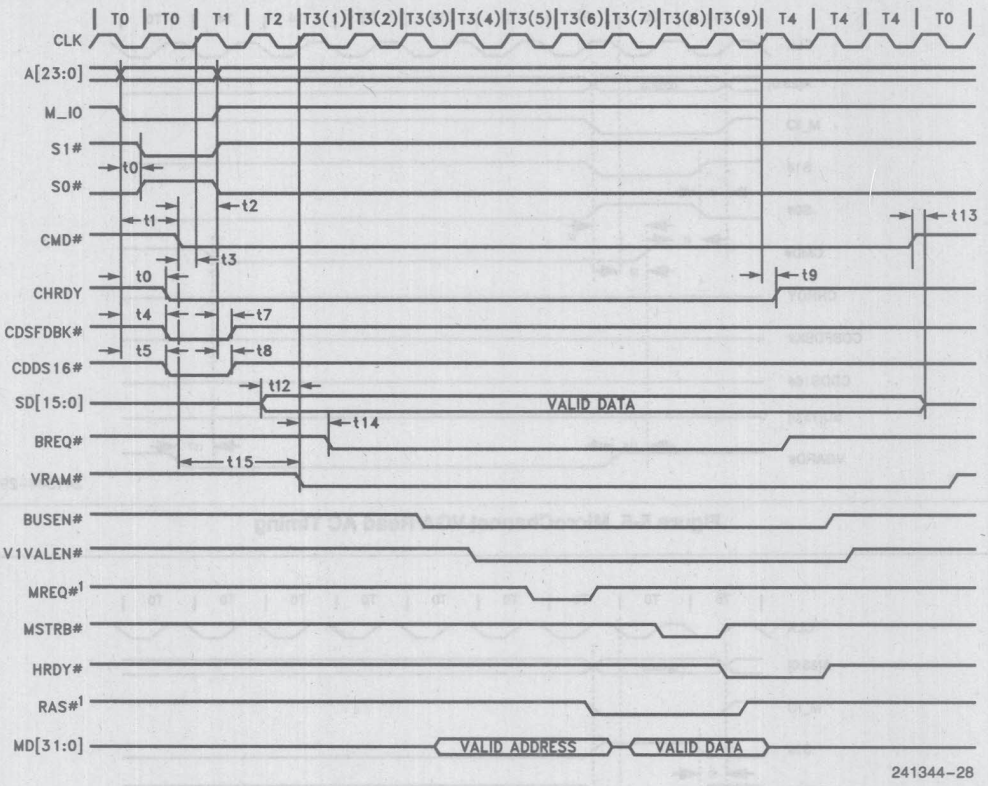


Figure 5-2. MicroChannel I/O Write AC Timing



NOTE:
1. Signal not physically connected to the HIGA.

Figure 5-3. MicroChannel Memory Read Timing



NOTE:
1. Signal not physically connected to the HIGA.

Figure 5-4. MicroChannel Memory Write AC Timing

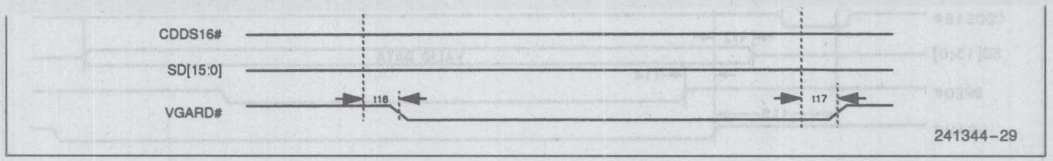


Figure 5-5. MicroChannel VGA Read AC Timing

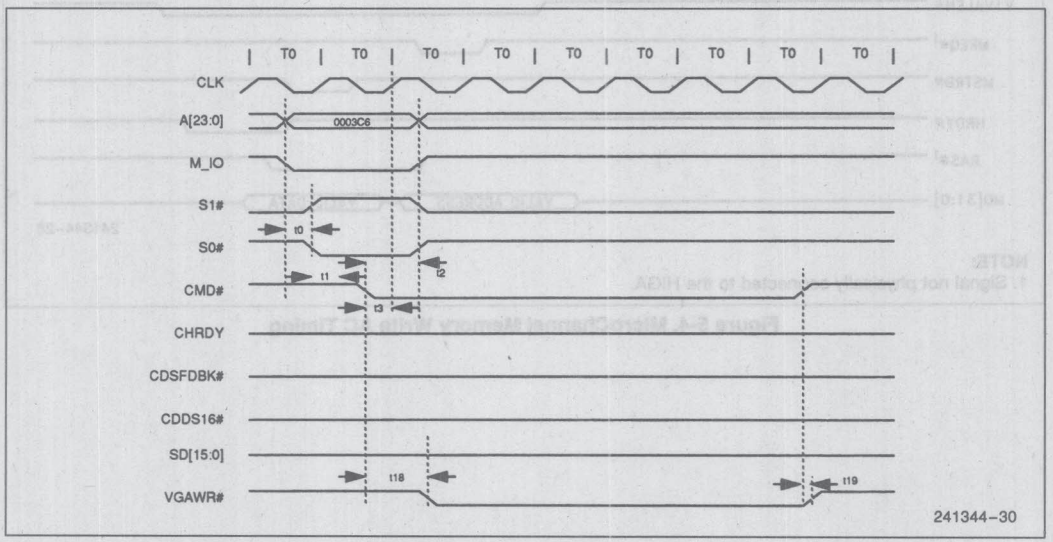


Figure 5-6. MicroChannel VGA Write AC Timing

5.2.2 ISA BUS INTERFACE TIMING

Table 5-6. ISA Bus Interface AC Characteristics

Symbol	Parameter	Min	Max	Units	Figure	Note
t0	A[23:0], CDSETUP# (AEN) Valid to MADE24 (IORDC#) Inactive	25		ns	5-7, -11	
t1	MADE24 (IORDC#) Inactive to CHRDY (IOCHRDY) Inactive		26	ns	5-7, -8, -11, -12	
t2	A[23:0], CDSETUP# (AEN) Valid to CDDS16# (IOCS16#) Active		30	ns	5-7, -8, -9, -10, -11, -12	
t3	CLK to CHRDY (IOCHRDY) Active		31	ns	5-7, -8, -9, -10, -11, -12	
t4	CLK to READ DATA VALID	9	51	ns	5-7, -9, -11	
t5	A[23:0] CDSETUP# (AEN) Hold from MADE24 (IORDC#) Active	5		ns	5-7, -11	
t6	MADE24 (IORDC#) Active to CHRDY (IOCHRDY) Invalid	7	26	ns	5-7, -11	
t7	READ DATA VALID Hold from MADE24 (IORDC#) Active	0		ns	5-7, -11	1
t8	SD[15:0] Tri-State from MADE24 (IORDC#) Active		30	ns	5-7, -11	
t9	A[23:0] CDSETUP# (AEN) Invalid to CDDS16# Inactive	5	30	ns	5-7, -8, -11, -12	
t10	A[23:0], CDSETUP# (AEN) Valid to M__IO (IOWRC#) Inactive	25		ns	5-8, -12	
t11	M__IO (IOWRC#) Inactive to CHRDY (IOCHRDY) Inactive		25	ns	5-8, -12	
t12	WRITE DATA VALID Setup to CLK	25		ns	5-8, -12	
t13	A[23:0] CDSETUP# (AEN) Hold from M__IO (IOWRC#) Active	10		ns	5-8, -12	
t14	M__IO (IOWRC#) Active to CHRDY (IOCHRDY) Invalid		25	ns	5-8, -12	
t15	WRITE DATA VALID Hold from M__IO (IOWRC#) Active	32		ns	5-8, -12	1
t16	SD[15:0] Tri-State from M__IO (IOWRC#) Active		30	ns	5-8, -12	
t17	A[23:0], CDSETUP# (AEN) Valid Setup to S0# (MRDC#) Active	39		ns	5-9	
t18	A[23:0] Valid Hold from S0# (MRDC#) Active	22		ns	5-9	
t19	S0# (MRDC#) Active to CHRDY (IOCHRDY) Inactive		39	ns	5-9	

Table 5-6. ISA Bus Interface AC Characteristics (Continued)

Symbol	Parameter	Min	Max	Units	Figure	Note
t20	A[23:0] Invalid to CDSFDBK# (MEMCS16#) Inactive	0		ns	5-9, -10	
t21	CLK to BREQ# Active	9	28	ns	5-9	
t22	CDSETUP# (AEN) Valid Hold from S0# (MRDC#) Inactive		8	ns	5-9	
t23	S0# (MRDC#) Inactive to CHRDY (IOCHRDY) Invalid	8	39	ns	5-9	
t25	READ DATA VALID Hold from S0# (MRDC#) Inactive	0		ns	5-9	1
t26	SD[15:0] Tri-State from S0# (MRDC#) Inactive		30	ns	5-9	
t27	A[23:0], CDSETUP# (AEN) Valid Setup to S1# (MWRC#) Active	39		ns	5-10	
t28	S1# (MWRC#) Active to CHRDY (IOCHRDY) Inactive		66	ns	5-10	
t29	A[23:0] Valid Hold from S1# (MWRC#) Active	41		ns	5-10	
t31	CDSETUP# (AEN) Valid Hold from S1# (MWRC#) Inactive	8		ns	5-10	
t32	S1# (MWRC#) Inactive to CHRDY (IOCHRDY) Invalid	7	40	ns	5-10	
t33	WRITE DATA VALID Hold from S1# (MWRC#) Inactive	32		ns	5-10	1
t34	SD[15:0] Tri-State from S1# (MWRC#) Inactive		30	ns	5-10	
t35	MADE24 (IORDC#) Inactive to VGARD# Active		42	ns	5-11	
t36	MADE24 (IORDC#) Active to VGARD# Inactive	4	24	ns	5-11	
t37	M_IO (IOWRC#) Inactive to VGAWR# Active		36	ns	5-12	
t38	M_IO (IOWRC#) Active to VGAWR# Inactive	8	23	ns	5-12	
t39	S0# (MRDC#) Active to VRAM# Active	6	55	ns	5-9	
t40	S1# (MWRC#) Active to VRAM# Active	6	55	ns	5-10	

NOTE:
1. Measured with C_L = 100 pF on SD[15:0].

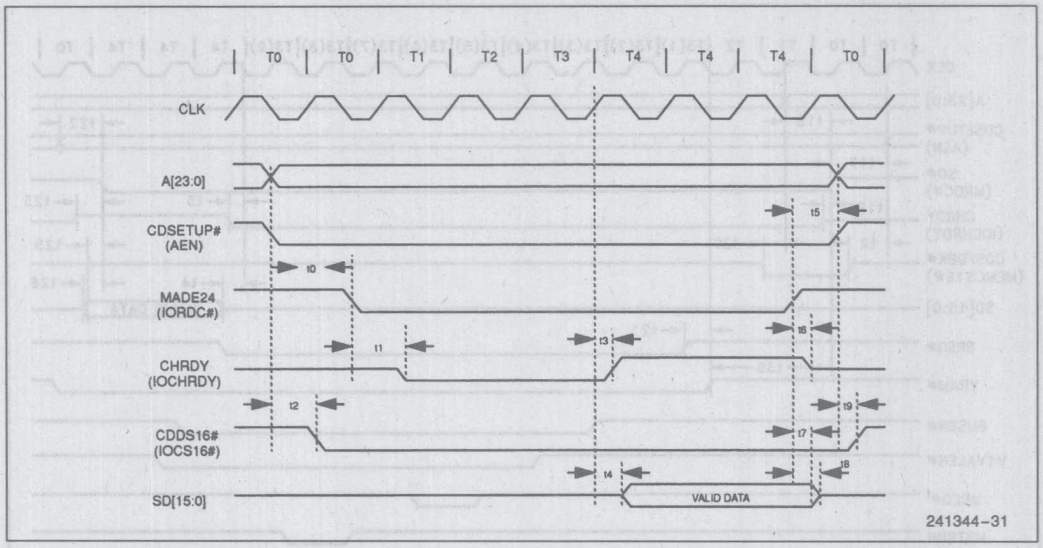


Figure 5-7. ISA I/O Read AC Timing

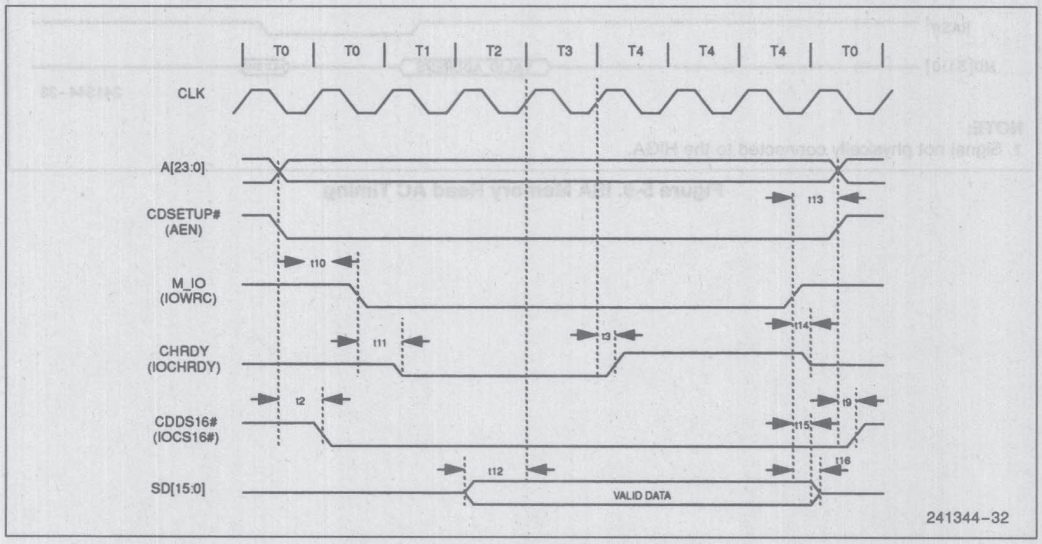
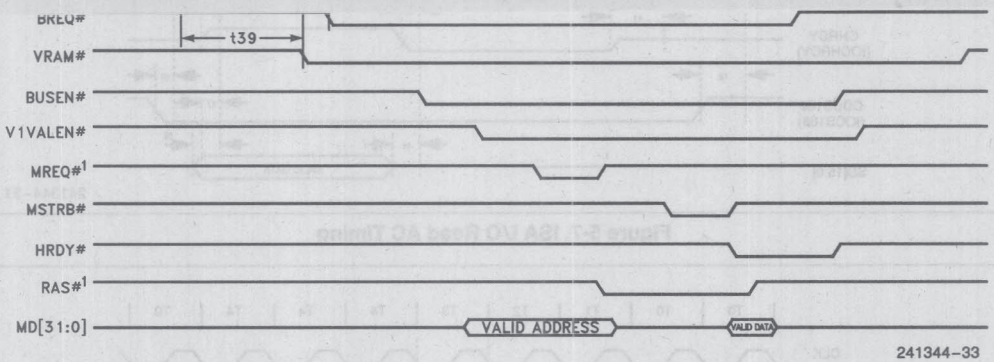
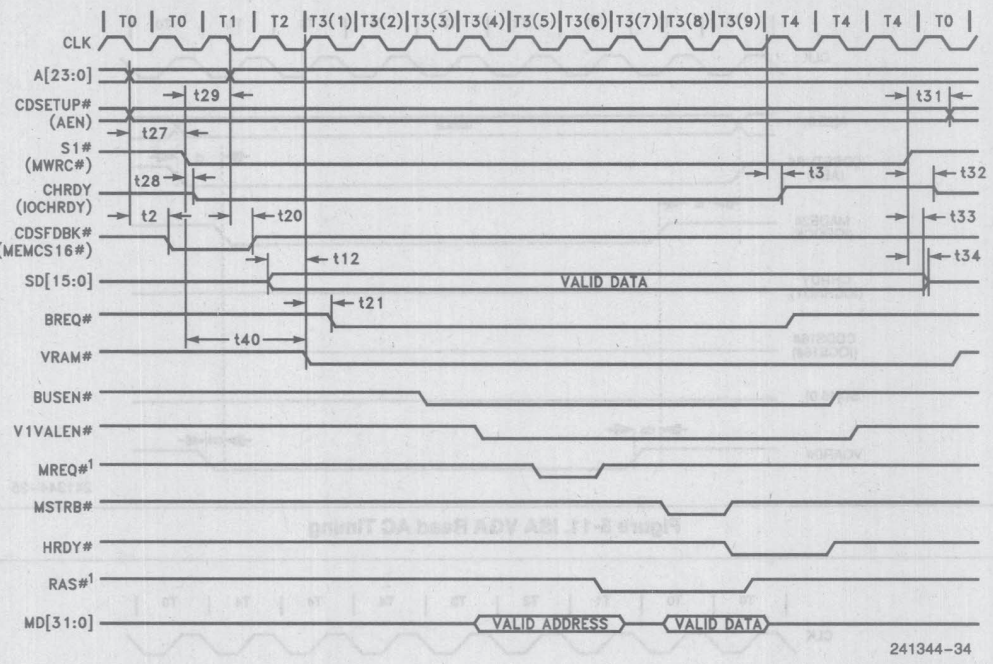


Figure 5-8. ISA I/O Write AC Timing



NOTE:
1. Signal not physically connected to the HIGA.

Figure 5-9. ISA Memory Read AC Timing



NOTE:
1. Signal not physically connected to the HIGA.

Figure 5-10. ISA Memory Write AC Timing

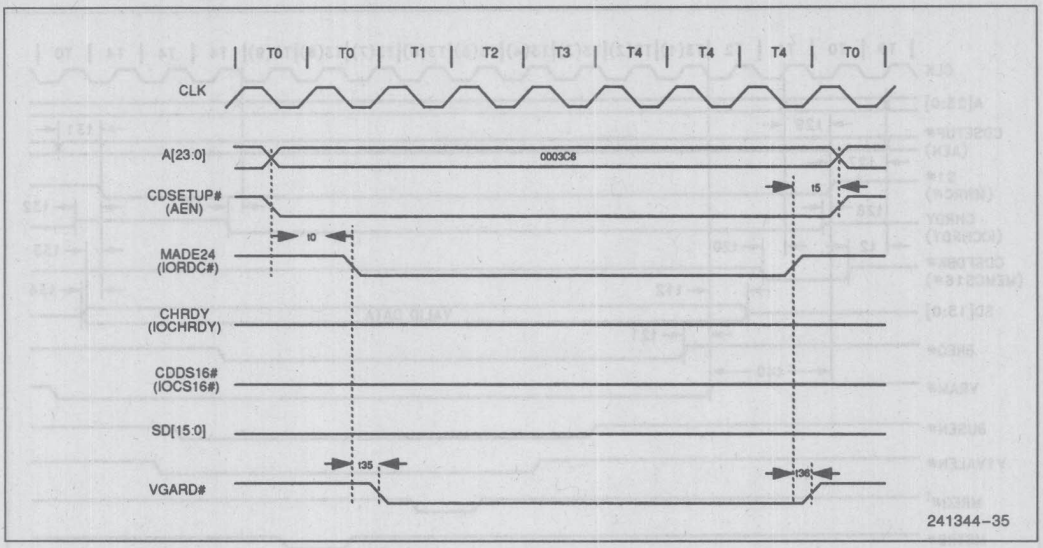


Figure 5-11. ISA VGA Read AC Timing

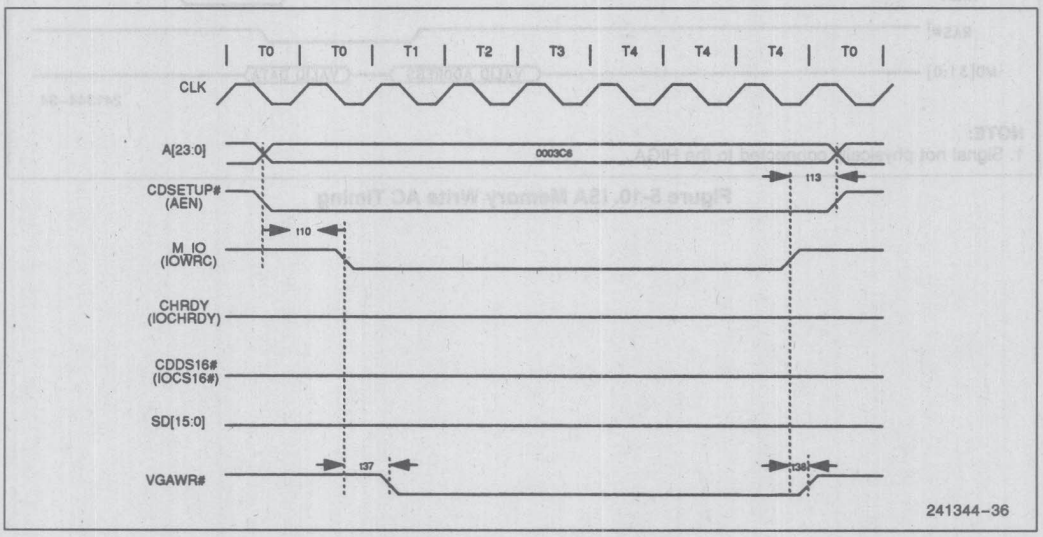


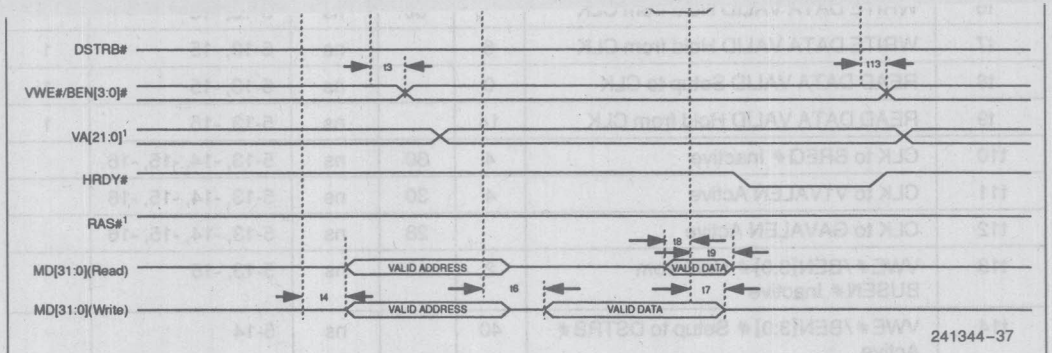
Figure 5-12. ISA VGA Write AC Timing

5.2.3 DVI BUS INTERFACE TIMING

Table 5-7. DVI Bus Intertace AC Characteristics

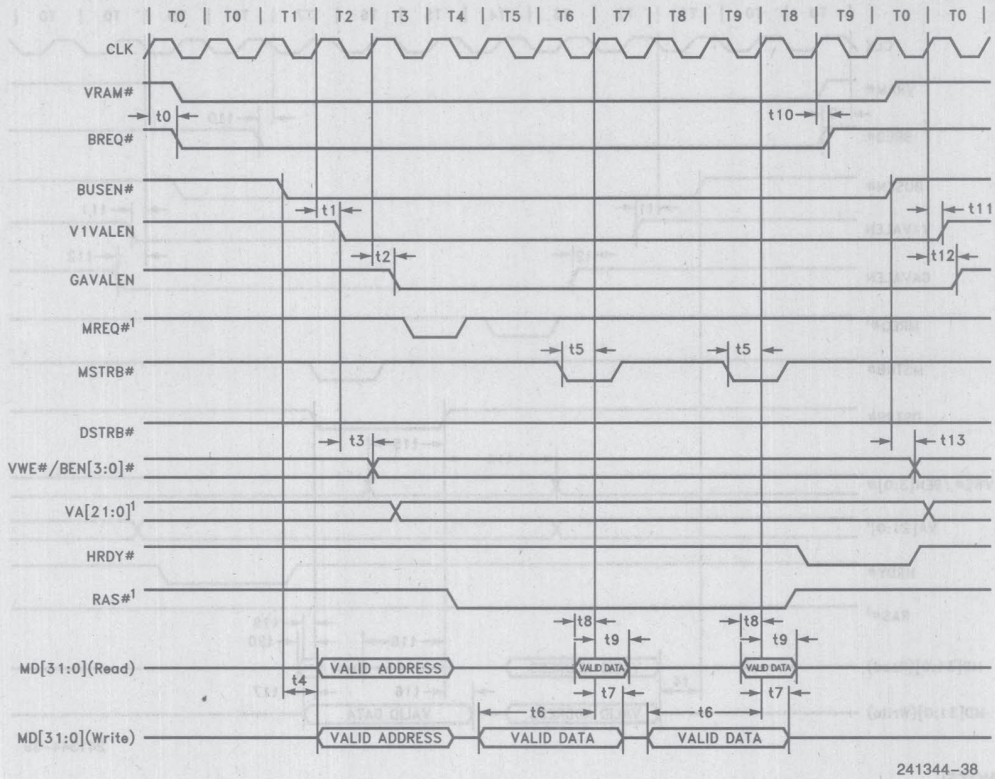
Symbol	Parameter	Min	Max	Units	Figure	Note
t0	CLK to BREQ# Active		28	ns	5-13, -14, -15, -16	
t1	CLK to V1VALEN Inactive		30	ns	5-13, -14, -15, -16	
t2	CLK to GAVALEN Inactive	4	30	ns	5-13, -14, -15, -16	
t3	V1VALEN Inactive to VWE#/ BEN[3:0]# Valid		40	ns	5-13, -15	
t4	BUSEN# Active to VALID ADDRESS	7		ns	5-13, -14, -15, -16	1
t5	MSTRB# Active Setup to CLK	10		ns	5-13, -15	
t6	WRITE DATA VALID Hold from CLK		60	ns	5-13, -15	1
t7	WRITE DATA VALID Hold from CLK	6		ns	5-13, -15	1
t8	READ DATA VALID Setup to CLK	0		ns	5-13, -15	1
t9	READ DATA VALID Hold from CLK	14		ns	5-13, -15	1
t10	CLK to BREQ# Inactive	4	30	ns	5-13, -14, -15, -16	
t11	CLK to V1VALEN Active	4	30	ns	5-13, -14, -15, -16	
t12	CLK to GAVALEN Active		28	ns	5-13, -14, -15, -16	
t13	VWE#/BEN[3:0]# Hold from BUSEN# Inactive	2	40	ns	5-13, -15	
t14	VWE#/BEN[3:0]# Setup to DSTRB# Active	40		ns	5-14	
t15	VWE#/BEN[3:0]# Hold from DSTRB# Active	40		ns	5-14	
t16	WRITE DATA VALID Setup to DSTRB# Active	40		ns	5-14	1
t17	WRITE DATA VALID Hold from DSTRB# Active	20		ns	5-14	1
t18	DSTRB# Active to READ DATA VALID		60	ns	5-14	
t19	READ DATA VALID Hold from DSTRB# Inactive	0		ns	5-14	1
t20	DSTRB# Inactive to MD[31:0] Tri-State	2	15	ns	5-14	2
t21	BUSEN# Active to VWE#/BEN[3:0]# Valid	3	55	ns	5-16	
t22	HRDY# Active Setup to CLK	0		ns	5-16	

NOTES:
1. Measured with C_L = 100 pF on MD[31:0].
2. With VWE# high.



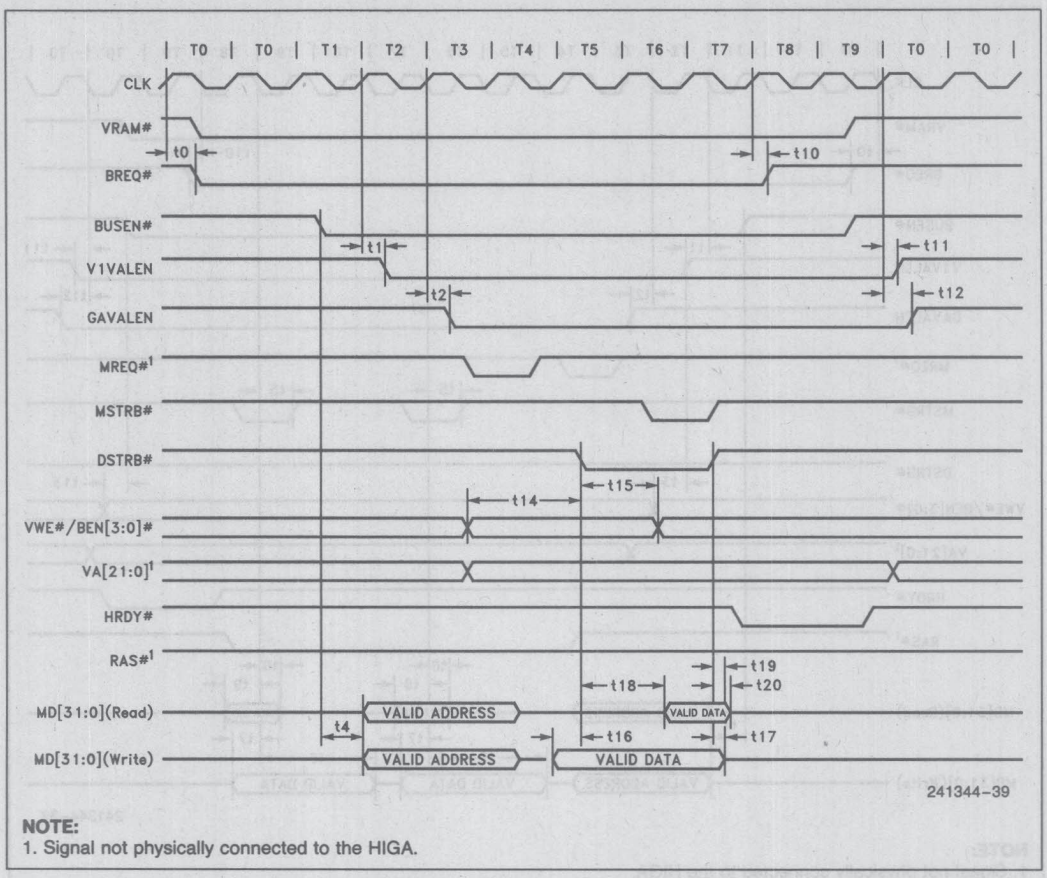
NOTE:
1. Signal not physically connected to the HIGA.

Figure 5-13. DVI Bus DVI Device VRAM Access AC Timing



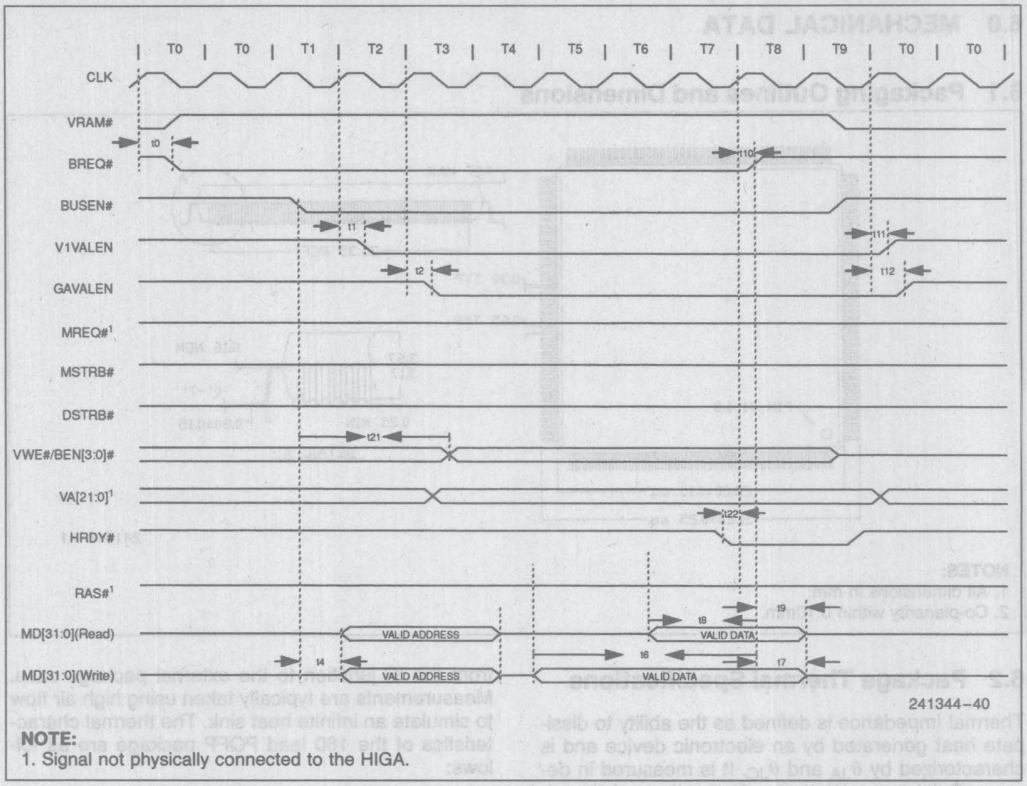
NOTE:
1. Signal not physically connected to the HIGA.

Figure 5-14. DVI Bus Next-Fast VRAM Access AC Timing



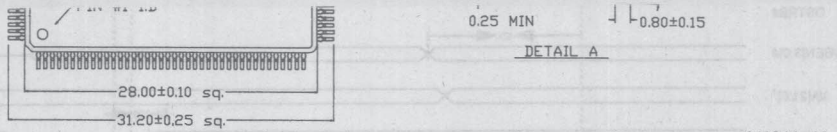
NOTE:
1. Signal not physically connected to the HIGA.

Figure 5-15. DVI Bus DVI Device Access AC Timing



NOTE:
1. Signal not physically connected to the HIGA.

Figure 5-16. DVI Bus 82750PB Register Access AC Timing



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NOTES:
1. All dimensions in mm.
2. Co-planarity within 0.10mm.

6.2 Package Thermal Specifications

Thermal Impedance is defined as the ability to dissipate heat generated by an electronic device and is characterized by θ_{JA} and θ_{JC}. It is measured in degrees Celcius per Watt. θ_{JA} is the thermal impedance from the IC chip junction to still air ambient with the package mounted in a socket or directly mounted on a PC Board. θ_{JC} is the thermal impedance from the IC junction to the external package case. Measurements are typically taken using high air flow to simulate an infinite heat sink. The thermal characteristics of the 160 lead PQFP package are as follows:

$$\theta_{JA} = 60.0°C/W$$

$$\theta_{JC} = 18.0°C/W$$