CACHE DATA SRAM

DUAL 4K x 18 SRAM, SINGLE 8K x 18 SRAM

CONFIGURABLE CACHE DATA SRAM

FEATURES

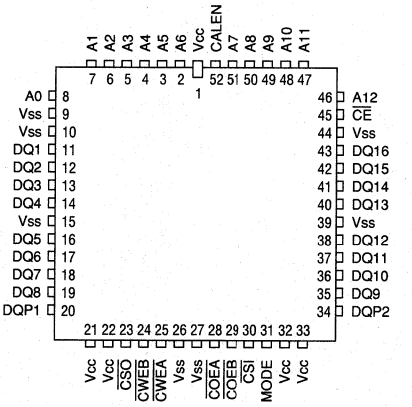
- Operates as two 4K x 18 SRAMs with common addresses and data; also configurable as a single 8K x 18 SRAM
- Built-in input address latches
- Separate upper and lower Byte Select
- Fast access times: 20ns, 25ns and 35ns allow operation with 40, 33 and 25 MHz microprocessor systems
- Fast Output Enable: 8ns
- Directly interfaces with the Intel 82385 cache controller as well as other 80386 cache memory controllers
- Parity bits provided for large cache applications such as secondary cache for the Intel 80486 microprocessors

OPTIONS

	MARKING
• Timing	
20ns access (40 MHz)	-20
25ns access (33 MHz)	-25
35ns access (25 MHz)	-35
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG

PIN ASSIGNMENT (Top View)

52-Pin PLCC (D-3)
52-Pin PQFP (D-4)



GENERAL DESCRIPTION

The MT56C0818 is one of a family of fast SRAM cache memories. It employs a high-speed, low-power design using a four-transistor memory cell. It is fabricated using double-layer polysilicon, double-layer metal CMOS technology.

The MT56C0818 is a highly integrated cache data memory building block. It easily interfaces with cache controllers for the Intel 80386 in either the DIRECT MAPPED or TWO-WAY SET ASSOCIATIVE mode. A mode control pin (MODE) determines the configuration of the memory. When this pin is held LOW, the device functions as an 8K-word by 18-bit SRAM. When the mode pin is HIGH, the device is configured as a dual 4K-word by 18-bit SRAM.

Input addresses are latched in the on-chip register on the negative edge of the CALEN signal. This register is functionally equivalent to a 74LS373.

The memory functions are controlled by the chip select ($\overline{CE}$, $\overline{CS0}$ and $\overline{CS1}$), output enable ($\overline{COEA}$ and $\overline{COEB}$) and write enable ($\overline{CWEA}$ and $\overline{CWEB}$) signals.

In either the DIRECT MAPPED (direct) or TWO-WAY SET ASSOCIATIVE (dual) operational modes, $\overline{CE}$ is a global chip enable, while $\overline{CS0}$ and $\overline{CS1}$ control lower and upper byte selection for READ and WRITE operations.

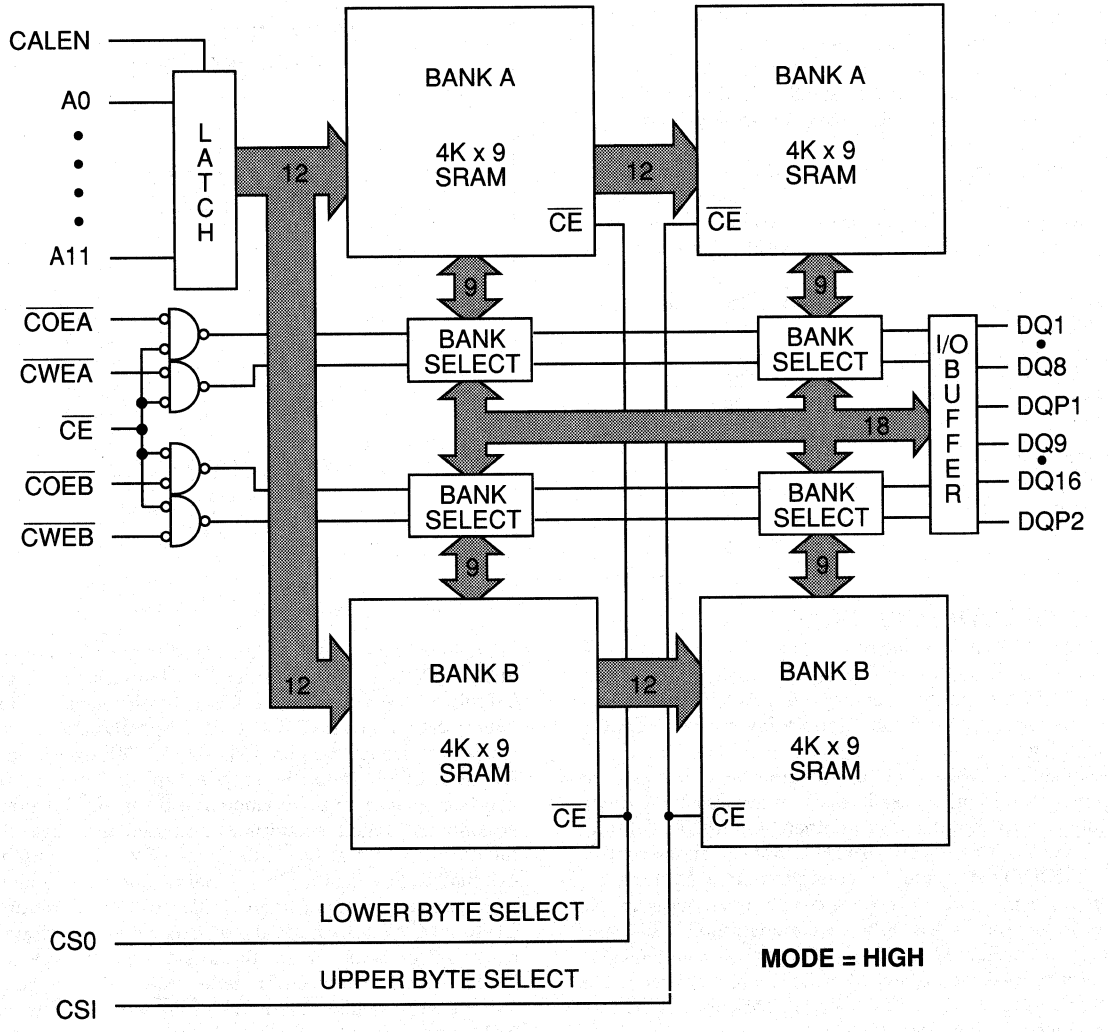
Outputs are enabled on a HIGH to LOW transition of $\overline{COEA}$ or $\overline{COEB}$. In the dual mode, bank "A" or bank "B" may be enabled. In the direct mode, $\overline{COEA}$ and $\overline{COEB}$ should be connected together externally and used as a single output enable. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.

Write enable is activated on a HIGH to LOW transition of $\overline{CWEA}$ or $\overline{CWEB}$. In the dual mode, data may be written to bank "A" or bank "B". In the direct mode, $\overline{CWEA}$ and $\overline{CWEB}$ should be connected together externally and used as a single write enable. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.

The MT56C0818 operates from a +5V power supply and all inputs and outputs are fully TTL compatible.

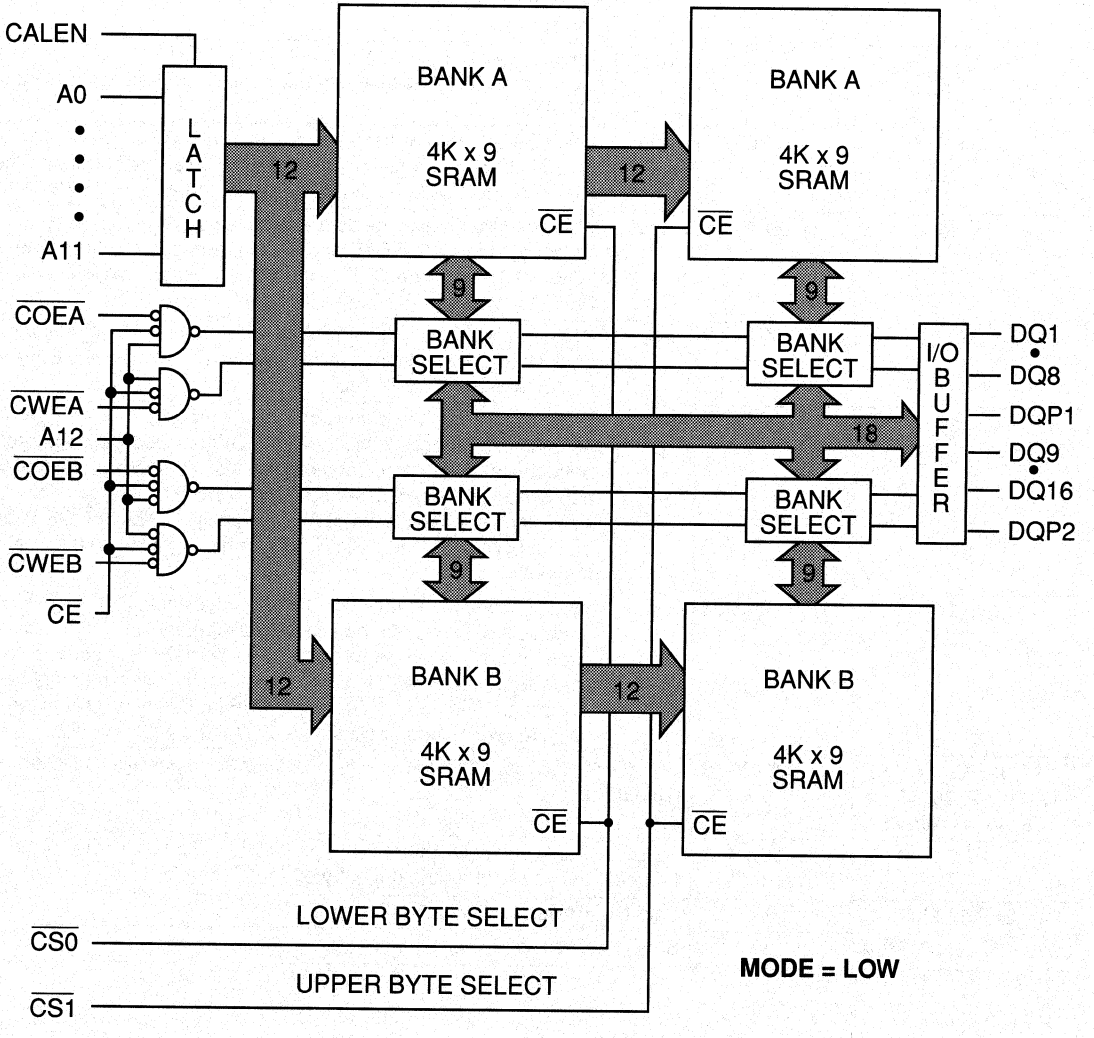
FUNCTIONAL BLOCK DIAGRAM

DUAL 4K x 18
(TWO-WAY SET ASSOCIATIVE)



FUNCTIONAL BLOCK DIAGRAM

8K x 18
(DIRECT MAP)



PIN DESCRIPTIONS

PLCC PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
8, 7, 6, 5, 4, 3, 2, 51, 50, 49, 48, 47	A0-A11	Input	Address Inputs: These inputs are clocked by CALEN and stored in a latch.
46	A12	Input	Address Input: This input is the high order address bit in the direct 8K x 18 configuration. It is not used in the dual 4K x 18 configuration.
52	CALEN	Input	Address Latch Enable: When CALEN is HIGH, the latch is transparent. The negative edge latches the current address inputs (A0-A11).
31	MODE	Input	Mode Select: This controls the device configuration. When this pin is tied HIGH, the device is in the dual 4K x 18 configuration. When the pin is tied LOW, the device is configured as an 8K x 18 SRAM.
23, 30	$\overline{CS0}$, $\overline{CS1}$	Input	Chip Selects: These signals are used to select the upper and lower bytes for both READ and WRITE operations. When $\overline{CS0}$ is LOW, DQ1-DQ8 and DQP1 are enabled. When $\overline{CS1}$ is LOW, DQ9-DQ16 and DQP2 are enabled.
45	$\overline{CE}$	Input	Chip Enable: When $\overline{CE}$ is LOW, the device is enabled. It is a global control signal that activates both bank A and bank B for READ or WRITE operations.
28, 29	$\overline{COEA}$, $\overline{COEB}$	Input	Output Enable: In the dual configuration the signal that is LOW enables bank A or B. Simultaneous LOW assertion will deselect both banks. In the direct mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is enabled. Alternately, $\overline{COEA}$ or $\overline{COEB}$ can be tied LOW externally, allowing the other signal to control the outputs.
25, 24	$\overline{CWEA}$, $\overline{CWEB}$	Input	Write Enable: In the dual configuration the signal that is LOW enables a data write to the addressed memory location. In the direct mode, these signals should be externally connected and, when asserted LOW, allow A12 to determine which memory bank is written. Alternately, $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the write function.
11, 12, 13, 14, 16 17, 18, 19, 35, 36, 37 38, 40, 41, 42, 43	DQ1-DQ16	Input/ Output	SRAM Data I/O: lower byte is DQ1-DQ8; upper byte is DQ9-DQ16.
20, 34	DQP1 DQP2	Input/ Output	Parity Data I/O: DQP1 is the parity bit for the lower byte. DQP2 is the parity bit for the upper byte.
1, 21, 22, 32, 33,	Vcc	Supply	Power Supply: +5V ±5%
9, 10, 15, 26, 27, 39, 44	Vss	Supply	Ground: GND

TRUTH TABLE

DUAL 4K x 18 (MODE PIN = HIGH)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
Outputs High-Z	X	X	X	L	L	X	X
READ DQ1-DQ8, DQP1 bank A	L	L	H	L	H	H	H
READ DQ1-DQ8, DQP1 bank B	L	L	H	H	L	H	H
READ DQ9-DQ16, DQP2 bank A	L	H	L	L	H	H	H
READ DQ9-DQ16, DQP2 bank B	L	H	L	H	L	H	H
READ DQ1-DQ16, DQP1, DQP2 bank A	L	L	L	L	H	H	H
READ DQ1-DQ16, DQP1, DQP2 bank B	L	L	L	H	L	H	H
WRITE DQ1-DQ8, DQP1 bank A	L	L	H	X	X	L	H
WRITE DQ1-DQ8, DQP1 bank B	L	L	H	X	X	H	L
WRITE DQ9-DQ16, DQP2 bank A	L	H	L	X	X	L	H
WRITE DQ9-DQ16, DQP2 bank B	L	H	L	X	X	H	L
WRITE DQ1-DQ16, DQP1, DQP2 bank A	L	L	L	X	X	L	H
WRITE DQ1-DQ16, DQP1, DQP2 bank B	L	L	L	X	X	H	L
WRITE DQ1-DQ8, DQP1 banks A & B	L	L	H	X	X	L	L
WRITE DQ9-DQ16, DQP2 banks A & B	L	H	L	X	X	L	L
WRITE DQ1-DQ16, DQP1, DQP2 banks A & B	L	L	L	X	X	L	L

NOTE: $\overline{CE}$, when taken inactive while $\overline{CWEA}$ or $\overline{CWEB}$ remain active, allows a chip-enable-controlled WRITE to be performed.

TRUTH TABLE

8K x 18 (MODE PIN = LOW)

OPERATION	$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$
Outputs High-Z, WRITE disabled	H	X	X	X	X	X	X
Outputs High-Z, WRITE disabled	X	H	H	X	X	X	X
Outputs High-Z	X	X	X	H	H	X	X
READ DQ1-DQ8, DQP1	L	L	H	L	L	H	H
READ DQ9-DQ16, DQP2	L	H	L	L	L	H	H
READ DQ1-DQ16, DQP1, DQP2	L	L	L	L	L	H	H
WRITE DQ1-DQ8, DQP1	L	L	H	X	X	L	L
WRITE DQ9-DQ16, DQP2	L	H	L	X	X	L	L
WRITE DQ1-DQ16, DQP1, DQP2	L	L	L	X	X	L	L

NOTE: 1. $\overline{CE}$, when taken inactive while $\overline{CWEA}$ and $\overline{CWEB}$ remain active, allows a chip-enable-controlled WRITE to be performed.
2. $\overline{COEA}$ and $\overline{COEB}$ must both be LOW to enable outputs. However, one signal can be tied LOW externally, allowing the other signal to control the outputs. Similarly $\overline{CWEA}$ and $\overline{CWEB}$ must both be LOW to enable a WRITE cycle. Either $\overline{CWEA}$ or $\overline{CWEB}$ can be tied LOW externally, allowing the other signal to control the WRITE function.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -1.0V to +7.0V
Storage Temperature ..... -55°C to +150°C
Power Dissipation (PLCC) 1.2W
Power Dissipation (PQFP) 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; Vcc = 5V ±5%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Power Supply Voltage		Vcc	4.75	5.25	V	
Input High Voltage		VIH	2.2	Vcc+0.3	V	1
Input Low Voltage		VIL	-0.3	0.8	V	1, 2
Input Leakage Current	VIN = GND to Vcc	ILI	-5	5	µA	
Output Leakage Current	VI/O = GND to Vcc Output(s) Disabled	ILO	-5	5	µA	
Output Low Voltage	IOL = 4.0mA	VOL		0.4	V	1
Output High Voltage	IOH = -1.0mA	VOH	2.4		V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Average Operating Current	100% Duty cycle VIN = GND to Vcc	ICC1	130	220	mA	
Power Supply Current: Average Operating Current	50% Duty cycle VIN = GND to Vcc	ICC2	70	120	mA	
Power Supply Current: CMOS Standby	$\overline{CS0}$ = $\overline{CS1}$ ≥ Vcc - 0.2V Vcc = MAX VIL ≤ Vss + 0.2V VIH ≥ Vcc - 0.2V	ISB	20	20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz Vcc = 5V	CIN	6	pF	3
Output Capacitance		CI/O	6	pF	3

PQFP THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Thermal resistance – Junction to Ambient	Still Air	ØJA	100	°C/W	
Thermal resistance – Junction to Case		ØJC	45	°C/W	
Maximum Case Temperature		TC	110	°C	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \le T_A \le +70°C$, V_{CC} = 5V ±5%)

DESCRIPTION	SYM	-20 MIN	-20 MAX	-25 MIN	-25 MAX	-35 MIN	-35 MAX	UNITS	NOTES
READ Cycle									
READ cycle time	tRC	20		25		35		ns	4, 5
Address access time (A0-A11)	tAA		20		25		35	ns	
A12 address access time	tA12A		15		17		25	ns	
Chip Enable access time	tACE		20		20		25	ns	
Chip Select access time	tACS		20		25		35	ns	
Output Enable access time	tAOE		8		10		13	ns	
Output hold from address change	tOH	3		3		3		ns	
Chip Select to output Low-Z	tLZCS	3		3		3		ns	
Output Enable to output Low-Z	tLZOE	2		2		2		ns	
Chip deselect to output High-Z	tHZCS		15		15		25	ns	6
Output disable to output High-Z	tHZOE		10		10		14	ns	6
Address Latch Enable pulse width	tCALEN	8		8		10		ns	
Address setup to latch LOW	tASL	4		4		6		ns	
Address hold from latch LOW	tAHL	5		5		5		ns	
WRITE Cycle									
WRITE cycle time	tWC	20		25		35		ns	
Address valid to end of write	tAW	15		18		25		ns	
A12 address valid to end of write	tA12W	15		18		25		ns	
Chip Select to end of write	tCW	15		18		25		ns	
Data valid to end of write	tDW	10		10		10		ns	
Data hold from end of write	tDH	0		0		0		ns	
Write Enable output in High-Z	tHZWE		12		15		15	ns	6
Write disable to output in Low-Z	tLZWE	3		3		3		ns	
WRITE pulse width	tWP	15		18		25		ns	
$\overline{CE}$ pulse width (during Chip Enable controlled write)	tCP	15		18		25		ns	
Address setup time	tAS	0		0		0		ns	
WRITE recovery time	tWR	0		0		0		ns	
Address Latch Enable pulse width	tCALEN	8		8		10		ns	
Address setup to latch LOW	tASL	4		4		6		ns	
Address hold from latch LOW	tAHL	5		5		5		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

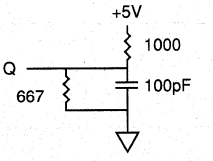


Fig. 1 OUTPUT LOAD EQUIVALENT

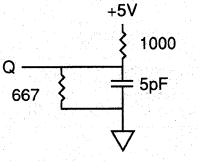
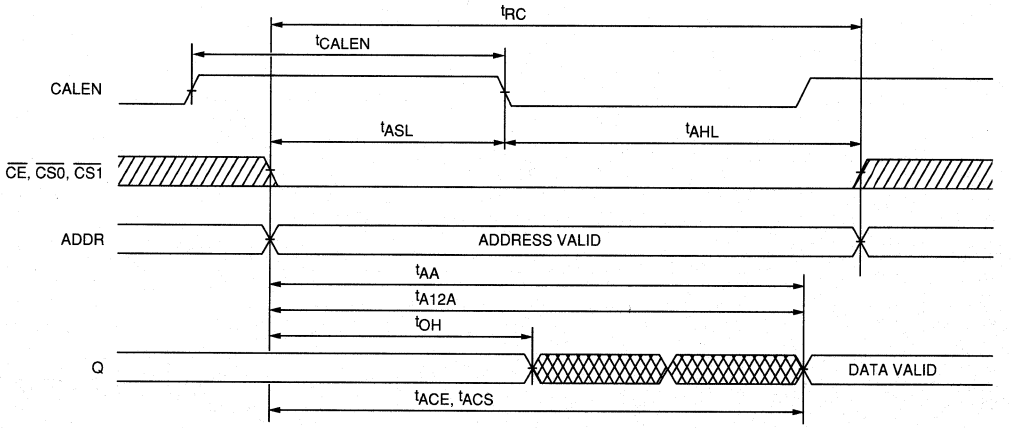


Fig. 2 OUTPUT LOAD EQUIVALENT

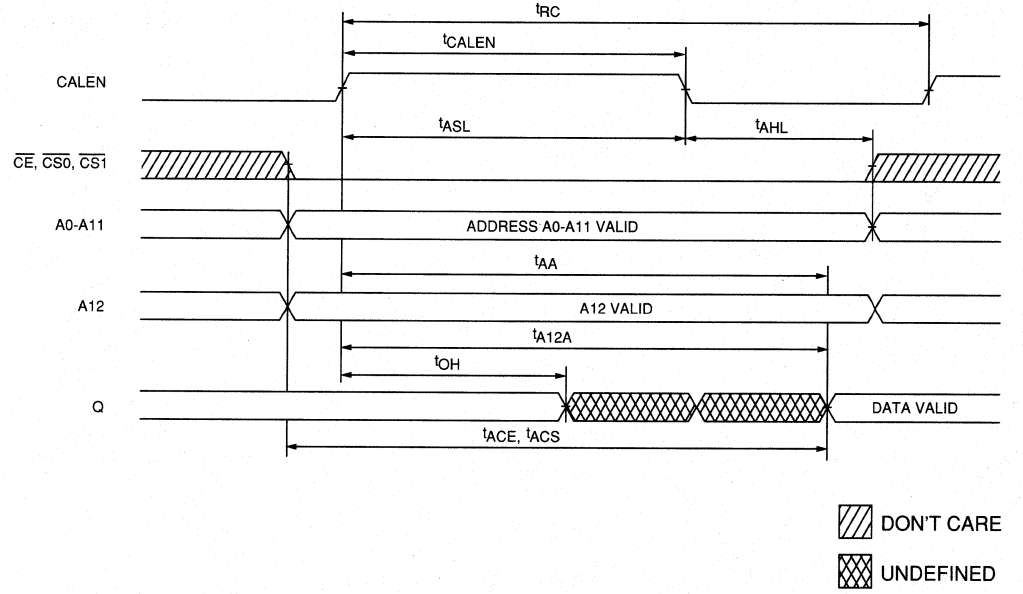
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. This parameter is sampled.
4. $\overline{CWE}$ is HIGH for a READ cycle.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. tHZCS, tHZOE, and tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.

READ CYCLE NO. 1
(Address Controlled)
$\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH}; $\overline{COEA}$ and/or $\overline{COEB}$ = V_{IL}

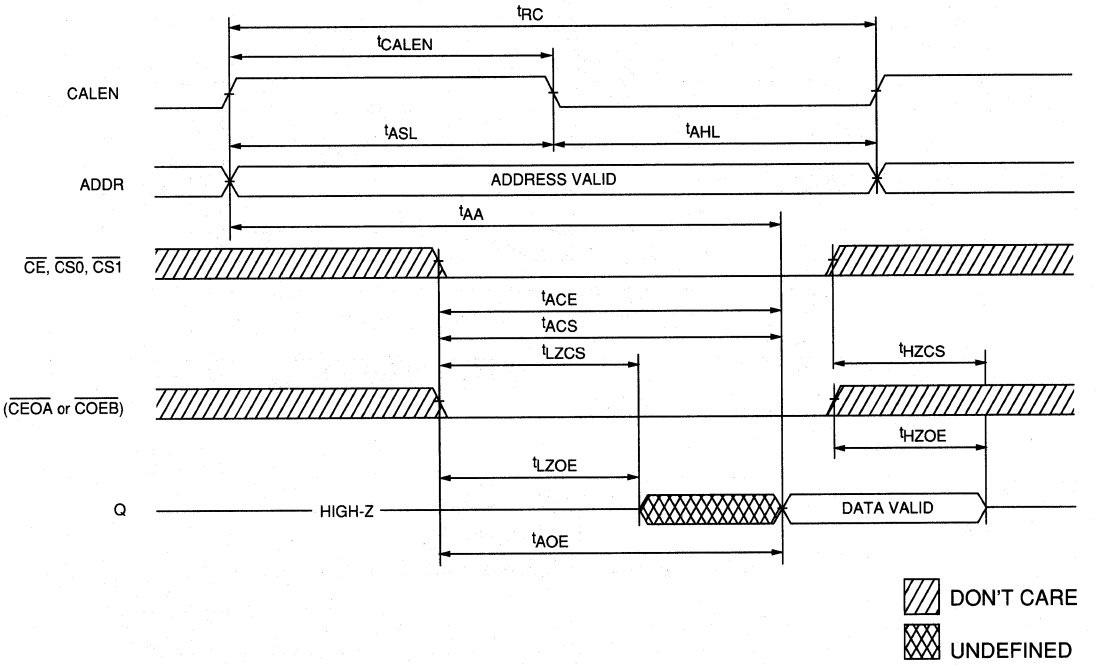


READ CYCLE NO. 2
(CALEN Controlled)
$\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH}; $\overline{COEA}$ and/or $\overline{COEB}$ = V_{IL}

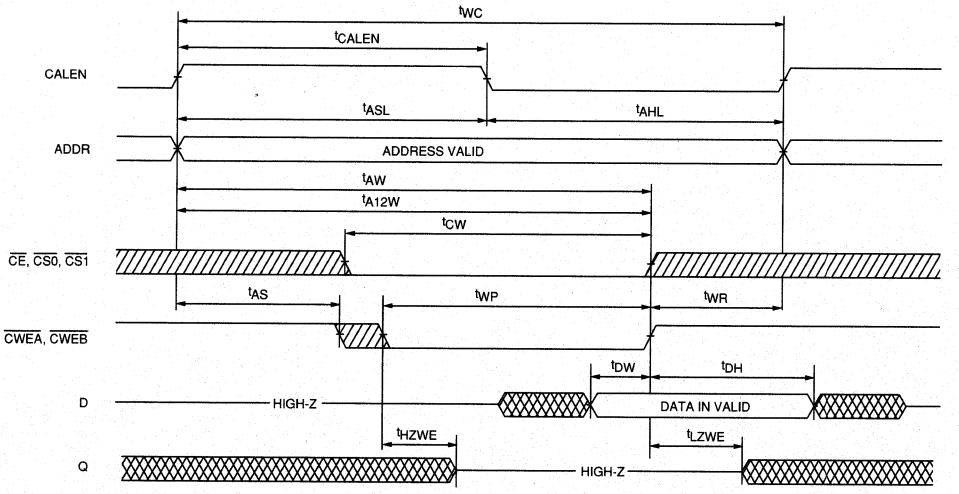


READ CYCLE NO. 3

$\overline{CWEA}$ = $\overline{CWEB}$ = V_{IH}



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Select Controlled)