National Semiconductor

October 1995

DP8392C/DP8392C-1 CTI Coaxial Transceiver Interface

General Description

The DP8392C Coaxial Transceiver Interface (CTI) is a coaxial cable line driver/receiver for Ethernet/Thin Ethernet (Cheapernet) type local area networks. The CTI is connected between the coaxial cable and the Data Terminal Equipment (DTE). In Ethernet applications the transceiver is usually mounted within a dedicated enclosure and is connected to the DTE via a transceiver cable. In Cheapernet applications, the CTI is typically located within the DTE and connects to the DTE through isolation transformers only. The CTI consists of a Receiver, Transmitter, Collision Detector, and a Jabber Timer. The Transmitter connects directly to a 50 ohm coaxial cable where it is used to drive the coax when transmitting. During transmission, a jabber timer is initiated to disable the CTI transmitter in the event of a longer than legal length data packet. Collision Detection circuitry monitors the signals on the coax to determine the presence of colliding packets and signals the DTE in the event of a collision.

The CTI is part of a three chip set that implements the complete IEEE 802.3 compatible network node electronics as shown below. The other two chips are the DP8391 Serial Network Interface (SNI) and the DP8390 Network Interface Controller (NIC).

The SNI provides the Manchester encoding and decoding functions; whereas the NIC handles the Media Access Protocol and the buffer management tasks. Isolation between the CTI and the SNI is an IEEE 802.3 requirement that can be easily satisfied on signal lines using a set of pulse transformers that come in a standard DIP. However, the power isolation for the CTI is done by DC-to-DC conversion through a power transformer.

Features

- Compatible with Ethernet II, IEEE 802.3 10Base5 and 10Base2 (Cheapernet)
- Integrates all transceiver electronics except signal & power isolation
- Innovative design minimizes external component count
- Jabber timer function integrated on chip
- Externally selectable CD Heartbeat allows operation with IEEE 802.3 compatible repeaters
- Precision circuitry implements receive mode collision detection
- Squelch circuitry at all inputs rejects noise
- Designed for rigorous reliability requirements of IEEE 802.3
- Standard Outline 16-pin DIP uses a special leadframe that significantly reduces the operating die temperature

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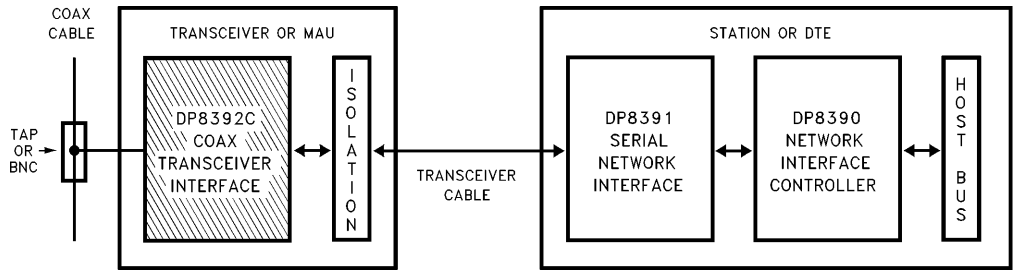
1.0 System Diagram



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IEEE 802.3 Compatible Ethernet/Cheapernet Local Area Network Chip Set

2.0 Block Diagram

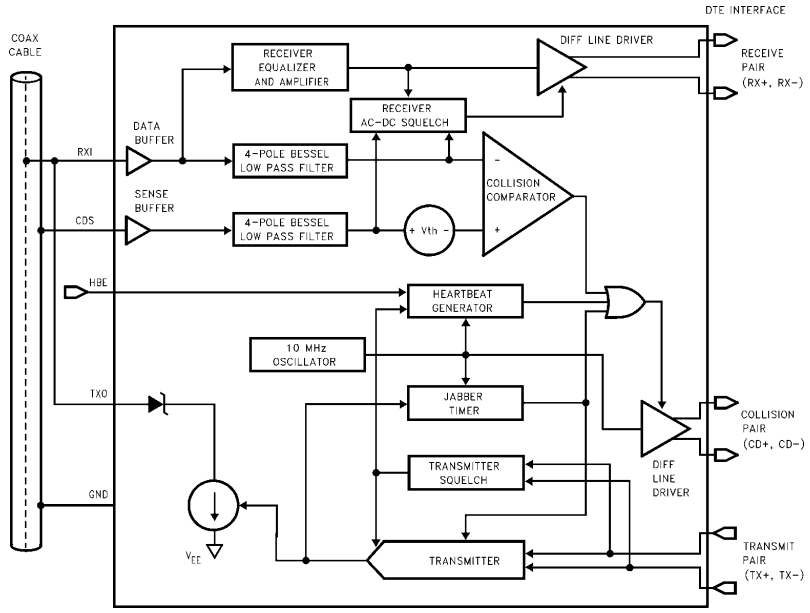

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FIGURE 1. DP8392C Block Diagram

3.0 Functional Description

The CTI consists of four main logical blocks:

a) the Receiver - receives data from the coax and sends it to the DTE

b) the Transmitter - accepts data from the DTE and transmits it onto the coax

c) the Collision Detect circuitry - indicates to the DTE any collision on the coax

d) the Jabber Timer - disables the Transmitter in case of longer than legal length packets

3.1 RECEIVER FUNCTIONS

The Receiver includes an input buffer, a cable equalizer, a 4-pole Bessel low pass filter, a squelch circuit, and a differential line driver.

The buffer provides high input impedance and low input capacitance to minimize loading and reflections on the coax.

The equalizer is a high pass filter which compensates for the low pass effect of the cable. The composite result of the maximum length cable and the equalizer is a flatband response at the signal frequencies to minimize jitter.

The 4-pole Bessel low pass filter extracts the average DC level on the coax, which is used by both the Receiver squelch and the collision detection circuits.

The Receiver squelch circuit prevents noise on the coax from falsely triggering the Receiver in the absence of the signal. At the beginning of the packet, the Receiver turns on when the DC level from the low pass filter is lower than the DC squelch threshold. However, at the end of the packet, a quick Receiver turn off is needed to reject dribble bits. This is accomplished by an AC timing circuit that reacts to high level signals of greater than typically 200 ns in duration. The Receiver then stays off only if within about 1 μs, the DC level from the low pass filter rises above the DC squelch threshold. *Figure 2* illustrates the Receiver timing.

The differential line driver provides ECL compatible signals to the DTE with typically 3 ns rise and fall times. In its idle state, its outputs go to differential zero to prevent DC standing current in the isolation transformer.

3.2 TRANSMITTER FUNCTIONS

The Transmitter has a differential input and an open collector output current driver. The differential input common mode voltage is established by the CTI and should not be altered by external circuitry. The transformer coupling of TX$\pm$ will satisfy this condition. The driver meets all IEEE 802.3/Ethernet Specifications for signal levels. Controlled rise and fall times (25 ns V $\pm$5 ns) minimize the higher harmonic components. The rise and fall times are matched to minimize jitter. The drive current levels of the DP8392C meet the tighter recommended limits of IEEE 802.3 and are set by a built-in bandgap reference and an external 1% resistor. An on chip isolation diode is provided to reduce the Transmitter's coax load capacitance. For Ethernet compatible applications, an external isolation diode (see *Figure 4*) may be added to further reduce coax load capacitance. In Cheapernet compatible applications the external diode is not required as the coax capacitive loading specifications are relaxed.

The Transmitter squelch circuit rejects signals with pulse widths less than typically 20 ns (negative going), or with levels less than $-$175 mV. The Transmitter turns off at the end of the packet if the signal stays higher than $-$175 mV for more than approximately 300 ns. *Figure 3* illustrates the Transmitter timing.

3.0 Functional Description (Continued)

3.3 COLLISION FUNCTIONS

The collision circuitry consists of two buffers, two 4-pole Bessel low pass filters (section 3.1), a comparator, a heartbeat generator, a 10 MHz oscillator, and a differential line driver.

Two identical buffers and 4-pole Bessel low pass filters extract the DC level on the center conductor (data) and the shield (sense) of the coax. These levels are monitored by the comparator. If the data level is more negative than the sense level by at least the collision threshold (Vth), the collision output is enabled.

At the end of every transmission, the heartbeat generator creates a pseudo collision for a short time to ensure that the collision circuitry is properly functioning. This burst on collision output occurs typically 1.1 μs after the transmission, and has a duration of about 1 μs. This function can be disabled externally with the HBE (Heartbeat Enable) pin to allow operation with repeaters.

The 10 MHz oscillator generates the signal for the collision and heartbeat functions. It is also used as the timebase for all the jabber functions. It does not require any external components.

The collision differential line driver transfers the 10 MHz signal to the CD± pair in the event of collision, jabber, or heartbeat conditions. This line driver also features zero differential idle state.

3.4 JABBER FUNCTIONS

The Jabber Timer monitors the Transmitter and inhibits transmission if the Transmitter is active for longer than 20 ms (fault). It also enables the collision output for the fault duration. After the fault is removed, The Jabber Timer waits for about 500 ms (unjab time) before re-enabling the Transmitter. The transmit input must stay inactive during the unjab time.

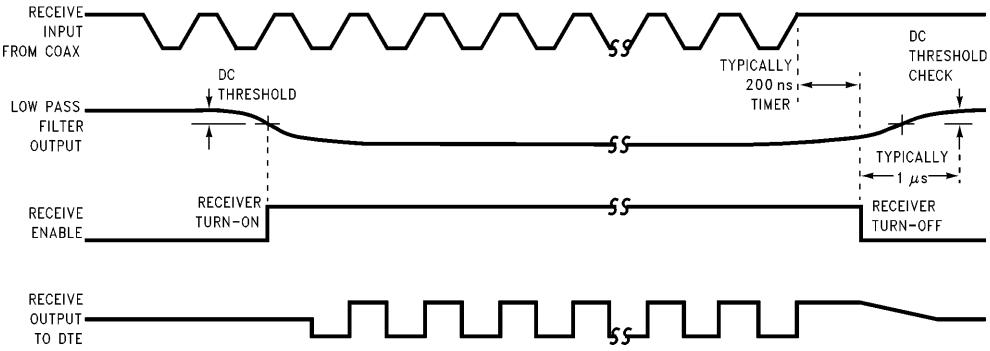


FIGURE 2. Receiver Timing

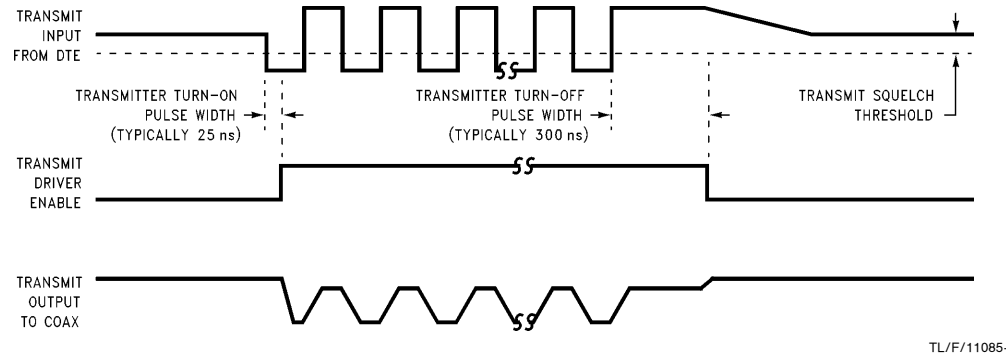
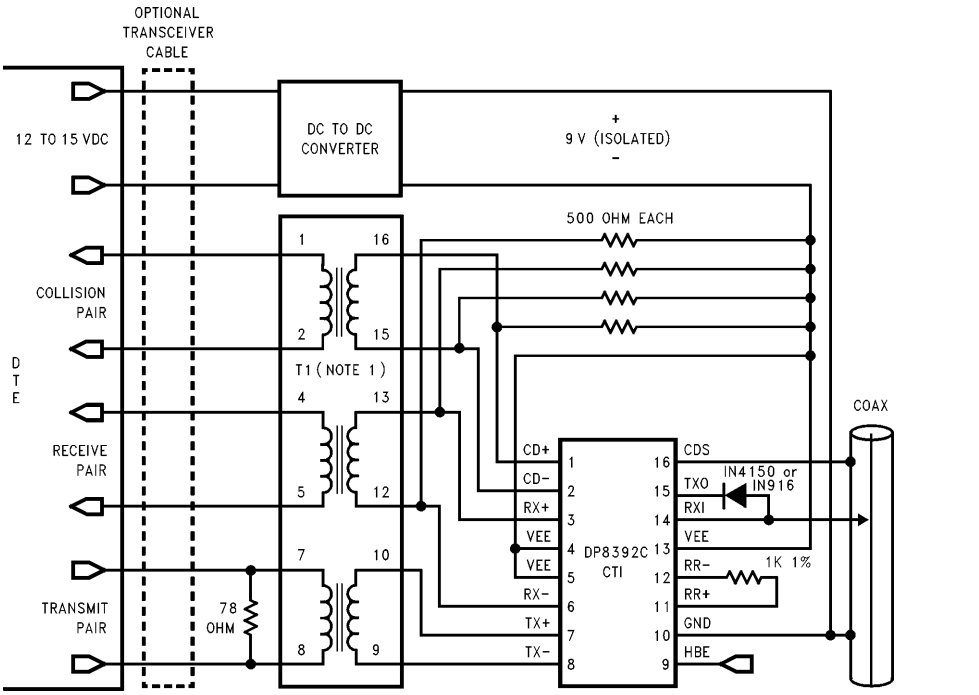


FIGURE 3. Transmitter Timing

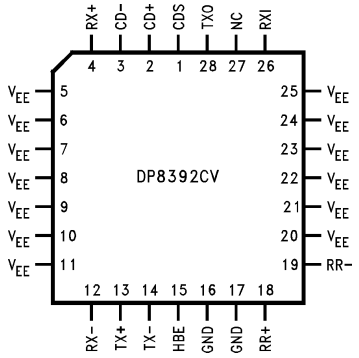
4.0 Typical Application



Note 1: T1 is a 1:1 pulse transformer, L = 100 μH
Pulse Engineering (San Diego) Part No. 64103
Valor Electronics (San Diego) Part No.
LT6003 or equivalent

FIGURE 4

5.0 Connection Diagrams



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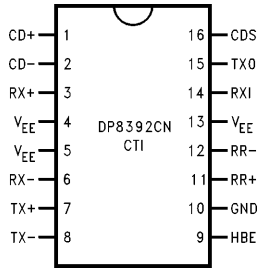
Order Number DP8392CV
See NS Package Number V28A



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Top View

Order Number DP8392CN
See NS Package Number N16E

FIGURE 5

6.0 Pin Descriptions

28-Pin PLCC	16-Pin DIP	Name	I/O	Description
2 3	1 2	CD+ * CD−	O	**Collision Output.** Balanced differential line driver outputs from the collision detect circuitry. The 10 MHz signal from the internal oscillator is transferred to these outputs in the event of collision, excessive transmission (jabber), or during CD Heartbeat condition. These outputs are open emitters; pulldown resistors to VEE are required. When operating into a 78Ω transmission line, these resistors should be 500Ω. In Cheapernet applications, where the 78Ω drop cable is not used, higher resistor values (up to 1.5k) may be used to save power.
4 12	3 6	RX+ * RX−	O	**Receive Output.** Balanced differential line driver outputs from the Receiver. These outputs also require 500Ω pulldown resistors.
13 14	7 8	TX+ * TX−	I	**Transmit Input.** Balanced differential line receiver inputs to the Transmitter. The common mode voltage for these inputs is determined internally and must not be externally established. Signals meeting Transmitter squelch requirements are waveshaped and output at TXO.
15	9	HBE	I	**Heartbeat Enable.** This input enables CD Heartbeat when grounded, disables it when connected to VEE.
18 19	11 12	RR+ RR−	I	**External Resistor.** A fixed 1k 1% resistor connected between these pins establishes internal operating currents.
26	14	RXI	I	**Receive Input.** Connects directly to the coaxial cable. Signals meeting Receiver squelch requirements are equalized for inter-symbol distortion, amplified, and outputted at RX±.
28	15	TXO	O	**Transmit Output.** Connects either directly (Cheapernet) or via an isolation diode (Ethernet) to the coaxial cable.
1	16	CDS	I	**Collision Detect Sense.** Ground sense connection for the collision detect circuit. This pin should be connected separately to the shield to avoid ground drops from altering the receive mode collision threshold.
16, 17	10	GND		**Positive Supply Pin.** A 0.1 μF ceramic decoupling capacitor must be connected across GND and VEE as close to the device as possible.
5–11 20–25	4 5 13	VEE		**Negative Supply Pins.** In order to make full use of the 3.5W power dissipation capability of this package, these pins should be connected to a large metal frame area on the PC board. Doing this will reduce the operating die temperature of the device thereby increasing the long term reliability.

*IEEE names for CD± = CI±, RX± = DI±, TX± = DO±

6.1 P.C. BOARD LAYOUT

The DP8392C package is uniquely designed to ensure that the device meets the 1 million hour Mean Time Between Failure (MTBF) requirement of the IEEE 802.3 standard. In order to fully utilize this heat dissipation design, the three V_{EE} pins are to be connected to a copper plane which should be included in the printed circuit board layout.

There are two basic considerations in designing a PCB for the DP8392C and C-1 CTI. The first is ensuring that the layout does not degrade the electrical characteristics of the DP8392, and enables the end product to meet the IEEE 802.3 specifications. The second consideration is meeting the thermal requirements to the DP8392.

Since the DP8392 is highly integrated the layout is actually quite simple, and there are just a few guidelines:

1. Ensure that the parasitic capacitance added to the RXI and TXO pins is minimized. To do this keep these signal traces short, and remove any power planes under these signals, and under any components that connect to these signals. *Figure 6* shows the component placement for the DIP package. The PLCC component placement would be similar, as shown in *Figure 7*.
2. The power supply layout to the CTI should be relatively clean. Usually the CTI's power is supplied directly by a DC-DC converter. The power should be routed either through separate isolated planes, or via thick PCB traces.

For the second consideration, the packaged DP8392 must have a thermal resistance of 40°C–45°C/W to meet the full 0°C–70°C temperature range. The CTI dissipates more power when transmitting than while it is idle. In order to do this the thermal resistance of the device must be 40°C–45°C/W. To meet this requirement during transmission, it is recommended that a small printed circuit board plane be connected to all V_{EE} pins on the solder side of the PCB.

The size of the trace plane depends on the package used and the duty cycle of transmissions. For the DIP package the plane should be connected to pins 4–5, 13, and the size should be approximately 0.2 square inches for applications where the duty cycle of the transmitter is very low (<10%). This would be typical of adapter or motherboard applications. In applications where the transmitter duty cycle may be large (repeaters and external transceivers) the total area should be increased to 0.4 in^2. *Figure 6* illustrates a recommended component side layout for these planes.

6.0 Pin Descriptions (Continued)

For the PLCC packaged DP8392, it is recommended that a small printed circuit board V_{EE} plane be connected to pins 5–11, and a second one be connected to pins 20–25. To reduce the thermal resistance to the required value, the area of the plane on EACH set of pins should be ≥ 0.20 in^2 for applications with low transmitter duty cycle, and ≥ 0.4 in^2 for high transmit duty cycle applications. *Figure 7* illustrates a recommended component side layout for these planes.

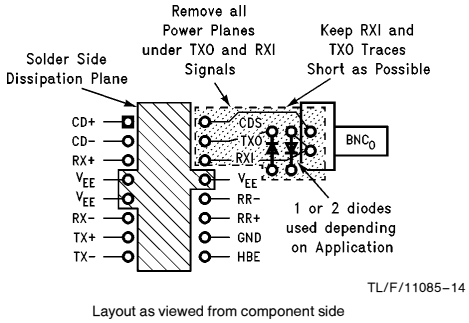

FIGURE 6. Typical Layout Considerations for DP8392CN (Not to Scale)

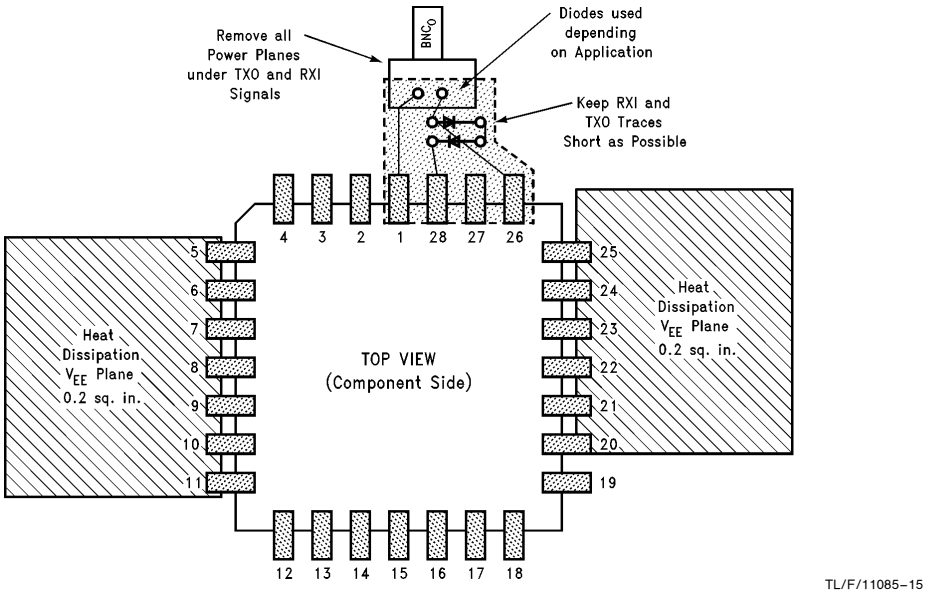

FIGURE 7. Recommended Layout and Dissipation Planes for DP8392CV (Not to Scale)

7.0 Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{EE})	−12V
Package Power Rating at 25°C	3.5 Watts*
(PC Board Mounted)	See Section 5
Derate linearly at the rate of 28.6 mW/°C	
Input Voltage	0 to −12V
Storage Temperature	−65° to 150°C
Lead Temp. (Soldering, 10 seconds)	260°C

*For actual power dissipation of the device please refer to section 7.0.

Recommended Operating Conditions

Supply Voltage (V_{EE})	−9v ±5%
Ambient Temperature	0° to 70°C

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

8.0 DP8392C Electrical Characteristics $V_{EE} = -9V \pm 5\%$, $T_A = 0°$ to 70°C (Notes 2 & 3)

All parameters with respect to CD± and RX± are measured after the pulse transformer except V_{OC}.

Symbol	Parameter	Min	Typ	Max	Units
I_{EE1}	Supply current out of V_{EE} pin—non transmitting		−85	−130	mA
I_{EE2}	Supply current out of V_{EE} pin—transmitting		−125	−180	mA
I_{RXI}	Receive input bias current (RXI)	−2		+25	μA
I_{TDC}	Transmit output dc current level (TXO)	37	41	45	mA
I_{TAC}	Transmit output ac current level (TXO)	±28		I_{TDC}	mA
V_{CD}	Collision threshold (Receive mode)	−1.45	−1.53	−1.58	V
V_{OD}	Differential output voltage (RX±, CD±)	±550		±1200	mV
V_{OC}	Common mode output voltage (RX±, CD±)	−1.5	−2.0	−2.5	V
V_{OB}	Diff. output voltage imbalance (RX±, CD±)			±40	mV
V_{TS}	Transmitter squelch threshold (TX±)	−175	−225	−300	mV
C_X	Input capacitance (RXI)		1.2		pF
R_{RXI}	Shunt resistance—non transmitting (RXI)	100			KΩ
R_{TXO}	Shunt resistance—transmitting (TXO)		10		KΩ

9.0 DP8392C-1 Electrical Characteristics $V_{EE} = -9V \pm 5\%$, $T_A = 0°$ to 70°C (Notes 2 & 3)

All parameters with respect to CD± and RX± are measured after the pulse transformer except V_{OC}.

Symbol	Parameter	Min	Typ	Max	Units
I_{EE1}	Supply current out of V_{EE} pin—non transmitting		−85	−130	mA
I_{EE2}	Supply current out of V_{EE} pin—transmitting		−125	−180	mA
I_{RXI}	Receive input bias current (RXI)	−2		+25	μA
I_{TDC}	Transmit output dc current level (TXO)	37	41	45	mA
I_{TAC}	Transmit output ac current level (TXO)	±28		I_{TDC}	mA
V_{CD}	Collision threshold (Receive mode)	−1.45	−1.53	−1.58	V
V_{OD}	Differential output voltage (RX±, CD±)	±550		±1200	mV
V_{OC}	Common mode output voltage (RX±, CD±)	−1.5	−2.0	−2.5	V
V_{OB}	Diff. output voltage imbalance (RX±, CD±)			±40	mV
V_{TS}	Transmitter squelch threshold (TX±)	−175	−225	−275	mV
C_X	Input capacitance (RXI)		1.2		pF
R_{RXI}	Shunt resistance—non transmitting (RXI)	100			KΩ
R_{TXO}	Shunt resistance—transmitting (TXO)	7.5K	10		KΩ

Note 1: Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.

Note 2: All currents into device pins are positive, all currents out of device pins are negative. All voltages referenced to ground unless otherwise specified.

Note 3: All typicals are given for $V_{EE} = -9V$ and $T_A = 25°C$.

10.0 DP8392C Switching Characteristics $V_{EE} = -9V \pm 5\%$, $T_A = 0°$ to 70°C (Note 3)

Symbol	Parameter	Fig	Min	Typ	Max	Units
t_{RON}	Receiver startup delay (RXI to RX±)	8 & 14		4		bits
t_{Rd}	Receiver propagation delay (RXI to RX±)	8 & 14		15	50	ns
t_{Rr}	Differential outputs rise time (RX±, CD±)	8 & 14		4		ns
t_{Rf}	Differential outputs fall time (RX±, CD±)	8 & 14		4		ns
t_{RJ}	Receiver & cable total jitter	13		±2		ns
t_{TST}	Transmitter startup delay (TX± to TXO)	9 & 14		1		bits
t_{Td}	Transmitter propagation delay (TX± to TXO)	9 & 14		25	50	ns
t_{Tr}	Transmitter rise time —10% to 90% (TXO)	9 & 14		25		ns
t_{Tf}	Transmitter fall time —90% to 10% (TXO)	9 & 14		25		ns
t_{TM}	t_{Tr} and t_{Tf} mismatch			0.5		ns
t_{TS}	Transmitter skew (TXO)			±0.5		ns
t_{TON}	Transmit turn-on pulse width at V_{TS} (TX±)	9 & 14		20		ns
t_{TOFF}	Transmit turn-off pulse width at V_{TS} (TX±)	9 & 14		250		ns
t_{CON}	Collision turn-on delay	10 & 14		7		bits
t_{COFF}	Collision turn-off delay	10 & 14			20	bits
f_{CD}	Collision frequency (CD±)	10 & 14	8.0		12.5	MHz
t_{CP}	Collision pulse width (CD±)	10 & 14	35		70	ns
t_{HON}	CD Heartbeat delay (TX± to CD±)	11 & 14	0.6		1.6	μs
t_{HW}	CD Heartbeat duration (CD±)	11 & 14	0.5	1.0	1.5	μs
t_{JA}	Jabber activation delay (TX± to TXO and CD±)	12 & 14	20	29	60	ms
t_{JR}	Jabber reset unjab time (TX± to TXO and CD±)	12 & 14	250	500	750	ms

DP8392C-1 Switching Characteristics $V_{EE} = -9V \pm 5\%$, $T_A = 0°$ to 70°C (Note 3)

Symbol	Parameter	Fig	Min	Typ	Max	Units
t_{RON}	Receiver startup delay (RXI to RX±)	8 & 14		4	5	bits
t_{Rd}	Receiver propagation delay (RXI to RX±)	8 & 14		15	50	ns
t_{Rr}	Differential outputs rise time (RX±, CD±)	8 & 14		4	7	ns
t_{Rf}	Differential outputs fall time (RX±, CD±)	8 & 14		4	7	ns
t_{RJ}	Receiver & cable total jitter	13		±2		ns
t_{TST}	Transmitter startup delay (TX± to TXO)	9 & 14		1	2	bits
t_{Td}	Transmitter propagation delay (TX± to TXO)	9 & 14	5	25	50	ns
t_{Tr}	Transmitter rise time —10% to 90% (TXO)	9 & 14	20	25	30	ns
t_{Tf}	Transmitter fall time —90% to 10% (TXO)	9 & 14	20	25	30	ns
t_{TM}	t_{Tr} and t_{Tf} mismatch			0.5		ns
t_{TS}	Transmitter skew (TXO)			±0.5		ns
t_{TON}	Transmit turn-on pulse width at V_{TS} (TX±)	9 & 14	5	20	40	ns
t_{TOFF}	Transmit turn-off pulse width at V_{TS} (TX±)	9 & 14	110		270	ns
t_{CON}	Collision turn-on delay	10 & 14		7	13	bits
t_{COFF}	Collision turn-off delay	10 & 14			20	bits
f_{CD}	Collision frequency (CD±)	10 & 14	8.5		12.5	MHz
t_{CP}	Collision pulse width (CD±)	10 & 14	35		70	ns
t_{HON}	CD Heartbeat delay (TX± to CD±)	11 & 14	0.6		1.6	μs
t_{HW}	CD Heartbeat duration (CD±)	11 & 14	0.5	1.0	1.5	μs
t_{JA}	Jabber activation delay (TX± to TXO and CD±)	12 & 14	20	29	60	ms
t_{JR}	Jabber reset unjab time (TX± to TXO and CD±)	12 & 14	250	500	750	ms

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Note 2: All currents into device pins are positive, all currents out of device pins are negative. All voltages referenced to ground unless otherwise specified.

Note 3: All typicals are given for $V_{EE} = -9V$ and $T_A = 25°C$.

11.0 Timing and Load Diagrams

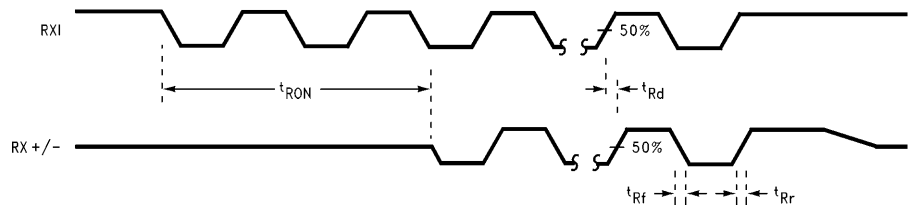

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FIGURE 8. Receiver Timing

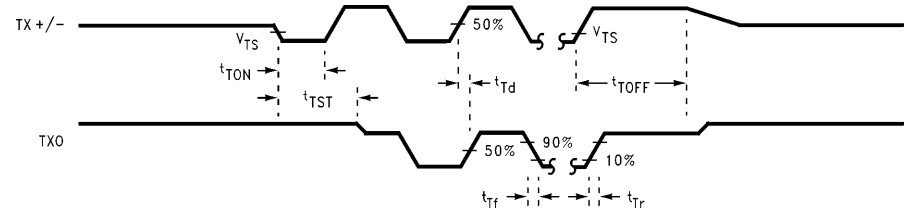

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FIGURE 9. Transmitter Timing

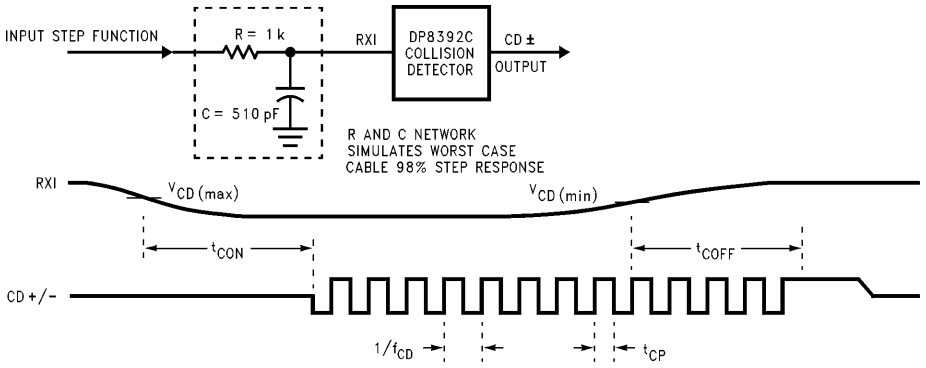

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FIGURE 10. Collision Timing

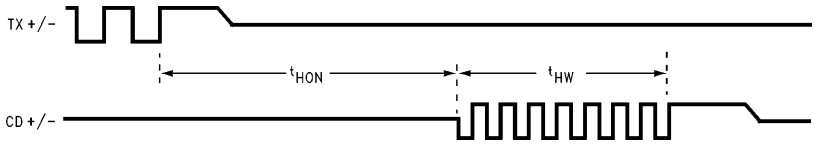

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FIGURE 11. Heartbeat Timing

11.0 Timing and Load Diagrams (Continued)

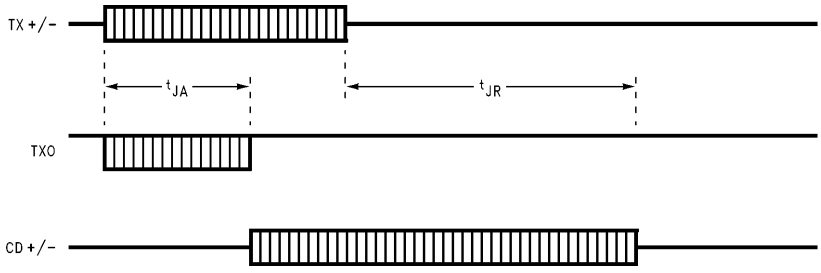

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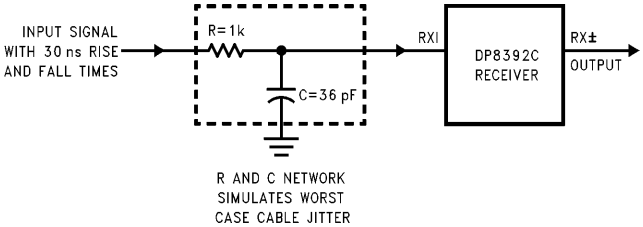
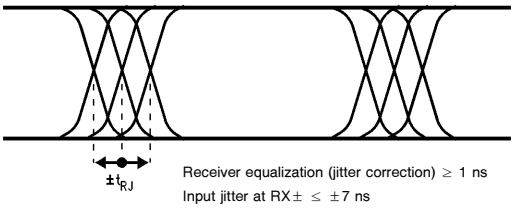
FIGURE 12. Jabber Timing





Receiver equalization (jitter correction) ≥ 1 ns
Input jitter at RX± ≤ ±7 ns
Output jitter at RX± ≤ ±6 ns

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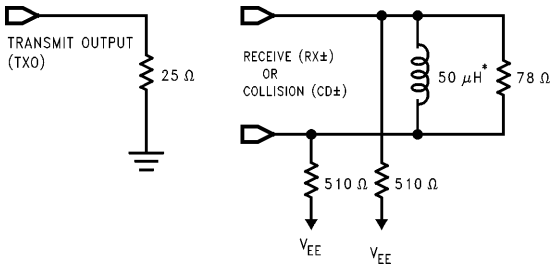
FIGURE 13. Receive Jitter Timing

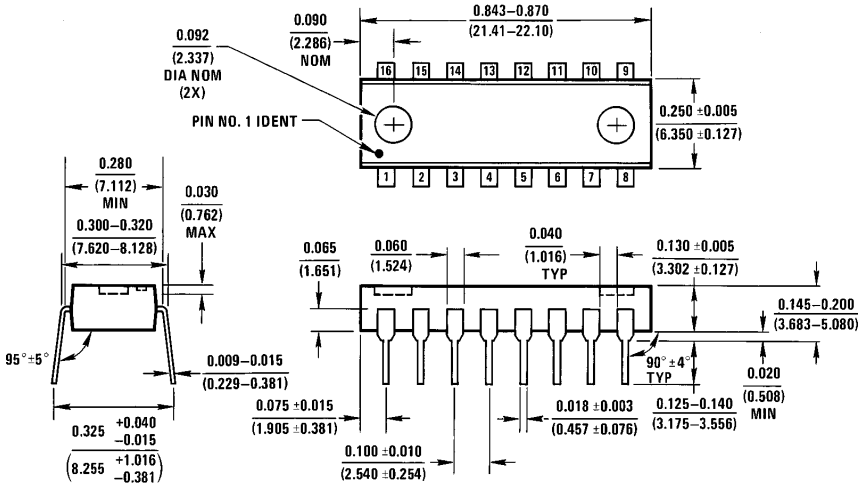


TL/F/11085–13

*The 50 μH inductance is for testing purposes. Pulse transformers with higher inductances are recommended (see *Figure 4*)

FIGURE 14. Test Loads

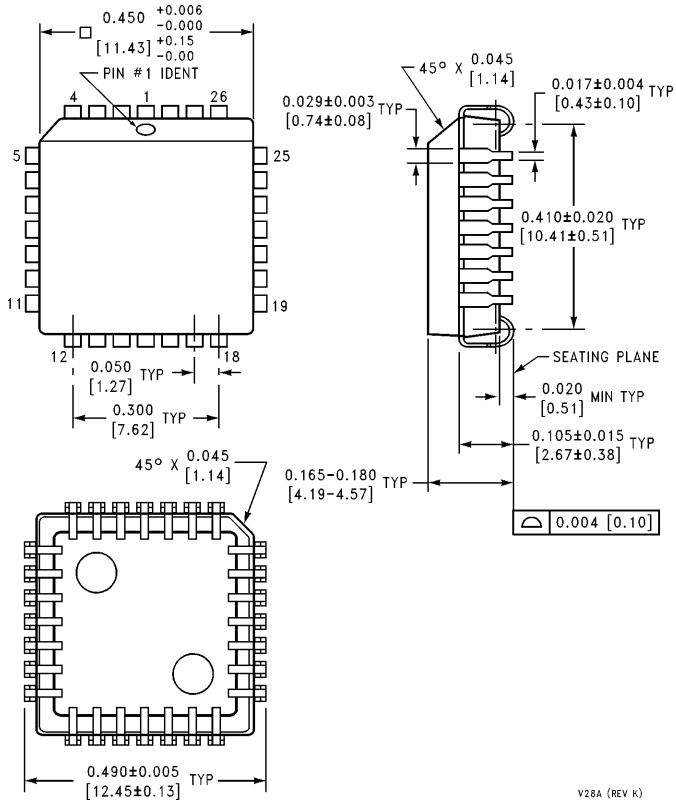
12.0 Physical Dimensions inches (millimeters)



Molded Dual-In-Line Package (N)
Order Number DP8392CN or DP8392CN-1
NS Package Number N16E

12.0 Physical Dimensions inches (millimeters) (Continued)

Lit. # 103054



28-Lead Plastic Chip Carrier
Order Number DP8392CV or DP8392CV-1
NS Package Number V28A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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