MCA 1200

Micro Channel* Bus Controller and Local Arbiter

September 1988

Distinctive Features

- Includes logic, high current drivers and buffers for master to Micro Channel* interface in slim 24 pin CMOS DIP
- Performs Micro Channel* bus control and local arbitration
- Microprocessor independent
- Includes burst or single cycle data transfer bus requester
- Includes fairness arbitration option
- Drives Micro Channel* signals to specifications: CMD*, ARB0-1, PREEMPT* and BURST*
- Input hysteresis filters bus noise

Programmable Version Available

If the MCA 1200 does not match the requirements of the design, a programmable version is available (the PLX 448) which allows the user to customize all inputs, outputs and logic. Programming is performed using industry standard tools such as ABEL™ or CUPL™ software and commonly available PLD programming hardware. Contact PLX for a data sheet on the PLX 448 and other information.

Applications

- Micro Channel Architecture* bus masters

General Description

The MCA 1200 is a high speed bus control master, bus requester and local arbiter. The device functions as a Micro Channel* adapter bus master.

The MCA 1200 is a CMOS device housed in a 24 pin 300 mil wide DIP and incorporates most of the logic, drivers and buffers required to control the bus. The controller, requester and local arbiter protocols are asynchronous and meet the IBM Micro Channel Architecture timing and electrical specifications.

The MCA 1200 performs bus request and local arbitration protocols. The device allows either single cycle or burst data transfer requests. The arbitration protocol features an optional fairness algorithm which prevents two consecutive bus accesses by the master. The bus control protocol controls the bus and aids the successful transfer of data.

The MCA 1200 is compatible with any processor, including the 80X86 and the 680XX series.

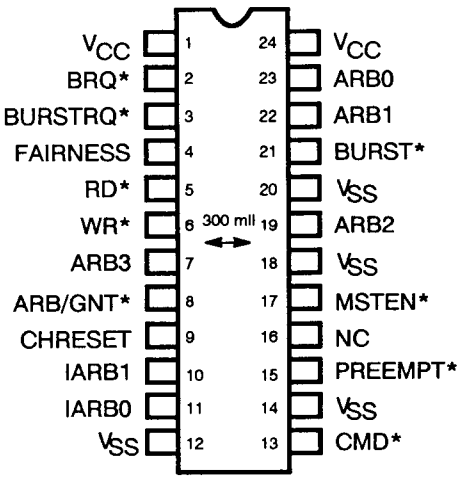

Figure 1. Pinout of MCA 1200

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Patent Pending
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PLX Technology, Inc., 625 Clyde Avenue, Mountain View, CA 94043 (415) 960-0448 FAX (415) 960-0479

Pin Description

Pin	Signal	Description	I/O	Function
1	V_{CC}	Power	I	5V supply
2	BRQ*	Bus Request	I	Active Low; Local bus request input to PREEMPT*
3	BURSTRQ*	Burst Request	I	Active Low; Local burst mode request input to BURST*
4	FAIRNESS	Fairness Enable	I	Active High; Fairness algorithm enable input to arbiter
5	RD*	Read	I	Active Low; Read command from 80X86 (UDS* from 680XX)
6	WR*	Write	I	Active Low; Write command from 80X86 (LDS* from 680XX)
7	ARB3	Arbitration level 3	I	Micro Channel Input; Active high; Arbitration priority level input.
8	ARB/GNT*	Arbitration/Grant	I	Micro Channel Input; Indicates arbitration in process or bus is granted
9	CHRESET	Channel Reset	I	Micro Channel Input; Active high; System reset
10	IARB1	Input arbitration level 1	I	Active high; selects arbitration level
11	IARB0	Input arbitration level 0	I	Active high; selects arbitration level
12	V_{SS}	Ground	I	Ground
13	CMD*	Command	O	Micro Channel Output; Active low; Indicates valid data cycle
14	V_{SS}	Ground	I	Ground
15	PREEMPT*	Preempt	I/O	Micro Channel Input/Output; Active low; Request control of bus to arbiter
16	NC		–	No Connect
17	MSTEN*	Master Enable	O	Active Low; Master enable output, master controls bus and enables buffers
18	V_{SS}	Ground	I	Ground
19	ARB2	Arbitration level 2	I	Micro Channel Input; Active high; Arbitration priority level input.
20	V_{SS}	Ground	I	Ground
21	BURST*	Burst	O	Micro Channel Output; Active low; Indicates burst or block data transfer
22	ARB1	Arbitration level 1	I/O	Micro Channel Input/Output; Active high; Arbitration priority level
23	ARB0	Arbitration level 0	I/O	Micro Channel Input/Output; Active high; Arbitration priority level
24	V_{CC}	Power	I	5V supply

Detailed Description

The following section describes the MCA 1200 initiating, executing and terminating a data transfer cycle. This explanation assumes that the device is implemented in a bus master adapter with an 80X86 processor as shown in figure 2. However, the MCA 1200 can be used with a wide variety of processors. For example, if a 680XX processor is used, replace RD* and WR* with UDS* and LDS*.

Figure 3 shows the timing relationships for a data transfer cycle.

Bus Request

The local processor initiates a bus request by asserting BRQ*. If the local processor requires a burst or block transfer data cycle, then it will also assert BURSTRQ*. While either RD* or WR* is active, the assertion of BRQ* enables PREEMPT* to the system arbiter. After asserting PREEMPT*, the local master will participate in the next arbitration cycle when ARB/GNT* is disabled.

Arbitration Priority Levels

The MCA 1200 can be configured for arbitration priority levels 12-15 (1100-1111) permanently or dynamically. By tying IARB0,1 inputs high or low, the two least significant arbitration priority level bits can be programmed to achieve the range of arbitration levels. Consult the factory for other configurations.

Arbitration

Since the MCA 1200's arbitration priority levels range from 12 to 15 (1100 to 1111), the two most significant arbitration bits are always 1. Consequently ARB2 and 3, the two most significant arbitration bits are inputs only. ARB0 and 1, the bits which can be configured by the user, are both inputs and outputs which can both monitor and drive the bus.

When ARB/GNT* goes high the MCA 1200 will participate in the arbitration process if it has asserted PREEMPT*. ARB0-1 drive the local master's priority arbitration level to the bus. At the same time, ARB0-3 monitor the arbitration priority levels of the other participating masters. The MCA 1200 will compare its arbitration level with those of the other masters in the system. If there is another master in the system which asserts a higher level, the MCA 1200 will tri-state the outputs of ARB0-1, indicating that it will not win the bus for the current cycle. In this case it will continue to request the bus in future arbitration cycles until it wins arbitration.

If, on the other hand, the MCA 1200 in the local master has the highest arbitration level of all the masters currently requesting the bus, these other masters will tri-state their ARB0-3 outputs as they recognize that their priority level is lower. By the end of the arbitration cycle, the local master will be the only master driving ARB0-1. It will recognize that it is the only master driving the bus because the Micro Channel* arbitration level will be the same as the arbitration level it is driving to the bus. This condition, combined with ARB/GNT* going low to the bus grant state, enables MSTEN*, which signifies that the local master has achieved control of the bus.

If FAIRNESS is enabled, then the local master will be prohibited from enabling PREEMPT* during the next arbitration cycle, assuming it wins and controls the bus in the current cycle.

Data Transfer

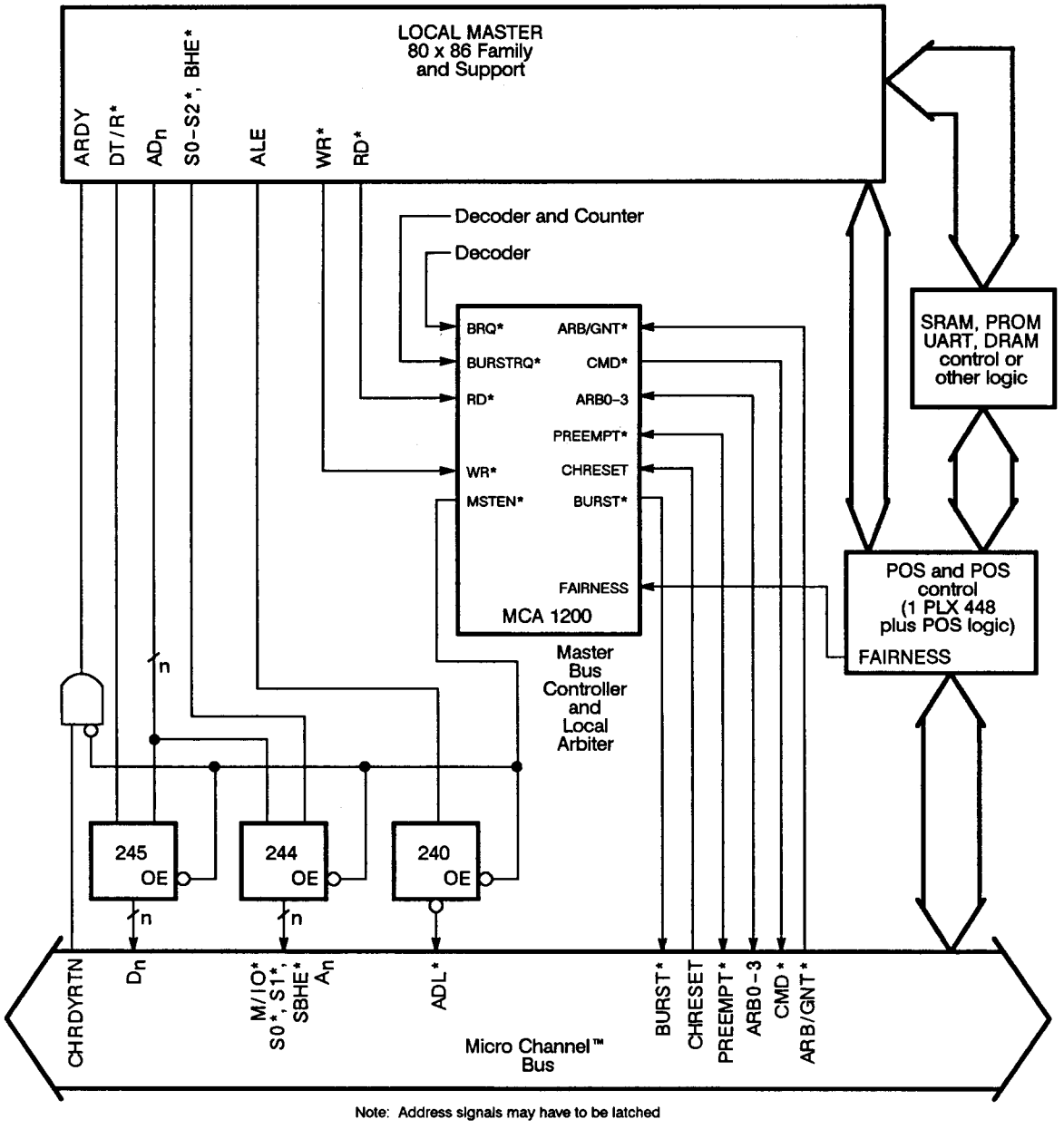
MSTEN* enables the address, data and status buffers. The assertion of MSTEN*, and the completion of the arbitration cycle (bus is granted) enables CMD* (and BURST* if a block of data is to be transferred) and releases PREEMPT*. The leading edge of CMD* indicates data is valid on the bus, and the trailing edge indicates the end of the data transfer.

The user must ensure that data is valid during a write cycle by the time WR* is enabled. This is important to ensure that there is valid data when CMD* is active.

During burst transfers, RD* or WR* strobes CMD* for each data cycle. BURST* is active during the transfer. The release of BURSTRQ* disables BURST*, which signifies the end of the address range. The trailing edge of BURST* indicates the end of the transfer.

Cycle Termination

The master owns the bus until the trailing edge of CMD*. After that, an arbitration cycle may begin. ARB/GNT* going high deasserts MSTEN* and the master no longer owns the bus.



Note: Address signals may have to be latched

Figure 2. MCA 1200 Master Bus Controller and Local Arbiter

MCA 1200 TIMING WAVEFORMS

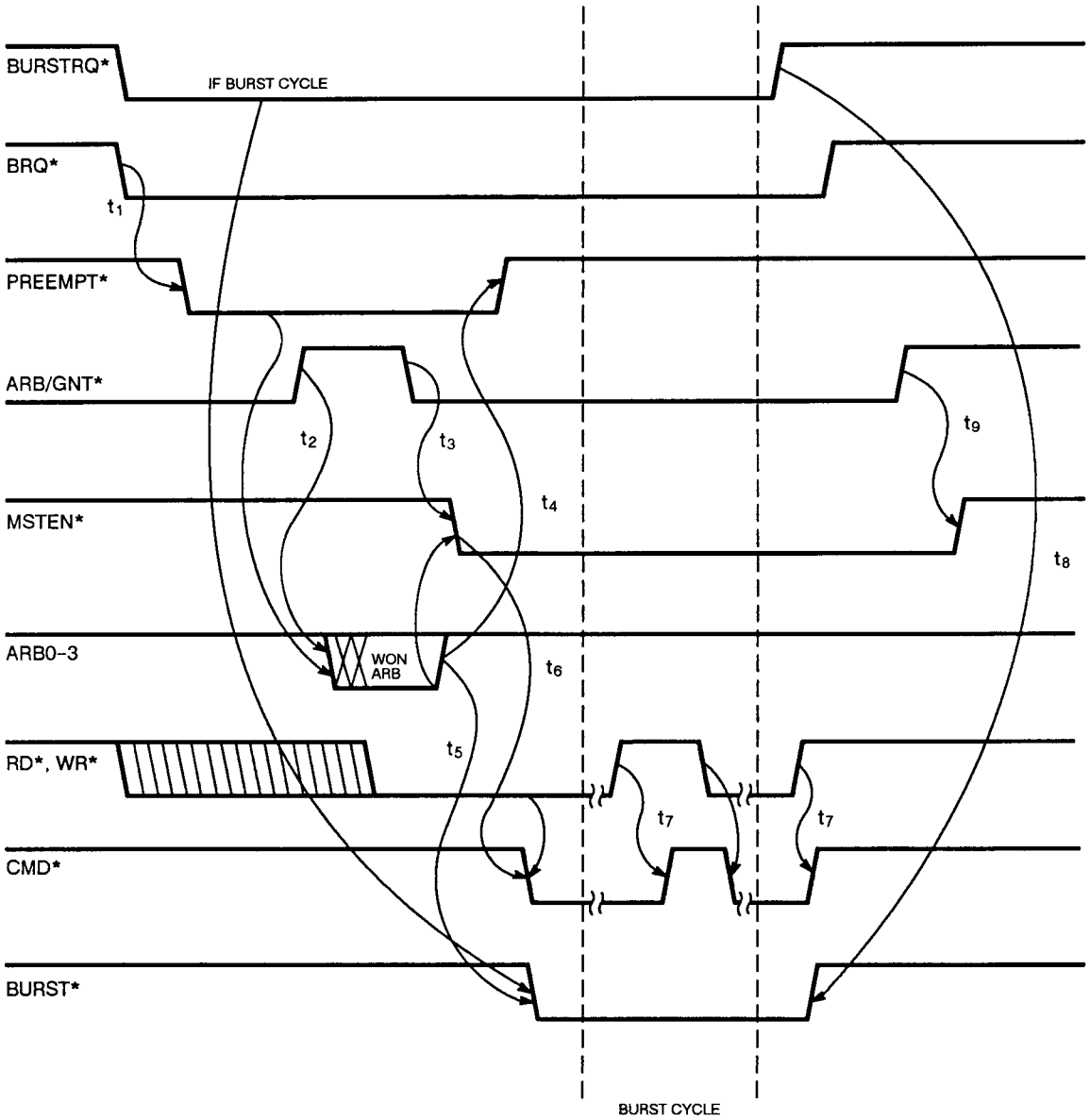


Figure 3. Micro Channel Master Controller Timing Diagram

MCA 1200 Timing Specifications

Timing Parameter	Signals	Max. Time (ns) -25, -45 parts unless otherwise specified	Description
t1	BRQ* to PREEMPT* enable	25, 45	
t2	ARB/GNT* to ARB0-3* enable	25, 45	PREEMPT* must be low
t3	ARB/GNT* to MSTEN* enable	25, 45	local master must win arbitration
t4	ARB0, 1 high to PREEMPT* disable	25, 45	
t5	ARB0, 1 high to BURST* enable	25, 45	BURSTRQ* must be low in addition
t6	MSTEN* to CMD*	25, 45	RD* or WR* must be low to enable CMD*.
t7	RD*, WR* to CMD*	25, 45	
t8	BURSTRQ* disable to BURST* disable	25, 45	
t9	ARB/GNT* high to MSTEN* disable	25, 45	MSTEN* disabled disables CMD* driver

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Ambient Temperature with
Power Applied ..... -55°C to +125°C
Supply Voltage to Ground
(pin 24 to pins 12, 18, & 20) ..... -0.5V to +7.0V
DC Voltage to Outputs in
High Z State ..... -0.5V to +7.0V

Operating Ranges

Commercial (C) Devices
Temperature Ambient ..... 0°C to +70°C
Supply Voltage (V_{CC}) ..... 5V ±5%

Electrical Characteristics Tested over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min, V_{IN} =V_{IH} or V_{IL}	I_{OH} = -3.0mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, V_{IN} =V_{IH} or V_{IL}	Output pins I_{OL} = 24mA		0.5	V
V_{IH}	Input HIGH Level			2.0		V
V_{IL}	Input LOW Level				0.8	V
I_{IX}	Input Leakage Current	V_{SS} <=V_{IN} <=V_{CC}, V_{CC} = Max		-10	10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{SS} < = V_{OUT} < = V_{CC}		-40	40	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_{OUT} = 0.5V		-30	-90	mA
I_{CC}	Power Supply Current	V_{CC} = Max, V_{IN} = GND Outputs Open			80	mA

Capacitance (sample tested only)

Parameter	Test Conditions	Pins	Typ	Units
C_{IN}	V_{IN} = 2.0V @ f = 1MHz	2-10	5	pF
		I/Os	10	pF
C_{OUT}	V_{IN} = 2.0V @ f = 1MHz	I/Os	10	pF

Package

The devices are available in a 24 pin slimline package. The plastic version comes in a 300 mil molded DIP P13.

The devices will also be available in LCC and PLCC versions. Contact the factory for availability of package types.