CMOS GATE ARRAY
TC110G SERIES GATE ARRAY

Toshiba introduces the new generation gate arrays — The TC110G series—capable of integrating 5X more than the TC17G series.

Uses Toshiba's proprietary HC²MOS/VLSI technologies. State of the art processing with high packing densities which produced a 4Mbit Dynamic RAM.

TC110G Series—50K gates/0.6ns. Compact and powerful!

General

Toshiba CMOS Gate Array family, TC110G Series, with interconnect routing which is not confined to "routing channels". This technique increases silicon efficiency (functions/mm^2).
Higher density and Toshiba HC^{2}MOS process provide subnanosecond speeds of 0.6ns typical gate delays (2-input NAND gate, fanout = 2, tpd.). TC110G Series is introduced as 14 base arrays with 1.4K to 50K estimated usable gates.
Gate Array design using TC110G Series is supported by the TOSHIBA MAINFRAME CAD SYSTEM. Hierarchical designs with large macro capabilites.

Product Specifications

	TC110G series
Process technology	HC^{2}MOS Si-gate double layer metal
	1.5μm
Gate speed (inner gate, typ.)	0.6ns
Maximum toggle frequency	150MHz
Supply voltage	5V
Application	ASTTL/ECL

Product Lines

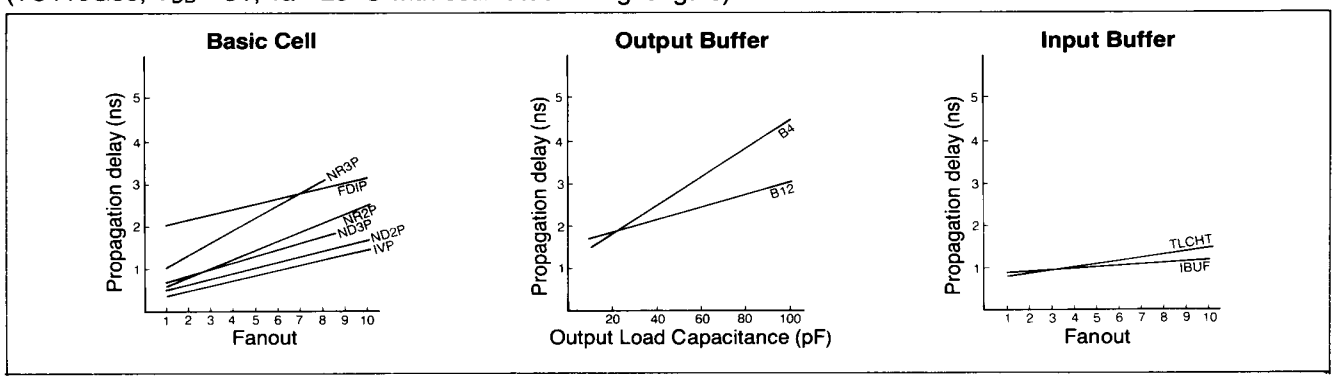
Part Number	Gate[1] Complexity	Estimated[2] Usable Gates	Maximum Pads[3]	Maximum I/O Pads[3][4]
TC110G C9	129,042	50,000	368	256
TC110G A0	100,182	40,000	326	256
TC110G 75	74,970	30,000	282	256
TC110G 51	50,904	20,000	234	226
TC110G 38	37,932	15,000	204	196
TC110G 32	32,000	13,000	188	180
TC110G 26	25,740	10,000	168	160
TC110G 21	21,060	8,400	154	146
TC110G 17	17,082	6,800	140	132
TC110G 14	14,204	5,600	128	120
TC110G 11	11,092	4,400	114	106
TC110G 08	8,000	3,200	100	92
TC110G 05	5,120	2,000	80	72
TC110G 03	3,498	1,400	68	60

Notes: 1. Raw-gates.
2. Based on 40% array utilization. Actual utilization varies, depending on cell types used.
3. Additional I/O pads may be configured as V_{DD}/V_{SS}, subject to number and drive of output buffers.
4. I/O signals presently limited to 256 by tester capability.

TAEC

Basic Cell Delay vs Fanout

(TC110G38, V_{DD} = 5V, Ta = 25°C with estimated wiring lengths)



Absolute Maximum Ratings (Vss = 0V)

Symbol	Parameter	Rating	Unit
V_{DD}	DC supply voltage	−0.3 to +7.0	V
V_{IN}	DC input voltage	−0.3 to V_{DD} + 0.3	V
I_{IN}	DC input current	±10	mA
Tstg	Storage temperature	−40 to +125	°C

Recommended Commercial Operating Conditions (Vss = 0V)

Symbol	Parameter	Rating	Unit
V_{DD}	DC supply voltage	4.75 to 5.25	V
Ta	Ambient temperature	0 to +70	°C

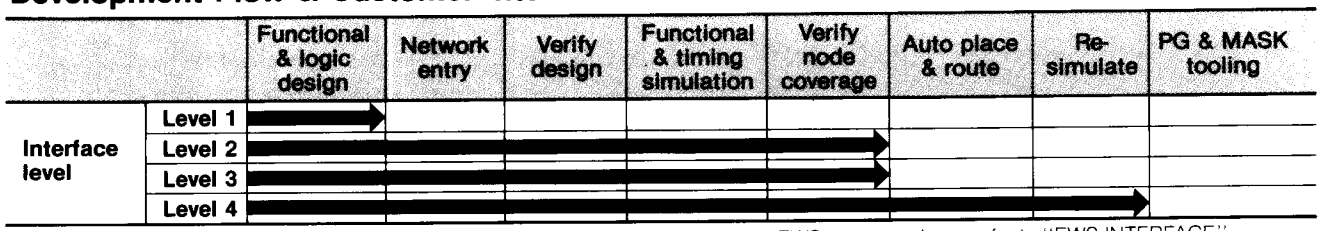
DC Electrical Characteristics

Specified at V_{DD} = 5V ±5% ambient temperature

Symbol	Parameter	Condition	TC110G Series Min.	TC110G Series Max.	Unit
V_{IH}	Low Level Input Voltage				V
	TTL Level		2.0		
	CMOS Level		3.5		
	SCHMITT Trigger		4.0		
V_{IL}	High Level Input Voltage				V
	TTL Level			0.8	
	CMOS Level			1.5	
	SCHMITT Trigger			1.0	
I_{IH}	High Level Input Current	$V_{IN} = V_{DD}$	−10	10	μA
	With Pull-down Resistors		10	200	
I_{IL}	Low Level Input Current	$V_{IN} = V_{SS}$	−10	10	μA
	With Pull-up Resistors		−200	−10	
V_{OH}	High Level Output Voltage		2.4		V
	Type B1	I_{OH} = −1mA			
	Type B2	I_{OH} = −2mA			
	Type B4	I_{OH} = −4mA			
	Type B6	I_{OH} = −6mA			
	Type B8	I_{OH} = −8mA			
	Type B12(1)	I_{OH} = −12mA			
V_{OL}	Low Level Output Voltage			0.4	V
	Type B1	I_{OL} = 1mA			
	Type B2	I_{OL} = 2mA			
	Type B4	I_{OL} = 4mA			
	Type B6	I_{OL} = 6mA			
	Type B8	I_{OL} = 8mA			
	Type B12(1)	I_{OL} = 12mA			
I_{OZ}	High Impedance Leakage Current	$V_{OUT} = V_{DD}$ or V_{SS}	−10	10	μA
	With Pull-up Resistors		−200	−10	
	With Pull-down Resistors		10	200	
I_{DD}	Quiescent Supply Current	$V_{IN} = V_{DD}$ or V_{SS}		100(2)	μA

Notes: (1) Requires two output pads. (2) Customer-Design Dependent

Development Flow & Customer Interface



(1) At level-2, design procedure takes place by customer at Toshiba LSI Design Center and at customer site for level-3.

(2) As for the EWS support, please refer to "EWS INTERFACE" (Document ID: SEMI-E-S1011)

CAS System Features ●TOSHIBA MAINFRAME CAD SYSTEM

Integrated Hierarchical Design System using Macrocell and Macrofunctions library for: ● Functional design ● Logic design ● Auto place & route ● Test pattern generation

High-speed logic simulation and Flexible auto place and route

Maximum circuit size: ●50K gates

Compatible interface language (TDL, TSTL)

Remote-access in man-machine environment

Package Adaptability List

As of June 1989

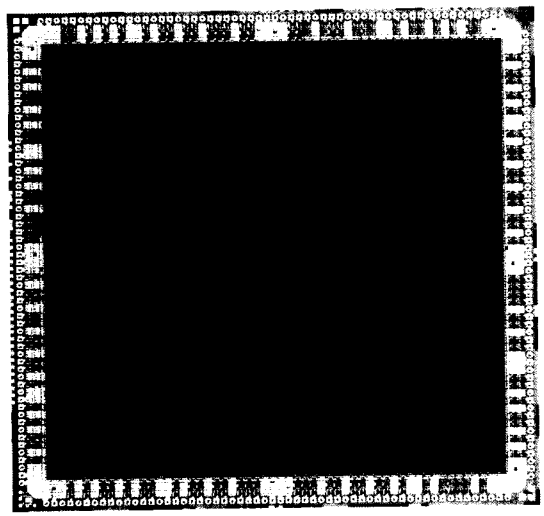
Package	Part Number	03	05	08	11	14	17	21	26	32	38	51	75	A0	C9
DIP	24	A	A	A	A										
	28	A	A	A	A	A									
	40	A	A	A	A	A	A								
	42	A	A	A	A	A	A								
	48	A	A	A	A	A	A								
	S42	A	A	A	A	A	A								
	S64		A	A	A	A	A	D	D						
PGA	64	A	A	A	A	A	A	A	A	A	A	A			
	68	A	A	A	A	A	A	A	A	A	A	A			
	84		A	A	A	A	A	A	A	A	A	A			
	100			A	A	A	A	A	A	A	A	A			
	120				A	A	A	A	A	A	A	A			
	135						A	A	A	A	A	A			
	144						A	A	A	A	A	A			
	180								A	A	A	A			
	224											A			
Metal PGA	120				A	A	A	A	A	A	A	A			
	144						A	A	A	A	A	A			
Cavity Down PGA	95										P	P	P		
	155										D	D	D	D	D
	223										A	A	A	A	A
	299												A	A	A
PLCC	44	A	A	A	A	A	A	P							
	68	A	A	A	A	A	A	A	A	A	A	D			
	84			A	A	A	A	A	A	A	A	D			
PFP Square	μ 44	A	A	A	D	D									
	44	A	A	A	A	A	A								
	60	A	A	A	A	A	A	D	D						
	100A[1]		A												
	100[1]			A	A	A	A	A	A	A	A	A			
	120					D	D	D	D	D	D	D			
	144			A	A	A	A	A	A	A	A	A	D	P	P
	160								A	A	A	A	A	P	P
	184							A	A	A	A	A	D	P	P
PFP Rectangular	64		A	A	A	A	A	P	P						
	80		A	A	A	A	A	A	P						
	100			A	A	A	A	P	P						
CFP	100[1]							A	A	A	A	A			
	144									A	A	A	D	D	D
	160									D	D	D	D	D	D
	184											D	D	D	D

A: Adaptable
D: Check with Toshiba for availability (Under development)
P: Check with Toshiba for availability (Under planning)

Notes: 1) Flat Package 100 pin is classified into 2 types determined by number of inner leads available: 100A—84 inner leads. 100—100 inner leads.
2) Please refer to "Package Selector Guide" (Document I.D. SEMI-E-S 1001) for further information in detail.

COMPACT AND POWERFUL!

TC110G Series Gate Array?



Part No.: TC110G 51
Used Gates: 15000 Gates

TC110G Series Library

TC17G series-compatible macrocells and macrofunctions
- Macrocell performance optimization (Standard/High drive)
- Macrocell equivalent to SSI/MSI

Functional block of Megacells, Megafunctions
- 2900 family
- Multiplier, Barrelshifter, ALU, CLA, FIFO
- LSI/VLSI CPU Peripheral

Building-block memory (32 to 16K bit)
- RAM cell: 3 gates
- ROM cell: 1/4 gate
- Customer-defined architecture

Macrocells

Logic Gate	62
Inverter/Internal Buffer	15
Tri-state Internal Buffer	6
Latch	22
Flip-flop	36
Decoder	8
Multiplexer	14
Adder	6
Input Buffer	48
Output Buffer	40
Bidirectional Output Buffer	324
Total	**581**

Macrofunction List

Function	Types	
	LSI Compatible	74HC Series Compatible
ADDERS	4	1
COMPARATORS	6	2
COUNTERS	19	11
DECODERS	10	4
FLIP-FLOPS	—	6
GATES	—	16
MULTIPLEXERS	11	10
REGISTERS	19	16
OTHERS	8	7
Total	**77**	**73**

RAM

RAM-C (SINGLE PORT RAM)	●Asynchronous ●Separated I/O, 3 state Output ●Max. 4608 Bit/Block (8 ~ 256 Word × 4 ~ 36 Bit) ●Read Access Time (t_{ACC}) 15ns typ.
RAM-E (TRIPLE PORT RAM)	●Asynchronous ●2 Read 1 Write ●Max. 1152 Bit/Block (16 ~ 64 Word × 4 ~ 18 Bit) ●Read Access Time(t_{ACC}) 11ns typ.

ROM

ROM-A (SINGLE PORT ROM)	●Asynchronous ●Max. 16384 Bit/Block (64 ~ 1024 Word × 2 ~ 32 Bit) ●Read Access Time(t_{ACC}) 18ns typ.

Features

- Proprietary 1.5μm HC^{2}MOS/VLSI process technology.
- 0.6ns speed (2-input NAND gate, fanout = 2, tpd.)
- Achieves ultra high speed equivalent to 10K ECL.
- High packing density up to 129K raw gates.
- 3K to 129K raw gates.
- Up to 256 I/O pins.
- Variable channel width architecture allows efficient silicon utilization.
- Full input/output TTL/CMOS compatibility.
- Advanced packaging techniques.
- Design is fully supported by TOSHIBA MAINFRAME CAD SYSTEM
- Programmable I/O cells with slew rate control (e.g. Output drive up to 12mA).
- Large macro capability (e.g. RAMs, ROMs, Megafunctions, Megacells*).
- Performance optimization (e.g. Standard/High drive cells).

*: Scheduled to be released gradually.

TC110G Series Base Array

- Variable routing track and column
- Max. 129K raw gates (1 raw gate = 2 pairs of Pch./Nch. transistor = 4 transistors)