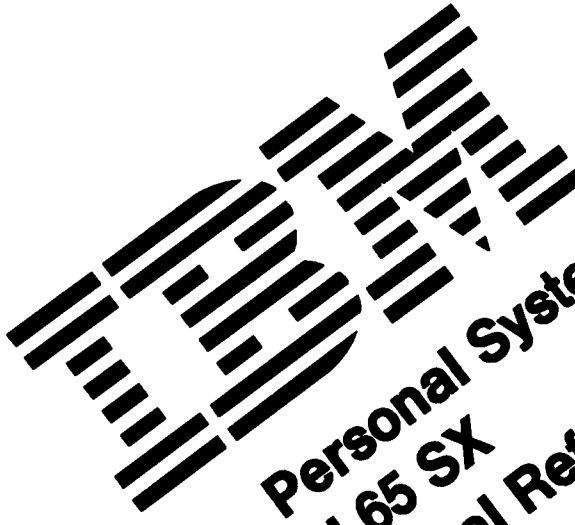

Personal System/2
Model 65 SX
Technical Reference

Second Edition (October 1990)

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Preface

This technical reference contains hardware and software interface information specific to the IBM Personal System/2 Model 65 computer. It is intended for those who develop hardware and software products for these systems. Users should understand computer architecture and programming concepts.

This publication consists of the following sections:

Section 1, "System Overview," describes the system, features and specifications.

Section 2, "Programmable Option Select," describes registers used for configuration.

Section 3, "System Board," describes the system specific hardware implementations.

This technical reference should be used with the following publications:

IBM Personal System/2 Hardware Interface Technical Reference — Architectures

IBM Personal System/2 Hardware Interface Technical Reference — Common Interfaces

IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference

These publications contain additional information on many of the subjects discussed in this technical reference.

Warning: The term *reserved* describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

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Section 1. System Overview

Notes:

Description

The IBM* Personal System/2* Model 65 SX computer is a self-contained, floor-standing computer that features the Micro Channel* architecture. The system comes with a keyboard, and can accommodate up to five internal drives, such as two internal diskette drives, two internal fixed disk drives, and a tape drive or CD-ROM.

Programs can identify the system by reading the model and submodel bytes. The model and submodel bytes for the Model 65 SX are:

Byte	Value
Model	F8
Submodel	1C

Interrupt hex 15, function code (AH) = hex C0, returns the model byte, submodel byte, and BIOS revision code.

Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* manual for a listing of the model and submodel bytes for other systems, and check the "Supplements" section for updates to that listing.

System-Board Features

The following table lists the system-board devices and features of the Model 65 SX. The Hardware Interface Technical Reference manuals describe devices common to PS/2* products by type number.

* IBM, Personal System/2, PS/2, and Micro Channel are trademarks of the International Business Machines Corporation.

Device	Type	Features
Microprocessor	---	80386SX**
		24-bit address and 16-bit data interface
System Timers	1	Channel 0 – System timer
		Channel 2 – Tone generation for speaker
		Channel 3 – Watchdog timer
ROM Subsystem	---	128KB (KB = 1024 bytes)
RAM Subsystem	---	1 to 8MB (MB = 1,048,576 bytes)
		Expandable on the channel
CMOS RAM Subsystem	---	64-byte CMOS RAM with real-time clock/calendar
		2KB CMOS RAM extension
		Battery backup
Video Subsystem	1	Auxiliary connector on the channel
		Analog output
		256KB video memory
Audio Subsystem	1	Driven by:
		- System-timer channel 2
		- The 'audio sum node' signal
DMA Controller	1	Eight independent DMA channels
		Single or burst transfers and read verification
Interrupt Controller	1	16 levels of system interrupts
		Interrupts are level-sensitive
Keyboard/Auxiliary Device Controller	1	Keyboard connector
		Auxiliary-device connector
		Password security
Diskette-Drive Controller	1	Supports:
		- 1.44MB formatted-diskette density
		- 720KB formatted-diskette density
Serial Controller	2	RS-232C interface
		Programmable as serial port 1 or 2
		FIFO mode* and character mode
Parallel Controller	1	Programmable as parallel port 1, 2, or 3
		Supports bidirectional input and output
Micro Channel	---	Eight channel connectors for Type 3 adpaters:
		- Seven 16-bit connectors
		- One 16-bit connector with an auxiliary-video extension
Math Coprocessor Socket	---	Supports 80387SX** math-coprocessor option
		Same clock speed as the system microprocessor

* The Model 65 SX supports FIFO through ABIOS calls only.

Figure 1-1. System-Board Devices and Features

Additional memory can be added in any available Micro Channel connector; however, the total amount of memory installed must not exceed the 16MB addressing limit.

** 80386SX and 80387SX are trademarks of the Intel Corporation.

System-Board I/O Address Map

Figure 1-2 shows the address map for the various system-board I/O functions.

Address (Hex)	Device
0000 - 001F	DMA Controller (0 – 3)
0020, 0021	Interrupt Controller (Master)
0040, 0042 - 0044, 0047	System Timers
0060	Keyboard, Auxiliary-Device
0061	System-Control Port B
0064	Keyboard, Auxiliary-Device
0070, 0071	RT/CMOS and NMI Mask
074 - 076	2KB CMOS RAM extension
0081 - 0083, 0087	DMA Page Registers (0 – 3)
0089 - 008B, 008F	DMA Page Registers (4 – 7)
0090	Central Arbitration Control Point
0091	Card-Selected Feedback Register
0092	System-Control Port A
0094	System-Board Enable/Setup Register
0096	Adapter Enable/Setup Register
00A0, 00A1	Interrupt Controller (Slave)
00C0 - 00DF	DMA Controller (4 – 7)
00F0 - 00FF	Math Coprocessor
0100 - 0107	Programmable Option Select
0278 - 027B	Parallel Port 3
02F8 - 02FF	Serial Port 2 (RS-232C)
0378 - 037B	Parallel Port 2
03B4, 03B5, 03BA	Video Subsystem
03BC - 03BF	Parallel Port 1
03C0 - 03C5	Video Subsystem
03C6 - 03C9	Video DAC
03CE, 03CF	Video Subsystem
03D4, 03D5, 03DA	Video Subsystem
03F0 - 03F7	Diskette-Drive Controller
03F8 - 03FF	Serial Port 1 (RS-232C)

Figure 1-2. System-Board I/O Address Map

Specifications

Device	Number of Waits	Cycle Time (ns)
Microprocessor (16 MHz, 62.5 ns Clock)		
Access to System-Board RAM: *		
Memory Read (Page Hit)	0	125
Memory Read (Anticipated Page Miss)	1	187.5
Memory Read (Page Miss)	2	250
Memory Write (Page Hit)	1	187.5
Memory Write (Anticipated Page Miss)	1	187.5
Memory Write (Page Miss)	2	250
Access to Channel:		
Default Transfer Cycle	2	250
Synchronous Transfer Cycle	4	375
Access to ROM	3	312.5
Refresh Rate (typically performed every 15.1 μs)		625 (min)
Bus-Master Access to System Board RAM		300 (min)
DMA Controller (8 MHz, 125 ns Clock):		
Single Transfer: 375 + (I/O Access + Memory Access)		
Burst Transfer: 375 + (I/O Access + Memory Access)N **		
System-Board Memory Access		375
Default Transfer Cycle		250
Synchronous Transfer Cycle		375

* Adapters installed in the channel should not rely on monitoring system board memory access, because channel-memory control signals may not be present during these accesses.
** N is the number of transfers in the burst.

Figure 1-3. Performance Specifications

Note: The cycle times shown for access to system board RAM is based on 85- or 100-nanosecond memory.

Size	
Width	165 mm (6.5 in.)
Depth	483 mm (19.0 in.)
Height	597 mm (23.5 in.)
Weight (with one fixed disk drive)	20.6 kg (45.3 lb)
Cables	
Power Cable	1.8 m (6 ft)
Keyboard Cable	3.05 m (10 ft)
Air Temperature	
System On	10.0 to 35.0°C (50 to 95°F)
System Off	10.0 to 43.0°C (50 to 110°F)
Humidity	
System On	8% to 80%
System Off	8% to 80%
Maximum Altitude	2133.6 m (7000 ft)
Heat Output	390 Watts (1330 BTUs/hour)
Acoustical Readings	(See Figure 1-5 on page 1-8)
Electrical Input:	
Input Voltage (Range is automatically selected; sinewave input is required):	
Low Range	90 (min) – 137 (max) Vac
High Range	180 (min) – 265 (max)Vac
Frequency:	
Low Range	47 (min) – 53 (max) Hz
High Range	57 (min) – 63 (max) Hz
Input in Kilovolt-Ampere (kVA):	
Minimum configuration (as shipped by IBM)	0.10 kVA
Maximum configuration	0.65 kVA
Electromagnetic Compatibility	FCC Class B

Figure 1-4. Physical Specifications

Description	L_{WAd} in bels		L_{pAm} in dB		$<L_{pA}>_m$ in dB	
	Operate	Idle	Operate	Idle	Operate	Idle
Model 65 SX	5.3	5.3	41	40	36	36

Notes:

L_{WAd} is the declared sound power level for the random sample of machines.

L_{pAm} is the mean value of the A-weighted sound pressure levels at the operator position (if any) for the random sample of machines.

$<L_{pA}>_m$ is the mean value of the A-weighted sound pressure levels at the one-meter positions for the random sample of machines.

All measurements are made in accordance with ANSI S12.10, and reported in conformance with ISO DIS 9296.

The measurements are preliminary data and subject to change.

Figure 1-5. Declared Acoustical Noise Emission Values

Power Supply

The power supply requires a sinewave input and converts the ac input voltage to three dc output voltages. The power supply provides power for the following:

- System board
- Channel adapters
- Internal DASD drives
- Auxiliary device
- Keyboard.

The power switch and two light-emitting diodes (LEDs) are on the front of the system unit. The green LED indicates that the power supply is operating. The yellow LED indicates fixed disk drive activity.

Outputs

The power supply provides separate voltage sources for the system board and the drives. The system-board voltages are +5 Vdc, +12 Vdc, and −12 Vdc. The drive voltages are +5 Vdc and +12 Vdc. The following is a list of the power provided for each of the components.

System Component	Maximum Current	
	+12 Vdc	+5 Vdc
Internal Fixed Disk Drives (per power supply connector)	2.5 A	1.5 A
Auxiliary Device	None	300 mA
Keyboard	None	275 mA

Figure 1-6. Component Maximum Current

The following are the load currents allowed for each channel connector.

Supply Voltage	Maximum Current
+ 5.0 Vdc	1.6 A
+12.0 Vdc	0.175 A
−12.0 Vdc	0.040 A

Figure 1-7. Channel Load Current

The formulas used to determine the power requirements and the voltage regulation tolerances are in the Micro Channel adapter

design information in the *Hardware Interface Technical Reference - Architectures* manual.

Output Protection

A short circuit placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state with no damage to the power supply.

If an overvoltage fault occurs (internal to the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of its nominal value.

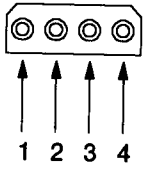
If either of these shutdown states is actuated, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least ten seconds.

Voltage Sequencing

At power-on time, the output voltages track within 50 milliseconds of each other when measured at the 50% points.

Power Supply Connectors

The power supply provides two 4-pin connectors for internal fixed disk drives. These connectors can be extended to provide power to more than one internal drive as long as the total power does not exceed the specifications shown in Figure 1-6 on page 1-9.



Pin	Signal
1	+12 Vdc
2	DC Return
3	DC Return
4	+5 Vdc

Figure 1-8. Voltage Assignments for the Internal Drive Power-Supply Connectors

Section 2. Programmable Option Select

Notes:

Description

Programmable Option Select (POS) eliminates the need for switches by replacing their function with programmable registers. This section describes the POS information used specifically by the the Model 65 SX system board. For additional POS information, refer to the Hardware Interface Technical Reference Micro Channel architecture information.

Warning:

- IBM recommends that programmable options be set only through the System-Configuration utilities. Directly setting the POS registers or CMOS RAM POS parameters can result in multiple assignments of the same system resource, improper operation of the feature, loss of data, or damage to the hardware.
- Application programs should not use the adapter identification (ID) unless absolutely necessary. Compatibility problems can result.
- If an adapter and the system board are in setup mode at the same time, bus contention occurs. When this happens, no useful programming can take place, and damage to the hardware can occur.
- After setup operations are complete, the Adapter Enable/Setup register (hex 0096) should be set to hex 00, and the System-Board Enable/Setup register (hex 0094) should be set to hex FF.
- The channel-reset bit (bit 7) in the Adapter Enable/Setup register (hex 0096) must be set to 0 to program the adapters.
- The system board does not support 16-bit I/O operations to 8-bit POS registers. Using 16-bit I/O instructions on 8-bit POS registers causes incorrect data to be written to or read from the registers. The system board supports only 8-bit transfers for setup operations.

Setup functions respond to I/O addresses hex 0100 through 0107 only when the setup signal is active. The following precautions must be taken before setting individual bits in the POS registers.

System-Board Video Subsystem Setup:

- Bit 5 in the System-Board Enable/Setup register (hex 0094) must be set to 0 to place the system-board video into the setup mode.
- Bit 3 in the Adapter Enable/Setup register (hex 0096) must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bit 7 in the System-Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to other system-board functions.

Adapter Setup:

- Bit 3 in the Adapter Enable/Setup register must be set to 1 to allow adapter setup.
- Bit 5 in the System-Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the video subsystem.
- Bit 7 in the System-Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to a system-board function.

Other System-Board Setup Requirements:

- Bit 7 in the System-Board Enable/Setup register must be set to 0 to allow setup of other system-board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.
- Bit 5 in the System-Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to the video subsystem.

System-Board POS Address Map

The following table shows the organization of the I/O address space used by system-board POS.

Address (Hex)	Function
0094	System-Board Enable/Setup Register
0096	Adapter Enable/Setup Register
0100	POS Register 0—Reserved
0101	POS Register 1—Reserved
0102	POS Register 2—System-Board I/O Register
0103	POS Register 3—Memory-Enable Register
0104	POS Register 4—Memory-Presence Register
0105	POS Register 5—Memory-Control Register
0106	Reserved
0107	Reserved

Figure 2-1. System-Board POS I/O Address Map

Card-Selected Feedback

Whenever the system addresses an adapter, the adapter responds by setting the '-card-selected feedback' signal (-CD SFDBK) to active. -CD SFDBK is derived from the address decode, driven by a totem-pole driver, and latched by the system board. It can be read through the Card-Selected Feedback register at address hex 0091. Diagnostic and automatic configuration programs use this signal to verify the operation of an adapter at a given address or DMA port. This signal must not be active during a setup cycle.

The Card-Selected Feedback register is a read-only register at address hex 0091. It allows programs to monitor -CD SFDBK and determine if the video subsystem, system-board I/O, or an adapter is addressed and functioning.

Bit	Function
7 - 1	Reserved
0	Card-Selected Feedback

Figure 2-2. Card-Selected Feedback Register (Hex 0091)

Bits 7 - 1 Reserved.

Bit 0 This bit is set to 1 whenever -CD SFDBK was active on a previous cycle or whenever the system-board I/O functions (diskette drive, serial, or parallel interfaces) are accessed by an I/O cycle. Reading this register resets the bit to 0.

System-Board Setup

The integrated I/O functions on the system board use POS information during setup. POS treats the diskette-drive controller, serial port, and parallel port as a single device. The video subsystem also is an integrated part of the system board, but POS treats it as a separate device. The System-Board Enable/Setup register is used to place the system board or the video subsystem in the setup mode.

System-Board Enable/Setup Register (Hex 0094)

This is a read/write register. All bits in this register default to 1 (enabled).

Bit	Function
7	Enable/-Setup System-Board Functions
6	Reserved
5	Enable/-Setup Video Subsystem
4 - 0	Reserved

Figure 2-3. System-Board Enable/Setup Register (Hex 0094)

Bit 7 When set to 0, this bit places various system-board I/O functions in the setup mode. The diskette-drive controller, serial port, and parallel port are controlled through System-Board POS Register 2 (hex 0102). The POS information for memory is in System-Board POS Register 3 (hex 0103), POS Register 4 (hex 0104), and POS Register 5 (hex 0105).

When set to 1, this bit enables the system-board functions.

Bit 6 This bit is reserved.

Bit 5 When set to 0, this bit places the video subsystem in the setup mode, and control is through POS Register 2 (hex 0102). When this bit is set to 1 and bit 0 in POS Register 2 is set to 1, video is enabled.

Bit 0 of POS Register 2 is the video-enable bit. When this bit is set to 0, the video subsystem does not respond to commands, addresses, or data. If video is being generated when the video-enable bit is set to 0, the output is still generated. For information on BIOS calls to enable or disable the video, see the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* manual.

Note: When video is disabled, access to the digital-to-analog converter (DAC) registers is disabled.

Bits 4 - 0 These bits are reserved.

System-Board POS Register 2 (Hex 0102)

When the system board is in the setup mode, this read/write register controls the diskette-drive controller, serial port, and parallel port. Reading this register returns the current state of the following system-board functions.

Bit	Function
7	Disable Parallel-Port Extended Mode
6, 5	Parallel-Port Select
4	Enable Parallel Port
3	Serial-Port Select
2	Enable Serial Port
1	Enable Diskette-Drive Interface
0	Enable System Board

Figure 2-4. System-Board POS Register 2 (Hex 0102)

Bit 7 When set to 0, this bit allows the parallel port to be configured as an 8-bit, parallel, bidirectional interface. When set to 1, this bit disables the bidirectional mode. This bit is set to 0 at power-on time, and the power-on self-test (POST) sets it to 1.

Bits 6, 5 These bits select the configuration of the system-board parallel port.

Bits 6 5	Assignment	Address (Hex)	Interrupt Level
0 0	Parallel 1	03BC - 03BE	7
0 1	Parallel 2	0378 - 037A	7
1 0	Parallel 3	0278 - 027A	7
1 1	Reserved	----------	-

Figure 2-5. Parallel-Port Select Bits

Bit 4 When this bit and bit 0 are set to 1, the system-board parallel port is enabled.

Bit 3 When set to 1, this bit sets the system-board serial port as Serial 1 (addresses hex 03F8 through 03FF), which uses interrupt level 4. When set to 0, this bit sets the serial port as Serial 2 (addresses hex 02F8 through 02FF), which uses interrupt level 3.

Bit 2 When this bit and bit 0 are set to 1, the system-board serial port is enabled.

Bit 1 When this bit and bit 0 are set to 1, the diskette-drive interface is enabled.

Bit 0 When set to 1, this bit allows bits 4, 2, and 1 to enable and disable their respective devices. When set to 0, this bit disables the system-board parallel port, the system-board serial port, and the diskette-drive interface, regardless of the state of bits 4, 2, and 1.

System-Board POS Register 3 (Hex 0103)

When the system board is in setup mode, this read/write register controls the system-board memory.

Bit	Function
7 - 1	Reserved
0	Enable System-Board RAM

Figure 2-6. System-Board POS Register 3 (Hex 0103)

Bits 7 - 1 These bits are reserved.

Bit 0 When set to 1, this bit enables system-board memory. When set to 0, this bit disables system-board memory. All RAM installed on the system board is enabled or disabled by this operation.

System-Board POS Register 4 (Hex 0104)

The system board has two memory connectors that support 1MB, 2MB, and 4MB memory cards. This read/write register contains information about the memory cards installed. POS Register 5 defines the connector.

Bit	Function
7 - 4	Memory Card ID
3 - 0	Enable Memory Card

Figure 2-7. System-Board POS Register 4 (Hex 0104)

Bits 7 - 4 Bits 7 through 4 provide the memory card ID.

Bits 7 6 5 4	Size	Speed
0 0 0 0	4MB	80 ns
0 0 0 1	2MB	100 ns
0 0 1 0	1MB	100 ns
0 0 1 1 - 0 1 0 0	Reserved	--
0 1 0 1	2MB	80 ns
0 1 1 0	1MB	80 ns
0 1 1 1 - 1 1 0 0	Reserved	--
1 1 0 1	2MB	120 ns
1 1 1 0	1MB	120 ns
1 1 1 1	No memory card installed	--

Figure 2-8. Memory Card ID Bits

4MB Memory Cards

Bits 3 - 0 When set to 1, a 4MB memory card is enabled

1MB and 2MB Memory Cards

Bits 3, 2 Reserved

Bit 1 When set to 1, this bit enables the second 1MB on a 2MB memory card.

Bit 0 When set to 1, this bit enables a 1MB memory card or the first 1MB on a 2MB memory card.

System-Board POS Register 5 (Hex 0105)

This is the memory-control register.

Bit	Function
7, 6	Reserved
5	640KB - 1MB Split Enable
4	ROM Enable
3	Memory-Access Speed
2 - 0	Memory-Connector Select Bit for POS Register 4

Figure 2-9. System-Board POS Register 5 (Hex 0105)

Bits 7, 6 These bits are reserved.

Bit 5 When set to 0, this bit enables the system-board RAM between 640KB and 1MB. Typically, 128KB of this memory is mapped to the system-board ROM address space, and the remaining 256KB is mapped to the first

available address following the last full 1MB block of activated system-board memory. When set to 1, this bit disables system-board RAM between 640KB and 1MB.

Bit 4 This bit determines how addresses hex 0E0000 to 0FFFFF are assigned.

When set to 1, this bit enables ROM; the system assigns the read-access addresses to ROM and the write-access addresses to RAM. When set to 0, this bit disables ROM; the system assigns the read-access addresses to RAM and disables the write-access addresses. Bit 5 of this register must be set to 0 before ROM can be disabled.

Bit 3 When set to 0, this bit sets the memory-access speed to 1, 2, or 3 wait states. When set to 1, this bit sets the memory-access speed to 0, 1, or 2 wait states. This bit is set to 0 by a power-on reset. For more information on memory-access speed, see Figure 1-3 on page 1-6.

Bits 2 - 0 These bits select the memory connector to be used by POS Register 4.

Bits 2 1 0	Function
0 0 0	Memory Connector 1
0 0 1	Memory Connector 2
0 1 0 - 1 1 1	Reserved

Figure 2-10. Memory-Connector Select for POS Register 4

Adapter Setup

The Adapter Enable/Setup register (hex 0096) selects the channel connector to be configured.

Bit	Function
7	Channel Reset
6 - 4	Reserved
3	Card-Setup Enable
2 - 0	Channel Select 2 - 0

Figure 2-11. Adapter Enable/Setup Register (Hex 0096)

Bit 7 When set to 1, this bit activates the 'channel reset' signal to all connectors.

Bits 6 - 4 These bits are reserved.

Bit 3 When set to 1, this bit enables the '-card setup' signal (-CD SETUP) selected by bits 2 through 0.

Bits 2 - 0 These bits are the address bits for -CD SETUP. Connectors 1 through 8 are addressed as 0 through 8, respectively. When bit 3 is set to 1, these bits select the connector that is put into setup mode.

Associated with each channel connector is a unique '-card setup' signal used to put the adapters in the setup mode, which allows access to the POS registers. The individual connectors are selected through the Adapter Enable/Setup register. Setup information is then read from or written to the selected adapter through I/O addresses hex 0100 through 0107.

Notes:

1. -CD SETUP goes active only when an operation is performed in the I/O address range of hex 0100 through 0107.
2. The status of the Adapter Enable/Setup register (hex 0096) can be read by a program. however, when the register is read, bits 6 through 4 are set to 1.

Section 3. System Board

Notes:

Description

This section describes the microprocessor, math coprocessor, channel differences, memory subsystems, and miscellaneous system ports and connectors for the Model 65 SX. Additional information on these topics can be found in the *Hardware Interface Technical Reference* listed in the preface of this manual.

Microprocessor and Math Coprocessor

The Model 65 SX uses an 80386SX Microprocessor that runs at 16 MHz and has a 24-bit address and a 16-bit data interface. The 80386SX Microprocessor is software compatible with the 80386 Microprocessor.

The 80387SX Math Coprocessor matches the speed of the system microprocessor and operates in the synchronous mode. The 80387SX Math Coprocessor is software compatible with the 80387 Math Coprocessor.

Micro Channel Implementation

This section describes the implementation of the Micro Channel architecture on the Model 65 SX system. For more information, refer to the Hardware Interface Technical Reference Micro Channel architecture information.

Exception Reporting

Exceptions should be reported using the asynchronous channel check procedure. The synchronous channel check procedure is not supported.

Central Arbiter

The central-arbitration control point gives intelligent subsystems on the channel the ability to share and control the system. It allows burst-data transfers and prioritization of control between devices. The central arbiter supports up to 15 arbitrating devices (levels 0 through E) and the system microprocessor (level F).

Arbitration-Bus Priority Assignments

The following figure shows the assignment of arbitration levels. The functions with the lowest arbitration level have the highest priority.

ARB Level	Primary Assignment
-2	Memory Refresh
-1	NMI
0	DMA Channel 0 (Programmable to any arbitration level)
1	DMA Channel 1
2	DMA Channel 2
3	DMA Channel 3
4	DMA Channel 4 (Programmable to any arbitration level)
5	DMA Channel 5
6	DMA Channel 6
7	DMA Channel 7
8 - E	Available
F	System Microprocessor

Figure 3-1. Arbitration-Bus Priority Assignments

Note: Devices designed for arbitration level 0 or 1 should have limited bandwidth or short bursts so diskette overruns can be prevented or recovered by retry operations. The diskette-drive controller on arbitration level 2 can be held inactive by devices on levels 0 and 1 by a refresh operation, and by the previous controlling master. The diskette-drive controller should not be held inactive for more than 12 microseconds to prevent data overruns.

Nonmaskable-interrupt (NMI) service executes at a priority level higher than 0, called -1. Memory refresh is prioritized at -2, two levels higher than 0. Levels -1 and -2 are reached on the system board only, while the 'arbitrate/-grant' signal (ARB/-GNT) is in the arbitrate state.

When the central-arbitration control point receives a level -1 request (NMI, a system-board internal signal), it activates -PREEMPT, waits for the end of transfer, and then places ARB/-GNT in the arbitrate state, which denies channel activity to arbitrating devices. The central-arbitration control point gives the grant to the level -1 request, and holds ARB/-GNT in the arbitrate state until the operation is complete and the NMI service is reset.

Central-Arbiter Programming

The central-arbitration control point provides access to programmable options through the Arbitration register, which is accessed at I/O address hex 0090. The bit definitions are different for read and write operations, as shown in the following tables.

Bit	Definition
7	Enable System-Microprocessor Cycle
6	Arbitration Mask
5	Enable Extended Arbitration (Not Supported)
4 - 0	Reserved

Figure 3-2. Arbitration Register, Write to Hex 0090

Bit	Definition
7	Enable System-Microprocessor Cycle
6	Arbitration Masked by NMI
5	Bus Time-Out
4	Reserved
3 - 0	Value of Arbitration Bus during Previous Grant State

Figure 3-3. Arbitration Register, Read Hex 0090

Bit 7 When set to 1, this bit enables system-microprocessor cycles during arbitration cycles. This bit can be set to 0 if an arbitrating device requires total control of the channel bandwidth. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates system-microprocessor cycles are enabled during arbitration.

Bit 6 When set to 1, this bit causes the central-arbitration control point to enter the arbitration state. The system microprocessor controls the channel until this bit is reset to 0. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates that an NMI has occurred and has masked arbitration.

Warning: This bit should be set to 1 only by diagnostic routines and system error-recovery routines.

Bit 5 When set to 1, this bit extends the arbitration cycle from a minimum of 400 nanoseconds to a minimum of 800 nanoseconds. The Model 65 SX does not support this mode of operation. When set to 1, this bit can cause unpredictable results.

Reading this bit as a 1 indicates that a bus time-out has occurred. The bus time-out indication is not reset until bit 6 of this register is set to 0.

Bit 4 This bit is reserved and should be set to 0.

Bits 3 - 0 These bits are undefined for a write operation and should be set to 0.

Reading these bits returns the arbitration level of the arbiter controlling the channel during the most recent grant state. This information allows the system microprocessor to determine the arbitration level of the device that caused a bus time-out.

Micro Channel Connectors

The Model 65 SX system board provides eight micro channel connectors:

- Seven 16-bit connectors
- One 16-bit connector with an auxiliary-video extension.

Diskette-Drive Controller

The system board uses the Type 1 diskette-drive controller. The following table shows the signal assignments and pin numbering for the 2- by 20-pin connector used in the Model 65 SX.

Pin	I/O	Signal	Pin	I/O	Signal
1	N/A	Drive 2 Installed	2	O	-Reduce Write
3	O	+5 Vdc	4	N/A	-Drive ID
5	N/A	Ground	6	O	+12 Vdc
7	N/A	Ground	8	I	-Index
9	N/A	Ground	10	O	-Motor Enable 0
11	N/A	Ground	12	O	-Drive Select 1
13	N/A	Ground	14	O	-Drive Select 0
15	N/A	Ground	16	O	-Motor Enable 1
17	N/A	Ground	18	O	-Direction
19	N/A	Ground	20	O	-Step
21	N/A	Ground	22	O	-Write Data
23	N/A	Ground	24	O	-Write Enable
25	N/A	Ground	26	I	-Track 0
27	N/A	Ground	28	I	-Write Protect
29	N/A	Ground	30	I	-Read Data
31	N/A	Ground	32	O	-Head 1 Select
33	N/A	Ground	34	I	-Diskette Change
35	N/A	Ground	36	N/A	Ground
37	N/A	+Slim/-Half High	38	O	+5 Vdc
39	N/A	Ground	40	O	+12 Vdc

Figure 3-4. Diskette-Drive Connector

Memory

The Model 65 SX uses the following types of memory:

- Read-only memory (ROM)
- Random access memory (RAM)
- Real-time clock and CMOS RAM (RT/CMOS RAM).

ROM Subsystem

The ROM subsystem consists of 128KB. ROM is active at power-on time and is assigned the top of the first and last 1MB of address space (0E0000 to 0FFFFF and FE0000 to FFFFFF). After POST ensures that system memory is operating properly, the ROM code is copied to RAM at the same address space, and ROM is disabled.

The ROM enable bit in System-Board POS Register 5 (hex 0105) controls ROM or RAM access at address space hex 0E0000 to 0FFFFF. When enabled, ROM is not parity-checked and operates with three 62.5-nanosecond wait states.

RAM Subsystem

The RAM subsystem on the system board starts at address hex 000000 of the address space. The RAM subsystem is 18 bits wide: 16 data bits and 2 parity bits. One parity bit is generated for each byte of data written. During a read operation, one parity bit is checked for each byte of data read by the device controlling the bus.

The system board contains two 72-pin memory connectors. Each connector can support 1MB, 2MB, or 4MB of memory. The system enables and disables memory in 1MB blocks. Each 1MB block must start on a 1MB boundary. Because 128KB of I/O ROM, 128KB of system-board ROM, and 128KB of video memory are mapped within the first 1MB of address space, the first physical 1MB of RAM cannot be mapped to contiguous addresses and is therefore split at the 640KB boundary, creating a 384KB overflow. The high 128KB of the overflow is mapped to the system-board ROM address space; the remaining 256KB, called the *split-memory block*, is either disabled or mapped to the first available address following the last full 1MB of activated system-board memory. Split-memory-block remapping and disabling are controlled by System-Board POS Register 5 (hex 0105).

Additional memory can be added in any of the micro channel connectors. The total amount of memory installed must not exceed the 16MB addressing limit. The total amount of usable memory is less than the amount of memory installed because of ROM-to-RAM remapping and split-memory-block remapping.

Error Recovery

If POST detects a memory error in any part of the system-board memory, an attempt is made to deactivate the physical 1MB block of memory that contains the error. The addresses assigned to the deactivated block are reassigned to the next physical block of system-board memory, if installed (the first 1MB of memory-address space cannot be assigned to memory installed in any of the micro channel connectors). If 1MB of valid system-board memory cannot be found, the system sets the memory size according to the last good memory available and allows a system reset; however, if a minimum of 64KB of good memory cannot be found, POST cannot recover from the error.

If the first physical 1MB of memory is disabled, the split-memory block and ROM-to-RAM remap feature will not be enabled.

System-Memory Map

Memory is mapped by System-Board POS Register 5 (hex 0105).

Warning: IBM recommends that programmable options be set only through the System-Configuration utilities. Directly setting the POS registers or CMOS RAM POS parameters can result in multiple assignments of the same system resource, improper operation of the feature, loss of data, or damage to the hardware.

The first 640KB of system-board RAM is mapped starting at address hex 000000. A 256-byte and 1KB portion of this RAM is reserved as BIOS data areas. See the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* manual for details.

Figure 3-5 on page 3-10 shows the memory map for a properly functioning system. Memory can be mapped differently if POST detects an error in system-board memory or RT/CMOS RAM. In the following figure, the variable *X* represents the number of 1MB blocks of system-board memory starting at or above the hex 100000 boundary. The variable *Y* represents the number of 1MB blocks of addressable memory installed in the channel starting at or above the hex 100000 boundary (*Y* cannot exceed 14.75).

Hex Range	Function
000000 to 09FFFF	640KB System-Board RAM
0A0000 to 0BFFFF	128KB Video RAM
0C0000 to 0DFFFF	Feature ROM/RAM
0E0000 to 0FFFFF	128K System-Board ROM mapped to RAM
100000 to (100000 + *X*MB)	*X*MB System-Board RAM
(100000 + *X*MB) to (100000 + *X*MB + 256KB)	256KB System-Board RAM (Split-Memory Block)
(100000 + *X*MB + 256KB) to (100000 + *X*MB + 256KB + *Y*MB)	*Y*MB Channel RAM
(100000 + *X*MB + 256KB + *Y*MB) to FDFFFF	Not Used
FE0000 to FFFFFF	128KB System-Board ROM (Same as 0E0000 to 0FFFFF)

Figure 3-5. System-Memory Map

System-Board Memory Connectors

The system board has two 72-pin memory connectors that support 1MB, 2MB, and 4MB memory cards. The following table shows the pin assignments for the connectors.

Pin	I/O	Signal	Pin	I/O	Signal
1	N/A	Ground	37	I/O	Parity Data 1
2	I/O	Data 0	38	I/O	Parity Data 1
3	I/O	Data 0	39	N/A	Ground
4	I/O	Data 1	40	O	CAS 0
5	I/O	Data 1	41	O	CAS 2
6	I/O	Data 2	42	O	CAS 3
7	I/O	Data 2	43	O	CAS 1
8	I/O	Data 3	44	O	RAS 0
9	I/O	Data 3	45	O	RAS 1
10	O	+5 Vdc	46	O	Block Select 1
11	O	-CAS Parity	47	O	Write Enable
12	O	Address 0	48	N/A	Reserved
13	O	Address 1	49	I/O	Data 8
14	O	Address 2	50	I/O	Data 8
15	O	Address 3	51	I/O	Data 9
16	O	Address 4	52	I/O	Data 9
17	O	Address 5	53	I/O	Data 10
18	O	Address 6	54	I/O	Data 10
19	N/A	Reserved	55	I/O	Data 11
20	I/O	Data 4	56	I/O	Data 11
21	I/O	Data 4	57	I/O	Data 12
22	I/O	Data 5	58	I/O	Data 12
23	I/O	Data 5	59	O	+5 Vdc
24	I/O	Data 6	60	I/O	Data 13
25	I/O	Data 6	61	I/O	Data 13
26	I/O	Data 7	62	I/O	Data 14
27	I/O	Data 7	63	I/O	Data 14
28	O	Address 7	64	I/O	Data 15
29	O	Block Select 0	65	I/O	Data 15
30	O	+5 Vdc	66	O	Block Select 2
31	O	Address 8	67	I	Presence Detect 0
32	O	Address 9	68	I	Presence Detect 1
33	O	RAS 3	69	I	Presence Detect 2
34	O	RAS 2	70	I	Presence Detect 3
35	I/O	Parity Data 0	71	O	Block Select 3
36	I/O	Parity Data 0	72	N/A	Ground

RAS = Row Address Strobe
CAS = Column Address Strobe

Figure 3-6. System-Board Memory Connectors

RT/CMOS RAM

The real-time clock/complementary metal-oxide semiconductor RAM (RT/CMOS RAM) chip contains the real-time clock and 64 bytes of CMOS RAM. The clock circuitry uses 14 bytes of this memory, and the rest is allocated to configuration and system-status information.

In addition to the 64 bytes of CMOS RAM, a 2KB CMOS RAM extension is provided for configuration and other system information.

A battery is built into each chip to keep the RT/CMOS RAM and the 2KB CMOS RAM extension active when the power supply is not in operation.

The following table shows the RT/CMOS RAM bytes and their addresses.

Address (Hex)	RT/CMOS RAM Bytes
000 - 00D	Real-Time-Clock Bytes
00E	Diagnostic-Status Byte
00F	Shutdown-Status Byte
010	Diskette-Drive-Type Byte
011 - 013	Reserved
014	Equipment Byte
015, 016	Low- and High-Base Memory Bytes
017, 018	Low- and High-Expansion Memory Bytes
019 - 031	Reserved
032, 033	Configuration CRC Bytes
034 - 036	Reserved
037	Date-Century Byte
038 - 03F	Reserved

Figure 3-7. RT/CMOS RAM Address Map

RT/CMOS Address and NMI Mask Register (Hex 0070)

This register is used in conjunction with the RT/CMOS Data register (hex 0071) to read from and write to the RT/CMOS RAM bytes.

Bit	Function
7	NMI Mask
6	Reserved
5 - 0	RT/CMOS RAM Address

Figure 3-8. RT/CMOS Address and NMI Mask Register (Hex 0070)

Warning: The operation following a write to hex 0070 should access hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Bit 7 When this bit is set to 1, the NMI is masked off (disabled). This bit is set to 1 by a power-on reset. This is a write-only bit.

Bit 6 This bit is reserved.

Bits 5 - 0 These bits are used to select RT/CMOS RAM addresses.

RT/CMOS Data Register (Hex 0071)

This register is used in conjunction with the RT/CMOS Address and NMI Mask register (hex 0070) to read from and write to the RT/CMOS RAM bytes.

Bit	Function
7 - 0	RT/CMOS Data

Figure 3-9. RT/CMOS Data Register (Hex 0071)

RT/CMOS RAM I/O Operations

During I/O operations to the RT/CMOS RAM addresses, interrupts should be masked to prevent other interrupt routines from changing the RT/CMOS Address register before data is read or written. After I/O operations, the RT/CMOS Address and NMI Mask register (hex 0070) should be left pointing to Status Register D (hex 00D).

Warning: The operation following a write to hex 0070 should access hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Writing to the RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS Address and NMI Mask register (hex 0070).
2. Write the data to the RT/CMOS Data register (hex 0071).

Reading from the RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Read the data from the RT/CMOS Data register (hex 0071).

Real-Time-Clock Bytes (Hex 000-00D)

Bit definitions and addresses for the real-time-clock bytes are shown in the following table.

Address (Hex)	Function	Byte Number
000	Seconds	0
001	Second Alarm	1
002	Minutes	2
003	Minute Alarm	3
004	Hours	4
005	Hour Alarm	5
006	Day of Week	6
007	Date of Month	7
008	Month	8
009	Year	9
00A	Status Register A	10
00B	Status Register B	11
00C	Status Register C	12
00D	Status Register D	13

Figure 3-10. Real-Time Clock Bytes

Note: The Setup program initializes Status Registers A, B, C, and D when the time and date are set. Interrupt hex 1A is the BIOS interface to read and set the time and date, and it initializes the register the same way as the Setup program.

Status Register A (Hex 00A)

Bit	Function
7	Update in Progress
6 - 4	22-Stage Divider
3 - 0	Rate-Selection Bits

Figure 3-11. Status Register A

Bit 7 When set to 1, this bit indicates that the time-update cycle is in progress. When set to 0, it indicates that the current date and time can be read.

Bits 6 - 4 These bits identify which time-base frequency is being used. The system initializes these bits to binary 010, which selects a 32.768-kHz time base. This is the only value supported by the system for proper timekeeping.

Bits 3 - 0 These bits allow the selection of a divider output frequency. The system initializes the rate selection bits to a binary 0110, which selects a 1.024-kHz, square-wave output frequency and a 976.562 microsecond periodic-interrupt rate.

Status Register B (Hex 00B)

Bit	Function
7	Set
6	Periodic-Interrupt Enable
5	Alarm-Interrupt Enable
4	Update-Ended Interrupt Enabled
3	Square-Wave Enabled
2	Date Mode
1	24-Hour Mode
0	Daylight-Saving Time Enabled

Figure 3-12. Status Register B

Bit 7 When set to 0, this bit updates the cycle, normally by advancing the counts at a rate of one per second. When set to 1, this bit immediately ends any update cycle in progress, and the program can initialize the 14 time bytes without any further updates occurring until this bit is set to 0.

Bit 6 This read/write bit allows an interrupt to occur at a rate specified by the rate and divider bits in Status Register A. When set to 1, this bit enables the interrupt. The system initializes this bit to 0.

Bit 5 When set to 1, this bit enables the alarm interrupt. The system initializes this bit to 0.

Bit 4 When set to 1, this bit enables the update-ended interrupt. The system initializes this bit to 0.

Bit 3 When set to 1, this bit enables the square-wave frequency as set by the rate-selection bits in Status Register A. The system initializes this bit to 0.

Bit 2 This bit indicates whether the binary-coded-decimal (BCD) or binary format is used for time and date calendar updates. When set to 1, this bit indicates the binary format. The system initializes this bit to 0.

Bit 1 This bit indicates if the hours byte is in 12-hour or 24-hour mode. When set to 1, this bit indicates the 24-hour mode. The system initializes this bit to 1.

Bit 0 When set to 1, this bit enables the daylight-saving-time mode. When set to 0, this bit disables the mode and the clock reverts to standard time. The system initializes this bit to 0.

Status Register C (Hex 00C)

Bit	Function
7	Interrupt-Request Flag
6	Periodic-Interrupt Flag
5	Alarm-Interrupt Flag
4	Update-Ended-Interrupt Flag
3 - 0	Reserved

Figure 3-13. Status Register C

Note: Interrupts are enabled by bits 6, 5, and 4 in Status Register B.

Bit 7 When set to 1, this bit indicates that an interrupt has occurred; bits 6, 5, and 4 indicate the type of interrupt.

Bit 6 When set to 1, this bit indicates that a periodic interrupt occurred.

Bit 5 When set to 1, this bit indicates that an alarm interrupt occurred.

Bit 4 When set to 1, this bit indicates that an update-ended interrupt occurred.

Bits 3 - 0 These bits are reserved.

Status Register D (Hex 00D)

Bit	Function
7	Valid RAM
6 - 0	Reserved

Figure 3-14. Status Register D

Bit 7 This read-only bit monitors the internal battery. When set to 1, this bit indicates that the real-time clock has power. When set to 0, it indicates that the real-time clock has lost power.

Bits 6 - 0 These bits are reserved.

CMOS RAM Configuration

The following shows the bit definitions for the CMOS RAM configuration bytes.

Diagnostic-Status Byte (Hex 00E)

Bit	Function
7	Real-Time Clock Chip Power
6	Configuration Record and Checksum Status
5	Incorrect Configuration
4	Memory-Size Mismatch
3	Fixed Disk Controller/Drive C Initialization Status
2	Time-Status Indicator
1	Adapter-Configuration Miscompare
0	Adapter-ID Time-Out

Figure 3-15. Diagnostic-Status Byte

Bit 7 When set to 1, this bit indicates that the real-time clock chip lost power.

Bit 6 When set to 1, this bit indicates that the checksum is incorrect.

Bit 5 This is a power-on check of the equipment byte (hex 014). When set to 1, this bit indicates that the configuration information is incorrect.

Bit 4 When set to 1, this bit indicates that the memory size does not match the configuration information.

Bit 3 When set to 1, this bit indicates that the controller or fixed disk drive failed initialization.

Bit 2 When set to 1, this bit indicates that the time is invalid.

Bit 1 When set to 1, this bit indicates that the adapters do not match the configuration information.

Bit 0 When set to 1, this bit indicates that a time-out occurred while an adapter ID was being read.

Shutdown-Status Byte (Hex 00F): This byte is defined by the power-on diagnostic programs.

Diskette-Drive-Type Byte (Hex 010): This byte indicates the type of diskette drive installed.

Bit	Function
7 - 4	First Diskette-Drive Type
3 - 0	Second Diskette-Drive Type

Figure 3-16. Diskette-Drive-Type Byte

Bits 7 - 4 These bits indicate the first diskette-drive type, as shown in the following table.

Bits 7 6 5 4	Function
0 0 0 0	No drive present
0 0 0 1	Double-sided diskette drive (48 tracks per inch, 360KB)
0 0 1 1	High-capacity diskette drive (720KB)
0 1 0 0	High-density diskette drive (1.44MB)

Note: All combinations that are not shown are reserved.

Figure 3-17. Diskette-Drive-Type Bits (Bits 7-4)

Bits 3 - 0 These bits indicate the second diskette-drive type, as shown in the following table.

Bits 3 2 1 0	Function
0 0 0 0	No drive present
0 0 0 1	Double-sided diskette drive (48 tracks per inch, 360KB)
0 0 1 1	High-capacity diskette drive (720KB)
0 1 0 0	High-density diskette drive (1.44MB)

Note: All combinations that are not shown are reserved.

Figure 3-18. Diskette-Drive-Type Bits (Bits 3-0)

Reserved Bytes (Hex 011 through 013): These bytes are reserved.

Equipment Byte (Hex 014): This byte defines the basic equipment in the system for the power-on diagnostic tests.

Bit	Function
7, 6	Number of Diskette Drives
5, 4	Display Operating Mode
3, 2	Reserved
1	Math Coprocessor Presence
0	Diskette-Drive Presence

Figure 3-19. Equipment Byte

Bits 7, 6 These bits indicate the number of diskette drives installed, as shown in the following table.

Bits 7 6	Number of Diskette Drives
0 0	One Drive
0 1	Two Drives
1 0	Reserved
1 1	Reserved

Figure 3-20. Number of Diskette-Drive Bits

Bits 5, 4 These bits indicate the operating mode of the display attached to the video port, as shown in the following table.

Bits 5 4	Display Operating Mode
0 0	Reserved
0 1	40-Column Mode
1 0	80-Column Mode
1 1	Monochrome Mode

Figure 3-21. Display-Operating-Mode Bits

Bits 3, 2 These bits are reserved.

Bit 1 When set to 1, this bit indicates that a math coprocessor is installed.

Bit 0 When set to 1, this bit indicates that a diskette drive is installed.

Low- and High-Base Memory Bytes (Hex 015 and 016): These bytes define the amount of memory below the 640KB address space.

The value from these bytes represents the number of 1KB blocks of base memory. For example, hex 0280 is equal to 640KB. The low byte is hex 015; the high byte is hex 016.

Low- and High-Expansion Memory Bytes (Hex 017 and 018): These bytes define the amount of memory above the 1MB address space.

The hexadecimal values in these bytes represent the number of 1KB blocks of expansion memory. For example, hex 0800 is equal to 2048KB. The low byte is hex 017; the high byte is hex 018.

Reserved Bytes (Hex 019 through 031): These bytes are reserved.

Configuration CRC Bytes (Hex 032 and 033): These bytes contain the cyclic-redundancy-check (CRC) data for bytes hex 010 through hex 031 of the 64-byte CMOS RAM. The low byte is hex 033; the high byte is hex 032.

Reserved Byte (Hex 034): This byte is reserved.

Low and High Useable Memory Bytes (Hex 035 and 036): These bytes define the total amount of useable memory above the 1MB.

The hexadecimal values in these bytes represent the number of 1KB

| blocks of useable memory. For example, hex 0800 is equal to
| 2048KB. The low byte is hex 35; the high byte is hex 36.

Date-Century Byte (Hex 037): Bits 7 through 0 of this byte contain the BCD value for the century. Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* manual for information about reading and setting this byte.

Reserved Bytes (Hex 038 through 03F): These bytes are reserved.

Miscellaneous System Functions and Ports

Nonmaskable Interrupt

The Nonmaskable interrupt (NMI) service signals the system microprocessor that a parity error, a channel check, a system channel time-out, or a system watchdog time-out has occurred. The NMI service stops all arbitration on the bus until bit 6 of the Arbitration register (I/O address hex 0090) is set to 0. This can result in lost data or an overrun error on some I/O devices. The NMI service masks all other interrupts, and the IRET instruction restores the interrupt flag to the state it was in before the interrupt. A system reset causes a reset of the NMI.

The NMI requests from system-board parity and channel check are subject to mask control with the NMI mask bit in the RT/CMOS Address and NMI Mask register. The watchdog timer and system channel time-out are not masked by this bit. (See "RT/CMOS Address and NMI Mask Register (Hex 0070)" on page 3-12.) The power-on default of the NMI mask is 1 (NMI disabled). Before NMI service is enabled after a power-on reset, the parity-check and channel-check states are initialized by POST.

Warning: The operation following a write to hex 0070 should access hex 0071; otherwise, intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

System-Control Port B (Hex 0061)

Bit definitions for the write and read functions of this port are shown in the following tables.

Bit	Function
7	Reset Timer 0 Output Latch (IRQ0)
6 - 4	Reserved
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-22. System-Control Port B (Write)

Bit	Function
7	Parity Check
6	Channel Check
5	Timer 2 Output
4	Toggles with Each Refresh Request
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-23. System-Control Port B (Read)

Bit 7 When set to 1 during a write operation, this bit resets IRQ0. When read as a 1, this bit indicates a parity check has occurred.

Bit 6 When read as a 1, this bit indicates a channel check has occurred.

Bit 5 When read, this bit indicates the condition of the timer 2 'output' signal.

Bit 4 When read, this bit toggles for each refresh request.

Bit 3 When set to 0, this bit enables channel check. This bit is set to 1 during a power-on reset.

Bit 2 When set to 0, this bit enables parity check. This bit is set to 1 during a power-on reset.

Bit 1 When set to 1, this bit enables speaker data.

Bit 0 When set to 1, this bit enables the timer 2 gate.

System-Control Port A (Hex 0092)

Bit	Function
7 - 5	Reserved
4	Watchdog-Timer Status
3	Security-Lock Latch
2	Reserved
1	Alternate Gate A20
0	Alternate Hot Reset

Figure 3-24. System-Control Port A

Bits 7 - 5 These bits are reserved.

Bit 4 This read-only bit indicates the watchdog timer status. When this bit is set to 1, a watchdog time-out has occurred. The Hardware Interface Technical Reference manuals contain more information about the Watchdog Timer.

Bit 3 This bit provides the security lock for the secured area of RT/CMOS RAM. When set to 1, this bit electrically locks the 8-byte, power-on password. Once this bit is set by POST, it can be cleared only by turning the system off.

Bit 2 This bit is reserved.

Bit 1 This bit is used to enable the 'address 20' signal (A20) when the microprocessor is in the real-address mode. When this bit is set to 0, A20 cannot be used in real mode addressing. This bit is set to 0 during a system reset.

Bit 0 This bit provides an alternative method of resetting the system microprocessor. This alternative method supports operating systems requiring faster operation than was provided on the IBM Personal Computer AT*. Resetting the system microprocessor switches the microprocessor from the protected mode to the real-address mode. The alternative reset takes 13.4 microseconds.

This bit is set to 0 by either a system reset or a write operation. When a write operation changes this bit from 0 to 1, the alternative-reset pin is pulsed high for 100 to 125 nanoseconds. The reset occurs after a minimum delay of 6.72 microseconds. While the reset is occurring, the latch

* Personal Computer AT is a trademark of the International Business Machines Corporation.

remains set so that POST can read this bit. If the bit is set to 0, POST assumes the system was just powered on. If the bit is set to 1, POST assumes a switch from the protected mode to the real mode has taken place.

When bit 0 is used to reset the system microprocessor to the real mode, use the following procedure:

1. Disable all maskable and nonmaskable interrupts.
2. Reset the system microprocessor by writing bit 0 to 1.
3. Issue a Halt instruction to the system microprocessor.

If this procedure is not followed, the results will be unpredictable.

Note: Whenever possible, BIOS or ABIOS should be used as an interface to reset the system microprocessor to the real mode.

Power-On Password

Eight bytes of RT/CMOS RAM are reserved for the power-on password and its check character. The eight bytes are initialized to hex 00. The microprocessor can access these bytes only during POST. After the completion of a POST, if a power-on password is installed, the password bytes are locked and cannot be accessed by a program. The power-on password can be from one to seven characters.

During power-on password installation, the password (1 to 7 keyboard scan codes), is stored in the security space.

Installing the password is a function of a program on the Reference Diskette. The power-on password does not appear on the screen when you install, change, or remove it. Once you install the power-on password, it can be changed only during POST.

The system unit cover can be physically locked to prevent access to the speaker/password security connector.

The Model 65 SX also has a keyboard password. For more information, see the Hardware Interface Technical Reference keyboard and auxiliary-device controller information.

Type 2 Serial-Port Controller

Some Type 2 serial controllers used on the Model 65 SX system board do not respond as described in the Hardware Interface Technical Reference serial controller information.

After the FIFO mode is enabled, bit 6 of the Interrupt Identification register is erroneously set to 0, indicating a Type 1 serial controller is installed. Any application program or operating system that uses bit 6 of the Interrupt Identification register as an indicator to determine FIFO support will default to the character mode. This indicator is ignored by the Model 65 SX ABIOS. Therefore, programs that operate through ABIOS can use the FIFO mode. The ABIOS routines also clear any error indications remaining after a mode change.

Some application programs reset the received-data-ready indication by writing bit 0 of the Line Status register as a 0. This method can cause compatibility problems and is not supported by Type 1 or Type 2 serial controllers. Compatibility problems can be avoided by resetting bit 0 of the Line Status register to 0. This can be accomplished by reading the data and discarding the data if it is not used.

Hardware Compatibility

The Model 65 SX maintains many of the interfaces used by the IBM Personal Computer AT. In most cases command and status organization of these interfaces is maintained.

The functional interfaces for the Model 65 SX are compatible with the following interfaces:

- The Intel** 8259 interrupt controllers (without edge triggering).
- The Intel 8253 timers driven from 1.193 MHz (timer 0 and 2 only).
- The Intel 8237 DMA controller-address/transfer counters, page registers, and status fields only. The Command and Request registers are not supported. The rotate and mask functions are not supported. The Mode register is partially supported.

** Intel is a trademark of the Intel Corporation.

- Generally compatible with the National Semiconductor** NS16550A serial-communications controller.
- The Intel 8088, 8086, 80286, and 80386 microprocessors.
- The Intel 8272 diskette-drive controller. The BIOS limits support to diskette drives that have a 3-millisecond step rate during recalibration.
- The Motorola** MC146818 Time of Day Clock command and status (CMOS reorganized).
- The Intel 8042 keyboard port at address hex 0060.
- Display modes supported by the IBM Monochrome Display and Printer Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter.
- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode.
- Generally compatible with the Intel 80387, 80287, and 8087 math coprocessors.

Whenever possible, BIOS or ABIOS should be used as an interface to reset the system microprocessor to the real mode.

The system microprocessor also can be reset to the real mode through bit 0 of port hex 0064 or hex 0092. When using either of these ports, you must perform the following procedure:

1. Disable all maskable and non-maskable interrupts.
2. Reset the system microprocessor.
3. Issue a Halt instruction to the system microprocessor.

If this procedure is not followed, the results will be unpredictable.

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