Keyboard ans Auxiliary Device Controller

Figures

Description

Input to the keyboard and auxiliary device controllers is through two connectors at the rear of the system unit. One connector is dedicated to the keyboard, the other is available for an auxiliary device. An auxiliary device can be any type of serial input device compatible with the controller interface. The device types include:

- Mouse
- Touchpad
- Trackball.

Both Type 1 and Type 2 controllers receive the serial data, check the parity, and present the data to the system as a byte of data at data port hex 0060. The Type 2 controller provides only 7 of the 32 internal addresses available on the Type 1, and two commands are not available on the Type 2. Also, the Type 1 controller can translate keyboard scan codes, and the Type 2 cannot. (To determine which controller is present, see the description for bit 6 of the Controller Command byte on page 8.)

Note: Because the Type 1 controller supports translation and the Type 2 does not, the keyboard must provide both scan set 1 and scan set 2.

The controller interrupts the system when data is available or waits for polling from the system microprocessor.

Address hex 0064 is the command/status port. When the system reads port hex 0064, it receives status information from the controller. When the system writes to the port, the controller interprets the byte as a command.

Secondary circuit protection is provided on the system board for the +5 Vdc line to the keyboard and auxiliary device.

Keyboard Password

Legal password characters are restricted to the 128 ASCII character set. The password can be up to seven bytes long but must be installed using the keyboard scan codes less than hex 80 (the controller does not compare keyboard scan codes greater than hex 7F). Scan code set 1 is recommended for all password operations.

While the password is enabled, the controller compares the incoming keyboard scan code against the installed password, and it discards all data from the keyboard and auxiliary device that does not match the password. After a match occurs, the controller is restored to normal operation and data is again passed to the system microprocessor.

The controller provides three commands for keyboard password operation; it does not provide a command to verify the installed password.

A4 Test Password Installed
A5 Load Password
A6 Enable Password.

The Test Password Installed command determines if a keyboard password is currently installed. The controlling program can use this command to determine if a keyboard password is loaded before enabling the password.

The Load Password command allows the system microprocessor to set a keyboard password in the controller at any time. The existing password is lost, and the new password becomes active. The keyboard password can be changed at any time and must be installed in scan-code format.

The Enable Password command places the controller in the secure mode. While in the secure mode, the controller intercepts the keyboard data stream and continuously compares it to the installed password pattern. The controller does not pass any information to the system microprocessor or accept any commands while the keyboard password is enabled. (To enable the 'address 20' signal while the password is enabled, use System Control Port A at address hex 0092.)

The controller provides four internal RAM locations to support the keyboard password: addresses hex 13, 14, 16, and 17. See "Controller Commands" on page 7 for the commands on reading and writing to these locations.

Hex Address	Description
13	Security on: If this byte is nonzero when the password is enabled, the controller loads this byte into the output buffer and generates a system interrupt.
14	Security off: If this byte is nonzero when the password is matched, the controller loads this byte into the output buffer and generates a system interrupt.
16 and 17	Make 1 and 2: While the password is enabled, the controller first compares the incoming scan code against these two bytes. If the incoming scan code matches one of these two bytes, the scan code is discarded before it is compared to the password. This allows the controller to ignore certain keystrokes such as that for the right and left shift keys.

Controller Status Register

The following table shows the Controller Status register.

Bit	Function
7	Parity Error
6	General Time-Out
5	Auxiliary Device Output Buffer Full
4	Inhibit Switch
3	Command/Data
2	System Flag
1	Input Buffer Full
0	Output Buffer Full

Figure 1. Controller Status Register, Read Port Hex 0064

Note: On the Type 1 controller, commands C1 and C2 place data in bits 7 through 4 of the Controller Status register. See commands C1 and C2 on page 10 for more information.

Bit 7 When set to 0, this bit indicates that the last byte of data received from the keyboard had odd parity. When a parity error occurs, this bit is set to 1 and hex FF is placed in the output buffer (the keyboard and auxiliary device use odd parity).

Bit 6 When set to 1, this bit indicates that a transmission was started by the keyboard but did not finish within the receive time-out delay, or that a transmission was started by the controller but the byte transmitted was not clocked out within the specified time limit.

When a receive time-out occurs, the controller places a hex FF in the output buffer. When a transmit time-out occurs, the controller places a hex FE in the output buffer.

The Type 1 controller also indicates a transmit time-out if a transmission was started and:

- The byte was clocked out, but a response was not received within the time limit (only this bit is set to 1).
- The byte was clocked out, but a response indicates a parity error (this bit and bit 7 are both set to 1).

Bit 5 This bit works in conjunction with bit 0. When this bit and bit 0 are set to 1, auxiliary device data is in the output buffer. When this bit is set to 0 and bit 0 is set to 1, keyboard or command controller response data is in the output buffer.

Bit 4 When set to 0, this bit indicates the password state is active and the keyboard is inhibited. When set to 1, this bit indicates the password state is inactive and the keyboard is not inhibited. See "Keyboard Password" on page 2 for more information.

Bit 3 The keyboard controller input buffer can be addressed as either address hex 0060 or 0064. Address hex 0060 is defined as the data port, and address hex 0064 is defined as the command/status port. Writing to address hex 0064 sets this bit to 1. The controller uses this bit to determine if the byte in its input buffer should be interpreted as a command byte or a data byte.

Bit 2 This bit is set to 0 or 1 by writing to the system flag bit (bit 2) in the Controller Command byte. This bit is set to 0 after a power-on reset.

Bit 1 When set to 1, this bit indicates that data has been written into the buffer, but the controller has not read the data. When the controller reads the input buffer, this bit returns to 0, indicating that the input buffer is empty.

On the Type 2 controller, this bit is also set to 1 while transmitting to the keyboard or auxiliary device. After the last bit is sent, this bit is reset to 0.

Bit 0 When set to 1, this bit indicates the controller has placed data into its output buffer but the system microprocessor has not yet read the data. When the system microprocessor reads the output buffer (address hex 0060), this bit returns to 0.

Input and Output Buffers

The output buffer is an 8-bit, read-only register at address hex 0060. When the output buffer is read, the controller sends information to the system microprocessor. The information can be keyboard scan codes, auxiliary device data, or data bytes from a controller command.

The input buffer is an 8-bit, write-only register at address hex 0060 or address hex 0064. When the input buffer is written to, the

input-buffer-full bit (bit 1) in the Controller Status Byte is set to 1. Data written to the input buffer through address hex 0064 is interpreted as a controller command. Data written to address hex 0060 is sent to the keyboard, unless the controller expects a data byte following a controller command. Bit 3 of the Controller Status register indicates whether the contents of the input buffer is a command or a data byte.

Note: Data should be written to the controller input buffer only if the input-buffer-full bit (bit 1) in the Controller Status register (address hex 0064) is 0.

Input and Output Ports

The input port consists of two signals driven to the controller by the keyboard and auxiliary device. The output port consists of eight signals driven by the controller to the keyboard, auxiliary device, or system interface. The following tables show the input port and the output port bytes.

Bit	Function
7 - 2	Reserved
1	Auxiliary Data In
0	Keyboard Data In

Figure 2. Input Port Definitions

Bit 7 - 2 Reserved.

Bit 1 This bit reflects the state of the 'data' line driven by the auxiliary device. For more information on the auxiliary device 'data' line, see "Auxiliary Device and System Timings" on page 13.

Bit 0 This bit reflects the state of the 'data' line driven by the keyboard.

Bit	Function
7	Keyboard Data Out
6	Keyboard Clock Out
5	IRQ12
4	IRQ01
3	Auxiliary Clock Out
2	Auxiliary Data Out
1	Gate Address Line 20
0	Reset Microprocessor

Figure 3. Output Port Definitions

Bit 7 This bit reflects the state of the 'data' line driven by the controller to the keyboard.

Bit 6 This bit reflects the state of the 'clock' line driven by the controller to the keyboard.

Bit 5 When set to 1, this bit indicates an interrupt has been generated by data from the auxiliary device in the output buffer. When the system reads the data from address hex 0060, this bit will be set to 0.

Bit 4 When set to 1, this bit indicates an interrupt has been generated by data from the keyboard or a command in the output buffer. When the system reads the data from address hex 0060, this bit will be set to 0.

Bit 3 This bit reflects the state of the 'clock' line driven by the controller to the auxiliary device.

Bit 2 This bit reflects the state of the 'data' line driven by the controller to the auxiliary device.

Bit 1 When this bit and bit 1 in port hex 0092 are set to 0, the system address line A20 is disabled and set to 0. This bit is set to 1 at power-on. (See "System Control Port A" in the system-specific technical reference.)

Bit 0 When set to 0, this bit resets the system microprocessor and holds it reset until the bit is set to 1.

Controller Commands

A command is a data byte written to the controller through address hex 0064. The commands are listed in order of their hex values; commands not listed are reserved.

20 - 3F Read Controller RAM: This command causes the controller to return the data contained in the internal address specified by bits 5 through 0 of this command. Internal address hex 00 is assigned as the Controller Command byte. The Type 2 controller supports only the internal addresses hex 00, 13, 14, 16, 17, 1D, and 1F.

Command hex 20 requests a read operation of the Controller Command byte. The controller returns the data to port hex 0060.

Bit	Function
7	Reserved
6	Keyboard Translate
5	Disable Auxiliary Device
4	Disable Keyboard
3	Reserved
2	System Flag
1	Enable Auxiliary Interrupt
0	Enable Keyboard Interrupt

Figure 4. Controller Command Byte

Bit 7 This bit is reserved.

Bit 6 When this bit is set to 1, the Type 1 controller translates the incoming keyboard scan codes to scan set 1. When this bit is set to 0, the controller passes the incoming scan codes without translation. Following power-on or a keyboard reset, the keyboard transmits using scan code set 2.

On the Type 2 controller, this bit cannot be set to 1; therefore, it can be used to determine the type of controller. Writing this bit as a 1 and reading it as a 0 indicates a Type 2 controller.

For keyboard operations that are compatible with IBM Personal Computers, the Type 1 controller is placed in the translate mode. To perform the same operations with the Type 2 controller, the keyboard is set up to transmit in scan code set 1 by using the Select Alternate Scan Codes command (see the Keyboard section for more information).

Note: For Type 1 controllers, this bit must be set to 0 while requesting the keyboard for its scan set. This prevents the controller from translating the keyboard response.

Bit 5 Setting this bit to 1 disables the auxiliary device interface by driving the 'clock' line low. Data is not received while the interface is disabled.

Bit 4 Setting this bit to 1 disables the keyboard interface by driving the 'clock' line low. Data is not received while the interface is disabled.

Bit 3 This bit is reserved.

Bit 2 The value written to this bit is placed in the system flag bit of the Controller Status register.

Bit 1 Setting this bit to 1 causes the controller to generate an interrupt (IRQ 12) when it places auxiliary device data into its output buffer.

Bit 0 Setting this bit to 1 causes the controller to generate an interrupt (IRQ 1) when it places keyboard or command controller response data into its output buffer.

60 - 7F Write to Controller RAM: Bits 5 through 0 of the command specify the address. Internal address hex 00 is assigned as the Controller Command byte. The Type 2 controller supports only the internal addresses hex 00, 13, 14, 16, 17, 1D, and 1F.

Command hex 0060 writes the Controller Command byte. The next byte of data written to address hex 0060 is placed in the Controller Command byte.

Warning: On the Type 2 controller, writing to unsupported internal addresses can cause the data to be transmitted to the keyboard.

A4 Test Password Installed: This command checks for a password currently installed in the controller. The test result is placed in the output buffer (address hex 0060 and IRQ 01). Hex FA means the password is installed; hex F1 means it is not installed.

A5 Load Password: This command initiates the Password Load procedure. Following this command, the controller takes input from the data port until a null (0) is detected. The null terminates password entry. (See "Keyboard Password" on page 2.)

A6 Enable Password: This command enables the controller password feature. This command is valid only when a password pattern is currently loaded in the controller. (See "Keyboard Password" on page 2.)

A7 Disable Auxiliary Device Interface: This command sets bit 5 of the Controller Command byte to 1. This disables the auxiliary device interface by driving the 'clock' line low. Data is not received while the interface is disabled.

A8 Enable Auxiliary Device Interface: This command sets bit 5 of the Controller Command byte to 0, releasing the auxiliary device interface.

AD Disable Keyboard Interface: This command sets bit 4 of the Controller Command byte to 1. This disables the keyboard interface by driving the 'clock' line low. Data is not received while the interface is disabled.

AE Enable Keyboard Interface: This command clears bit 4 of the Controller Command byte to 0, releasing the keyboard interface.

C0 Read Input Port: This command causes the controller to read its input port and place the data in its output buffer.

C1 Poll Input Port Low: This command causes the Type 1 controller to read its input port bits 3 through 0 and place them in bits 7 through 4 of the Controller Status register. This command is not supported by the Type 2 controller.

C2 Poll Input Port High: This command causes the Type 1 controller to read its input port bits 7 through 4 and place them in bits 7 through 4 of the Controller Status register. This command is not supported by the Type 2 controller.

D0 Read Output Port: This command causes the controller to read its output port and place the data in its output buffer. This command should be used only if the output buffer is empty.

D1 Write Output Port: The next byte of data written to address hex 0060 is placed in the controller output port. For this command, the Type 2 controller supports writing to only bit 1 (gate A20).

Note: For Type 1 controllers, bit 0 of the output port is connected to the 'reset' signal of the system microprocessor. Pulsing this bit resets the system.

D2 Write Keyboard Output Buffer: The next byte written to address hex 0060 input buffer is written to address hex 0060 output buffer as if initiated by the keyboard. An interrupt occurs if the interrupt is enabled.

D3 Write Auxiliary Device Output Buffer: The next byte written to address hex 0060 input buffer is written to address hex 0060 output buffer as if initiated by an auxiliary device. An interrupt occurs if the interrupt is enabled.

D4 Write to Auxiliary Device: The next byte written to address hex 0060 input buffer is transmitted to the auxiliary device.

E0 Read Test Inputs: This command causes the controller to read its test inputs and place the results in the output buffer. Test 0 (T0) is connected to the keyboard 'clock' line, and test 1 (T1) is connected to the auxiliary device 'clock' line. Data bit 0 represents T0, and data bit 1 represents T1.

F0 - FF Pulse Output Port: This command pulses selected bits in the controller output port for approximately 6 microseconds. Bits 3 through 0 select the respective bits in the controller output port. For example, when bit 0 of this command is set to 0, bit 0 of the output port is pulsed and the system microprocessor is reset.

Note: The only command supported for the Type 2 controller is hex FE, pulse bit 0.

Keyboard and Auxiliary Device Programming Considerations

The following are some programming considerations for the keyboard and auxiliary device controller:

- Address hex 0064 (Controller Status register) can be read at any time.
- The auxiliary-device-output-buffer-full bit in the Controller Status register indicates that the data in address hex 0060 came from the auxiliary device.
- Address hex 0060 and address hex 0064 should be written to only when the input-buffer-full bit and output-buffer-full bit in the Controller Status register are set to 0.
- To ensure that the buffer data is valid, disable the keyboard and auxiliary devices before initiating a command that causes the controller to generate output at port 60 (such as commands D1 and D3).
- When polling the Type 1 controller for the output-buffer-full condition, wait 7 microseconds from the buffer-full indication in the Controller Status register before reading the output buffer.

Auxiliary Device and System Timings

Data transmissions to and from the auxiliary device connector consist of an 11-bit data stream sent serially over the 'data' line. The following table shows the function of each bit.

Bit	Function
11	Stop bit (always 1)
10	Parity Bit (odd parity)
9	Data Bit 7 (most-significant)
8	Data Bit 6
7	Data Bit 5
6	Data Bit 4
5	Data Bit 3
4	Data Bit 2
3	Data Bit 1
2	Data Bit 0 (least-significant)
1	Start Bit (always 0)

Figure 5. Bit Definitions of Auxiliary-Device Data Stream

The parity bit is either 1 or 0, and the 8 data bits, plus the parity bit, always have an odd number of 1's.

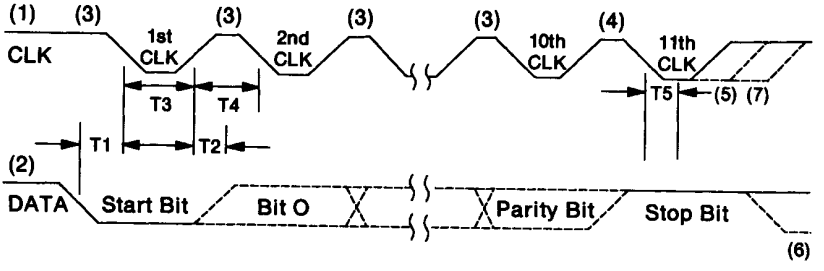
System Receiving Data

The following describes the typical sequence of events when the system is receiving data from the auxiliary device.

1. The auxiliary device checks the 'clock' line. If the line is inactive, output from the device is not allowed.
2. The auxiliary device checks the 'data' line. If the line is inactive, the controller receives data from the system.
3. The auxiliary device checks the 'clock' line during the transmission at intervals not exceeding 100 microseconds. If the device finds the system holding the 'clock' line inactive, the transmission is terminated. The system can terminate transmission anytime during the first 10 clock cycles.
4. A final check for terminated transmission is performed at least 5 microseconds after the 10th clock.
5. The system can hold the 'clock' signal inactive to inhibit the next transmission.
6. The system can set the 'data' line inactive if it has a byte to transmit to the device. The 'data' line is set inactive when the start bit (always 0) is placed on the 'data' line.

7. The system raises the 'clock' line to allow the next transmission.

The timing relationship is shown in the following figure.



	Timing Parameter	Min/Max
T1	Time from DATA transition to falling edge of CLK	5/25 μs
T2	Time from rising edge of CLK to DATA transition	5/T4 - 5 μs
T3	Duration of CLK inactive	30/50 μs
T4	Duration of CLK active	30/50 μs
T5	Time to auxiliary device inhibit after clock 11 to ensure the auxiliary device does not start another transmission	>0/50 μs

Figure 6. Receiving Data Timings

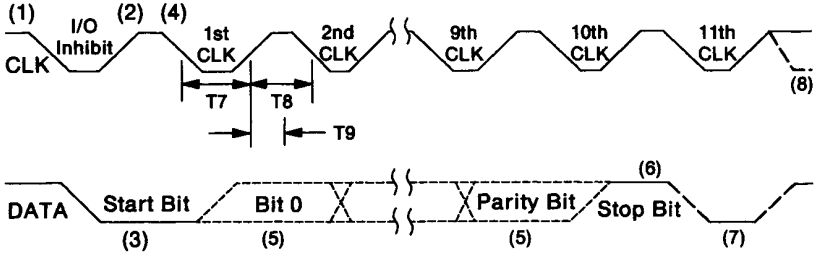
System Sending Data

The following describes the typical sequence of events when the system is sending data to the auxiliary device.

1. The system checks for an auxiliary device transmission in process. If a transmission is in process and beyond the 10th clock, the system must receive the data.
2. The auxiliary device checks the 'clock' line. If the line is inactive, an I/O operation is not allowed.
3. The auxiliary device checks the 'data' line. If the line is inactive, the system has data to transmit. The 'data' line is set inactive when the start bit (always 0) is placed on the 'data' line.
4. The auxiliary device sets the 'clock' line inactive. The system then places the first bit on the 'data' line. Each time the auxiliary device sets the 'clock' line inactive, the system places the next bit on the 'data' line until all bits are transmitted.
5. The auxiliary device samples the 'data' line for each bit while the 'clock' line is active. Data must be stable within 1 microsecond after the rising edge of the 'clock' line.

6. The auxiliary device checks for a positive-level stop bit after the 10th clock. If the 'data' line is inactive, the auxiliary device continues to clock until the 'data' line becomes active. Then it clocks the line-control bit and, at the next opportunity, sends a Resend command to the system.
7. The auxiliary device pulls the 'data' line inactive, producing the line-control bit.
8. The system can pull the 'clock' line inactive, inhibiting the auxiliary device.

The timing relationship is shown in the following figure.



	Timing Parameter	Min/Max
T7	Duration of CLK inactive	30/50 μs
T8	Duration of CLK active	30/50 μs
T9	Time from inactive to active CLK transition, used to time when the auxiliary device samples DATA	5/25 μs

Figure 7. Sending Data Timings

Signals

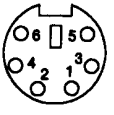
The keyboard and auxiliary device signals are driven by open-collector drivers pulled to 5 Vdc through a pull-up resistor. The following lists the characteristics of the signals.

Sink Current	20 mA	Maximum
High-Level Output Voltage	5.0 Vdc minus pullup	Minimum
Low-Level Output Voltage	0.5 Vdc	Maximum
High-Level Input Voltage	2.0 Vdc	Minimum
Low-Level Input Voltage	0.8 Vdc	Maximum

Figure 8. Keyboard and Auxiliary Device Signals

Connector

The keyboard and auxiliary device connectors use 6-pin miniature DIN connectors. The signals and voltages are the same for both connectors and are assigned as shown in the following table.



Pin	I/O	Signal Name
1	I/O	Data
2	NA	Reserved
3	NA	Ground
4	NA	+5 Vdc
5	I/O	Clock
6	NA	Reserved

Figure 9. Keyboard and Auxiliary Device Connector Information